

OPA640

Wideband Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- UNITY-GAIN BANDWIDTH: 1.3GHz
- UNITY-GAIN STABLE
- LOW NOISE: $2.9\text{nV}/\sqrt{\text{Hz}}$
- LOW HARMONICS: -75dBc at 10MHz
- HIGH COMMON MODE REJECTION: 85dB
- HIGH SLEW RATE: $350\text{V}/\mu\text{s}$

APPLICATIONS

- COMMUNICATIONS
- MEDICAL IMAGING
- TEST EQUIPMENT
- CCD IMAGING
- ADC/DAC GAIN AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LOW NOISE PREAMPLIFIER
- DIFFERENTIAL AMPLIFIER
- ACTIVE FILTERS

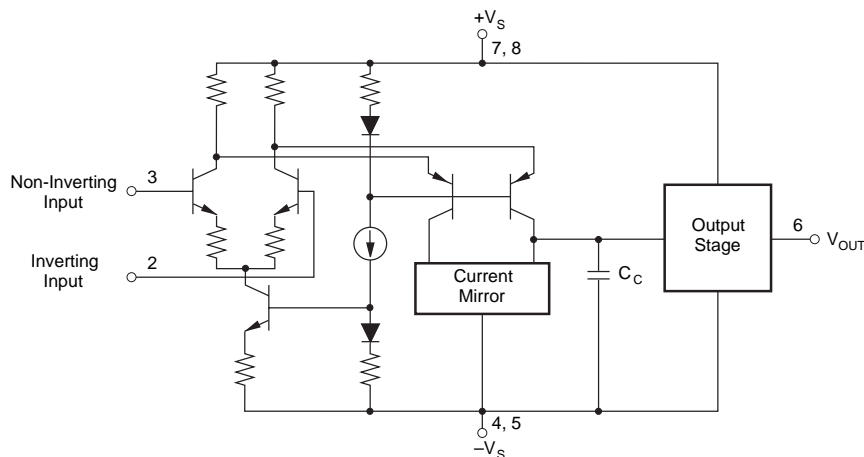
DESCRIPTION

The OPA640 is an extremely wideband operational amplifier featuring low noise, high common-mode rejection and high spurious free dynamic range.

The OPA640 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier

circuit architecture. This allows the OPA640 to be used in all op amp applications requiring high speed and precision.

Low noise, wide bandwidth, and high linearity make this amplifier suitable for a variety of RF and video applications.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

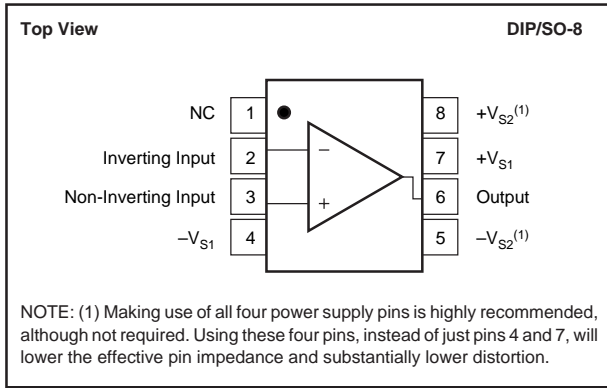
ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used, unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA640P, U			OPA640UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage Average Drift, Power Supply Rejection ($+V_S$) ($-V_S$)	$V_S = \pm 4.5$ to $\pm 5.5\text{V}$		± 2.0 ± 10 60 75 53	± 5		1.0 ± 6 *	± 2.0	mV $\mu\text{V}/^\circ\text{C}$ dB dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Over Specified Temperature Input Offset Current Over Specified Temperature	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		15 30 0.3 0.5	25 75 2.0 2.5		* 18 *	* 55 1.0 2.0	μA μA μA μA
NOISE Input Voltage Noise Density $f = 100\text{Hz}$ $f = 10\text{kHz}$ $f = 1\text{MHz}$ $f = 1\text{MHz}$ to 500MHz Voltage Noise, BW = 100Hz to 500MHz Input Bias Current Noise Density $f = 0.1\text{Hz}$ to 20kHz Noise Figure (NF) $R_S = 1\text{k}\Omega$ $R_S = 50\Omega$			7.0 2.8 2.8 2.9 65 2.0 2.6 10.9			* * * * * * * *	$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ μVrms $\text{pA}/\sqrt{\text{Hz}}$ dB dB	
INPUT VOLTAGE RANGE Common-Mode Input Range Over Temperature Common-Mode Rejection	$V_{CM} = \pm 0.5\text{V}$		± 2.5 ± 2.5 70	± 2.85 ± 2.75 85		* *	* 88	V V dB
INPUT IMPEDANCE Differential Common-Mode			15 1 2 1			* *		$\text{k}\Omega$ pF $\text{M}\Omega$ pF
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Over Specified Temperature	$V_O = \pm 2\text{V}$, $R_L = 100\Omega$ $V_O = \pm 2\text{V}$, $R_L = 100\Omega$		50 45	57 55		53 *	* *	dB dB
FREQUENCY RESPONSE Closed-Loop Bandwidth Slew Rate ⁽²⁾ At Minimum Specified Temperature Settling Time 0.01% 0.1% 1% Spurious Free Dynamic Range Gain Flatness to 0.1dB Differential Gain at 3.58MHz, $G = +2\text{V}/\text{V}$ Differential Phase at 3.58MHz, $G = +2\text{V}/\text{V}$	Gain = $+1\text{V}/\text{V}$ Gain = $+2\text{V}/\text{V}$ Gain = $+5\text{V}/\text{V}$ Gain = $+10\text{V}/\text{V}$ $G = +1$, 2V Step $G = +1$, 2V Step $G = +1$, 2V Step $G = +1$, 2V Step $G = +1$, 2V Step $G = +1$, $f = 5\text{MHz}$, $V_O = 2\text{Vp-p}$ $G = +1$, $f = 10\text{MHz}$, $V_O = 2\text{Vp-p}$ $G = +1$, $f = 20\text{MHz}$, $V_O = 2\text{Vp-p}$ $G = +1$ or $+2$ $V_O = 0\text{V}$ to 1.4V , $R_L = 150\Omega$ $V_O = 0\text{V}$ to 1.4V , $R_L = 150\Omega$		1.3 280 65 31 350 285 22 18 4.5 85 75 65 120 0.07 0.008			* * * * * * * * * * * * * * *		GHz MHz MHz MHz $\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$ ns ns ns dBc dBc dBc MHz %
OUTPUT Voltage Output Over Specified Temperature Voltage Output Over Specified Temperature Current Output, $+25^\circ\text{C}$ Over Specified Temperature Short Circuit Current Output Resistance	No Load $R_L = 100\Omega$ 1MHz, $G = +1\text{V}/\text{V}$		± 2.6 ± 2.25 ± 40 ± 25	± 3.0 ± 2.5 ± 52 ± 45 75 0.2		* * * * * * *		V V mA mA mA Ω
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current Over Specified Temperature	T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}		± 4.5	± 5 ± 5.5 ± 22 ± 24		* *	* * * *	V V mA mA
TEMPERATURE RANGE Specification: P, U, UB Thermal Resistance P 8-Pin DIP U, UB 8-Pin SO-8	Ambient θ_{JA} , Junction to Ambient		-40	+85		* * *	* *	$^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

PIN CONFIGURATION



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA640P	8-Pin Plastic DIP	006
OPA640U, UB	SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and package will be marked with a "B" by pin 8.

ABSOLUTE MAXIMUM RATINGS

Power Supply	$\pm 5.5\text{VDC}$
Internal Power Dissipation	Thermal Considerations
Differential Input Voltage	$\pm 1.2\text{V}$
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, U, UB	-40°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
(soldering, SO-8 3s)	$+260^\circ\text{C}$
Junction Temperature (T_J)	$+175^\circ\text{C}$



ELECTROSTATIC DISCHARGE SENSITIVITY

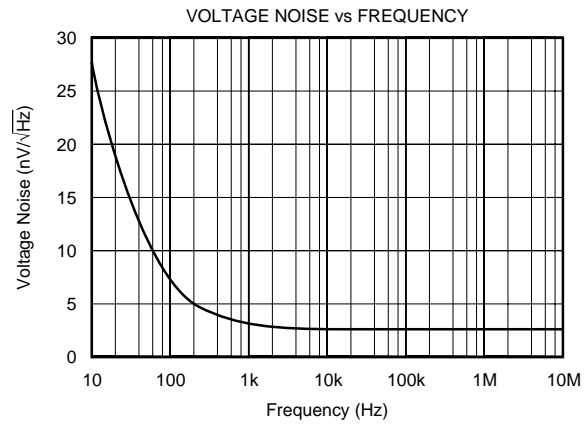
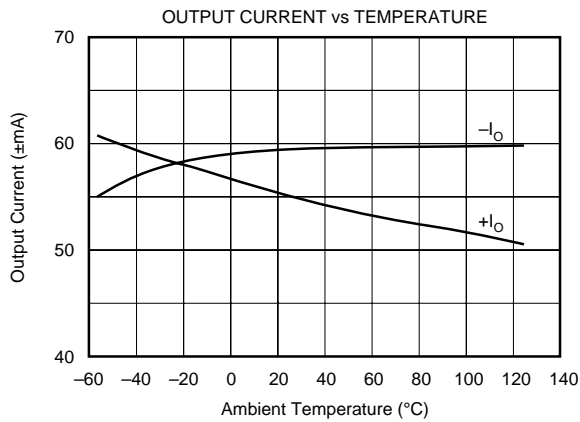
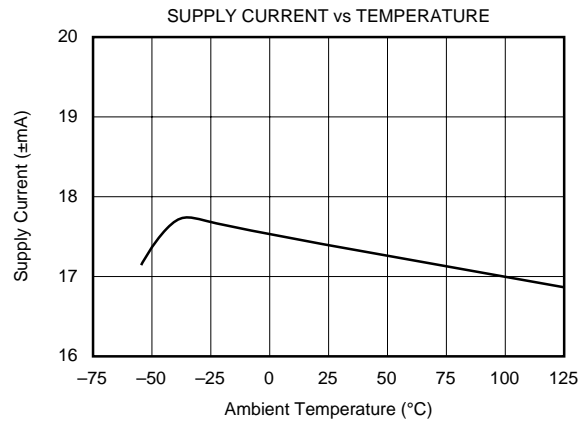
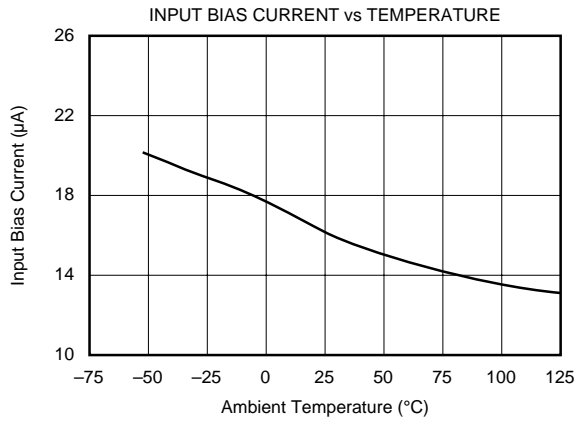
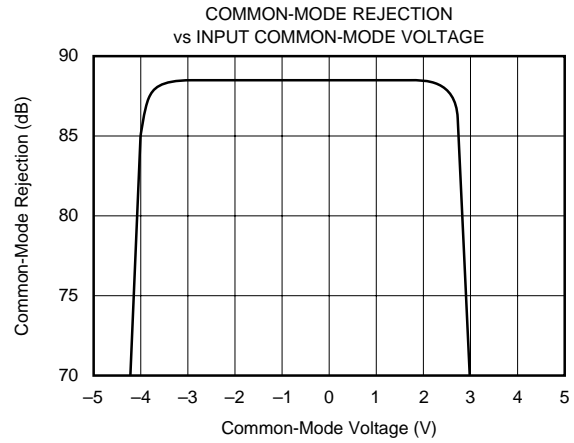
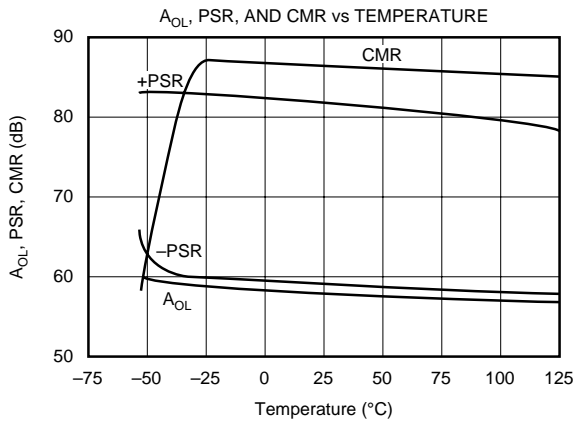
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

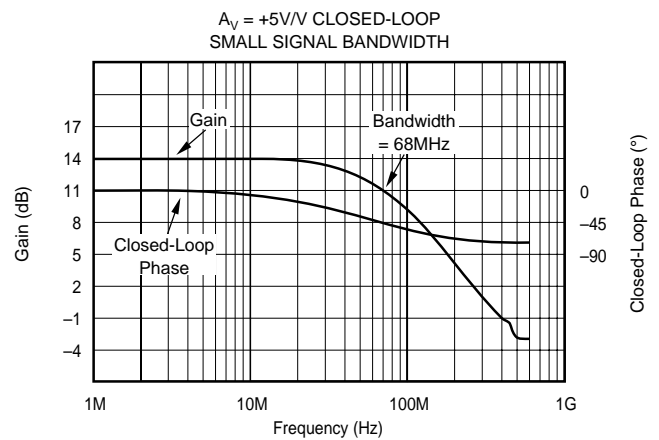
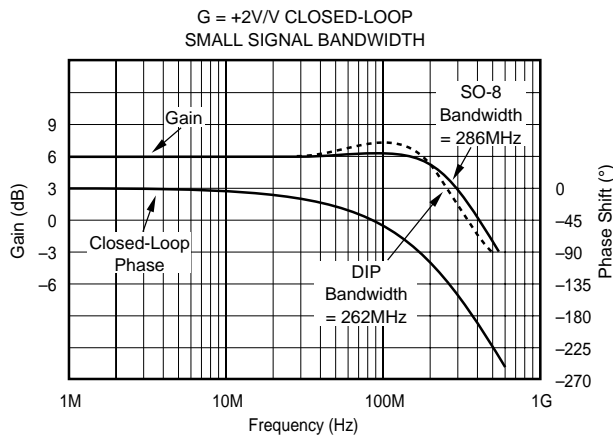
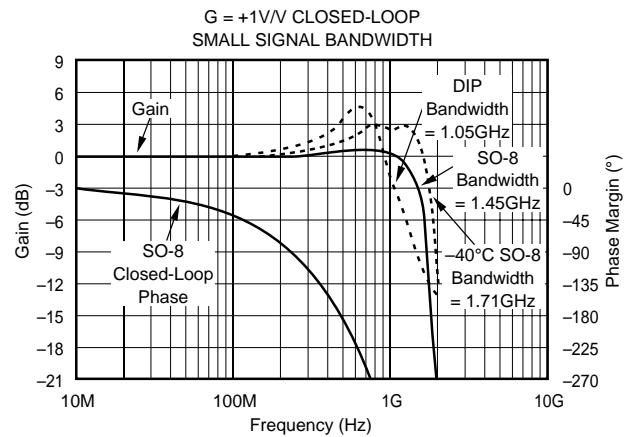
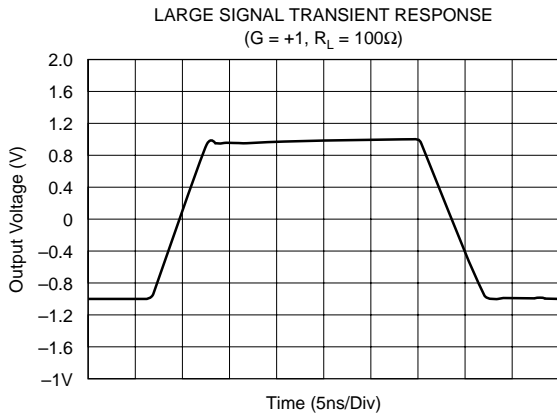
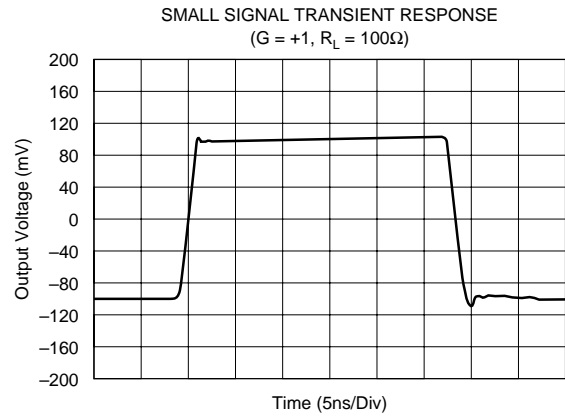
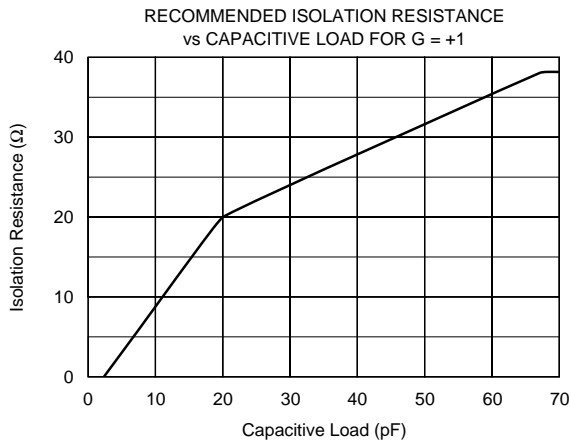
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used, unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



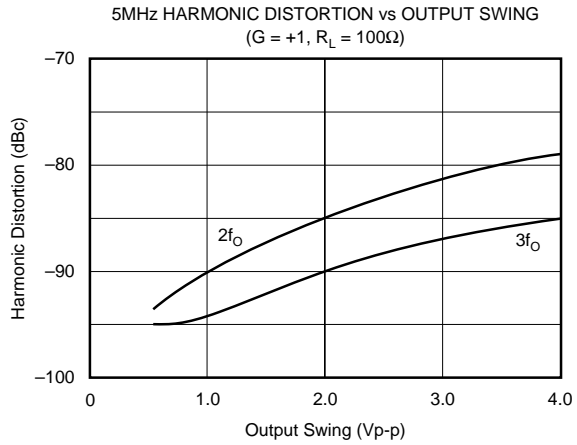
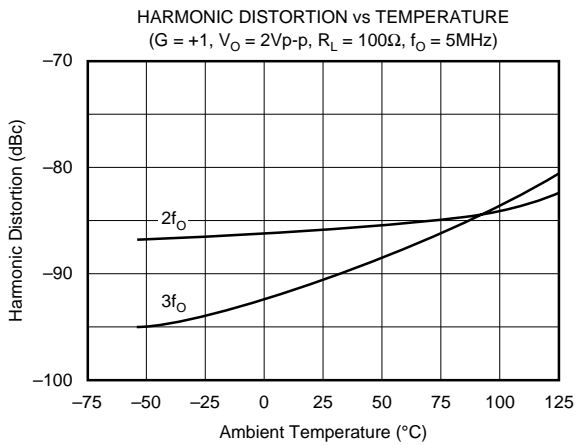
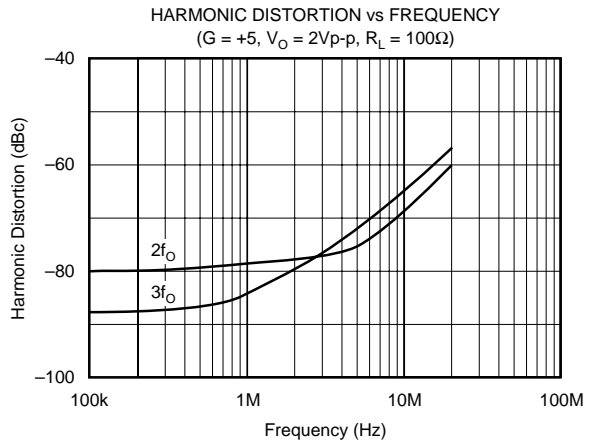
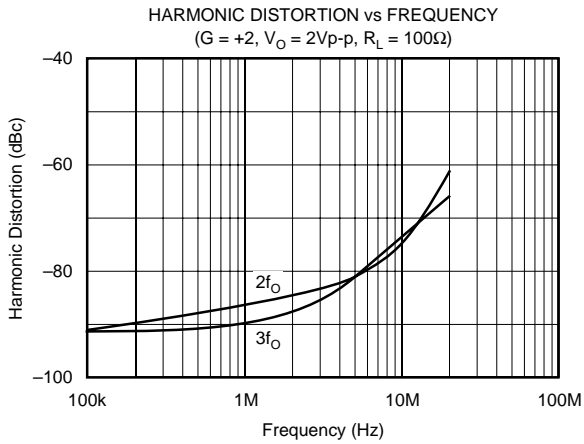
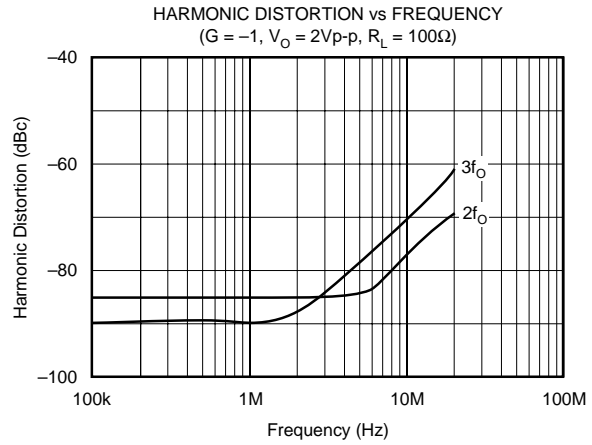
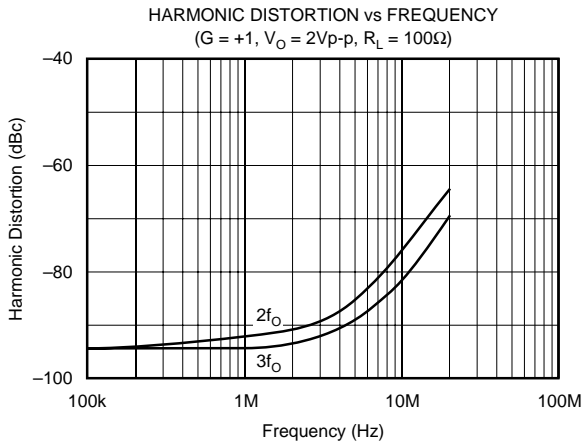
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used, unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



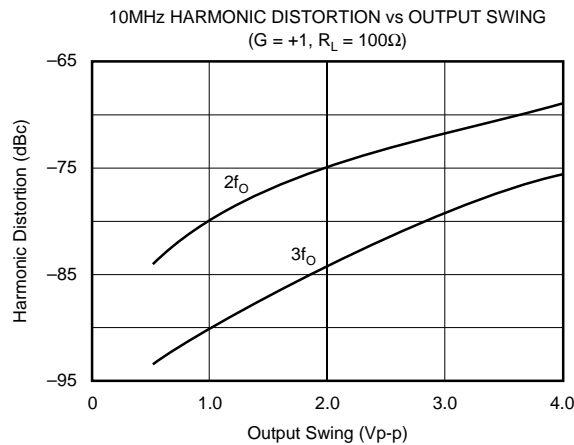
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used, unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used, unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA640 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA640's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors (due to input bias currents) through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA640's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA640.

WIRING PRECAUTIONS

Maximizing the OPA640's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and

instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA640, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2 μF) with very short leads are recommended. A parallel 0.01 μF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance **including lower distortion**. The lowest distortion is achieved when running separate traces to V_{S1} and V_{S2} . Power supply bypassing with $0.01\mu\text{F}$ and $2.2\mu\text{F}$ surface mount capacitors on the topside of the PC board is recommended. It is essential to keep the $0.01\mu\text{F}$ capacitor very close to the power supply pins. Refer to the DEM-OPA64X data sheet for the recommended layout and component placements.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA640 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about $1\text{k}\Omega$ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the data sheet. **A longer feedback path than this will decrease the realized bandwidth substantially.**

6) Due to the extremely high bandwidth of the OPA640, the SO-8 package is strongly recommended due its low parasitic impedance. The parasitic impedance in the DIP and package causes the OPA640 to experience about 5dB of gain peaking in unity-gain configurations. This is compared with virtually no gain peaking in the SO-8 package in unity-gain. The gain peaking in the DIP package is minimized in gains of 2 or greater, however. Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are also strongly recommended.

7) Avoid overloading the output. Remember that output

current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use $\pm 5\text{V}$ supplies. Although they will operate perfectly well with $+5\text{V}$ and -5.2V , use of $\pm 15\text{V}$ supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA640's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3 . This will reduce input bias current errors to the amplifier's offset current.

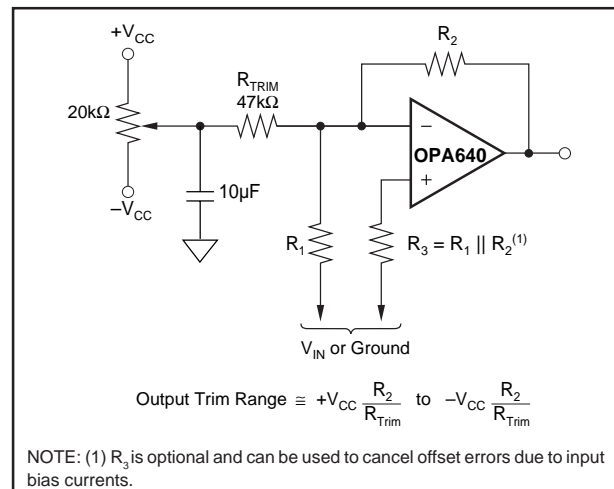


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA640 incorporates on-chip ESD protection diodes as shown in Figure 2.

This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA640 are internally protected from ESD

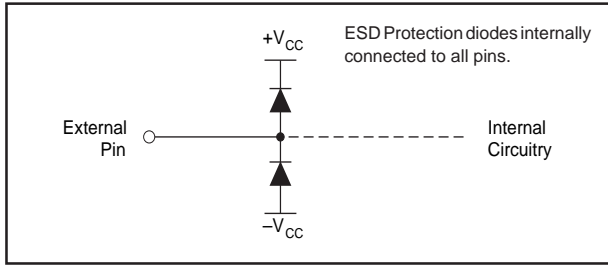


FIGURE 2. Internal ESD Protection.

by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA640 utilizes a fine geometry high speed process that withstands 500V using Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA640.

OUTPUT DRIVE CAPABILITY

The OPA640 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA640 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA640 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

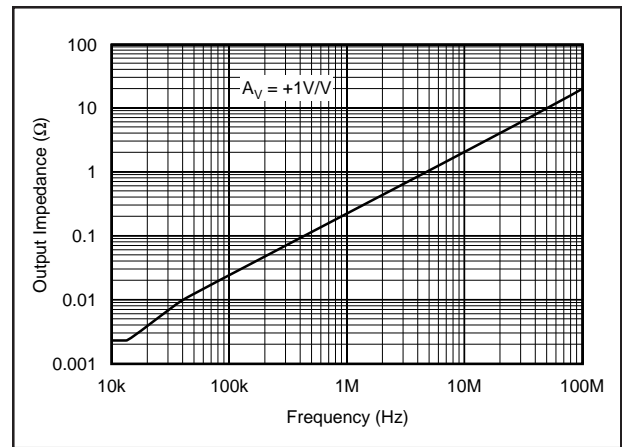


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA640 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 22mA = 220mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

A short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in Figure 4.

CAPACITIVE LOADS

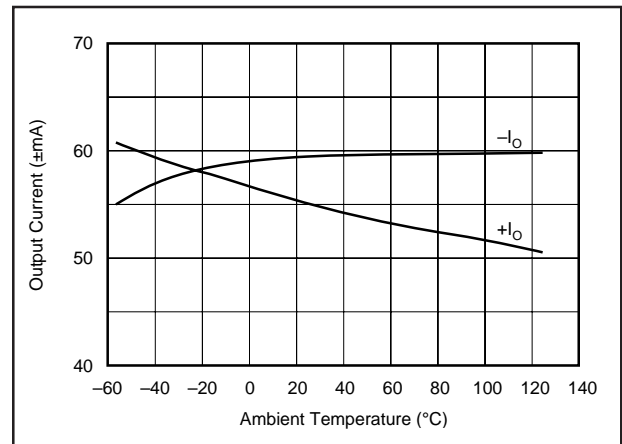


FIGURE 4. Output Current vs. Temperature.

The OPA640's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 2pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for opti-

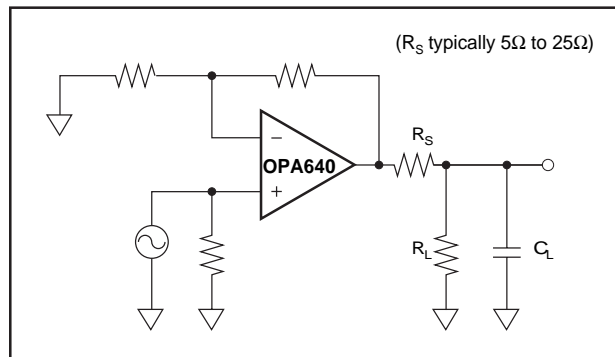


FIGURE 5. Driving Capacitive Loads.

imum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA640 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of $-1V/V$ is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA640 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve

the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of $\pm 200\mu V$ centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 15ns to 0.01% for a 2V step, making the OPA640 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 35ns.

In practice, settling time measurements on the OPA640 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA640's Harmonic Distortion characteristics vs frequency and power output are shown in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance. Refer to Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

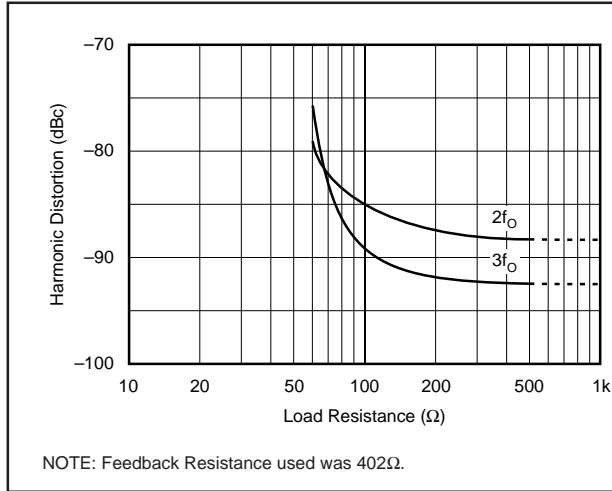


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 7 shows the OPA640's single tone, third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA640 to operate in a gain of +1V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 11 we find that the intercept point is +47dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - P_o)$$

$$\text{where OPI}^3\text{P} = \text{third-order intercept, dBm}$$

$$P_o = \text{output level, dBm}$$

For this case $\text{OPI}^3\text{P} = 47\text{dBm}$, $P_o = 47\text{dBm}$, and the third Harmonic = $2(47 - 10) = 74\text{dB}$ below the fundamental tone. The OPA640's low distortion makes the device an excellent choice for a variety of RF signal processing applications.

The value for the two-tone, third-order intercept is typically 8dB lower than the single tone value.

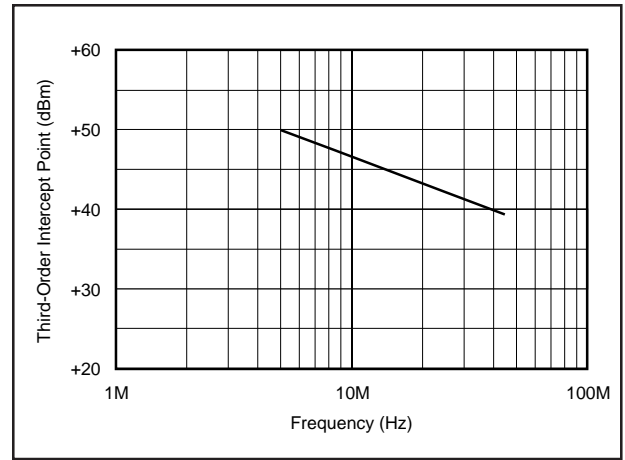


FIGURE 7. Single-Tone, 3rd-Order Intercept Point vs Frequency.

NOISE FIGURE

The OPA640 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA640's Noise Figure vs Source Resistance is shown in Figure 8.

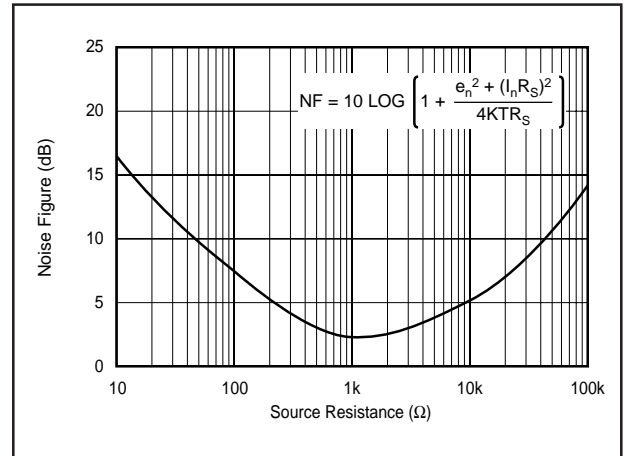


FIGURE 8. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA640. Contact Burr-Brown Applications Department to receive a spice diskette.

APPLICATIONS

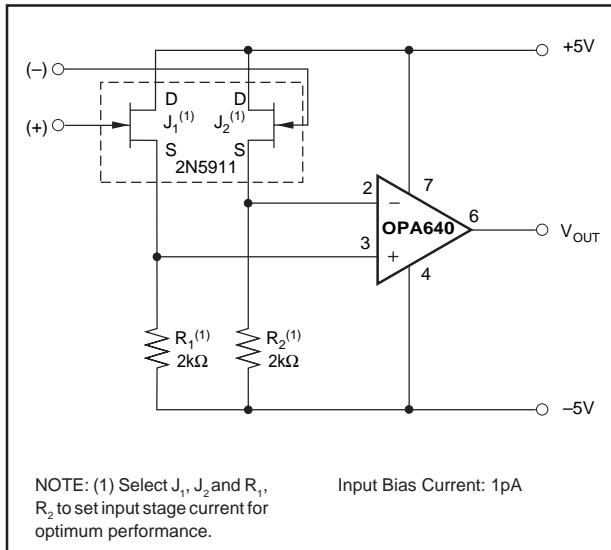


FIGURE 9. Low Noise, Wideband FET Input Op Amp.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x data sheet for details.

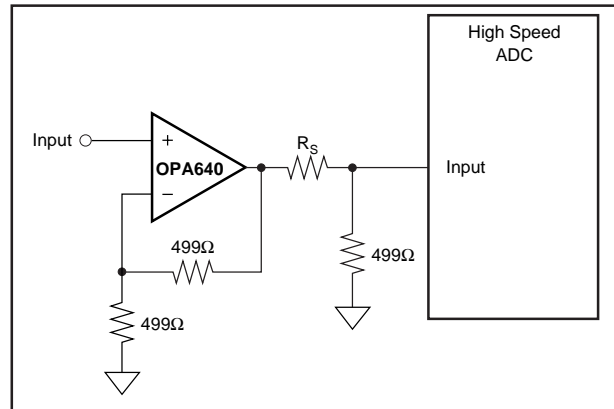


FIGURE 10. ADC Input Buffer Amplifier ($G = +2V/V$).

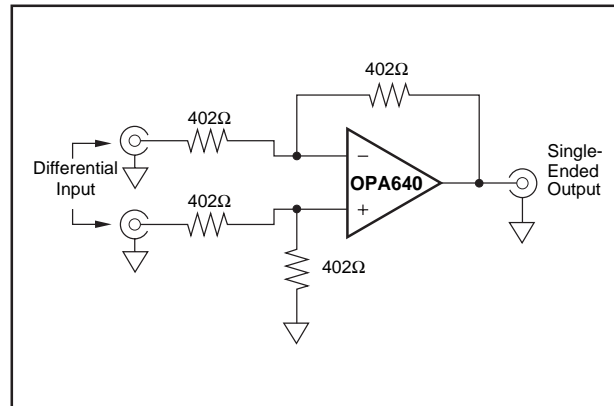


FIGURE 11. Unity Gain Difference Amplifier.

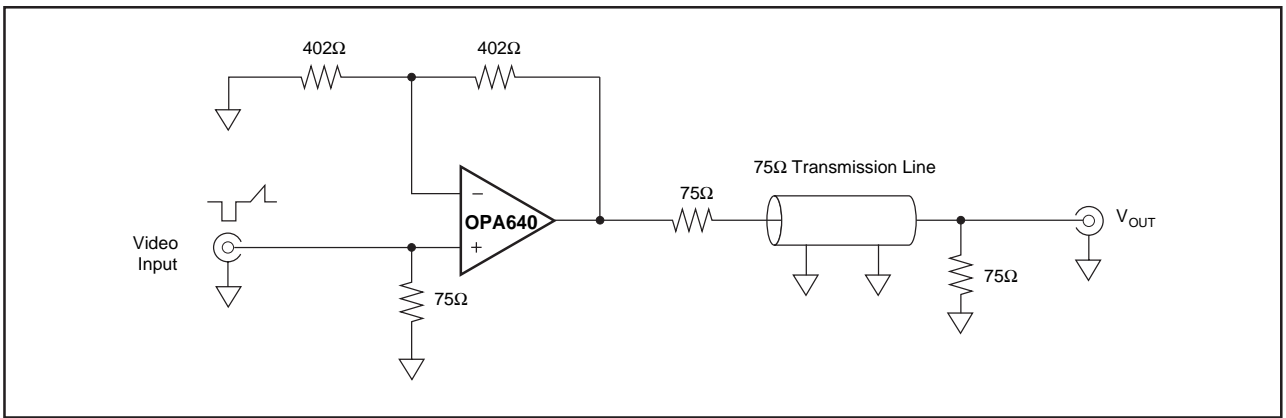


FIGURE 12. Video Gain Amplifier.

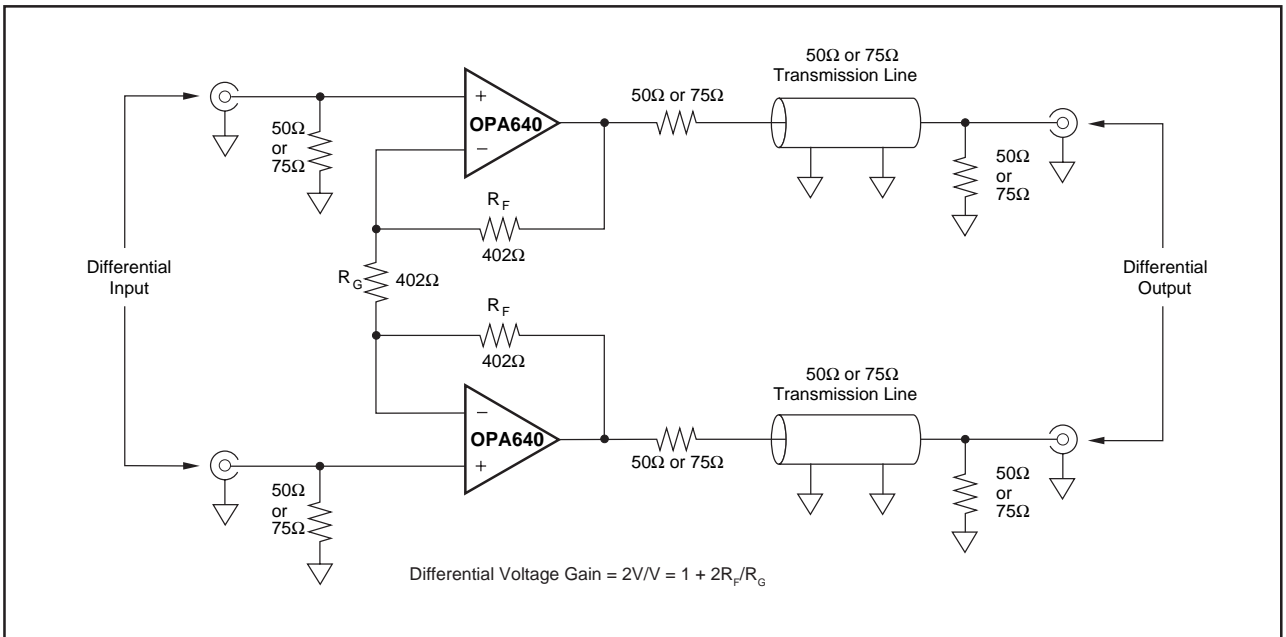


FIGURE 13. Differential Line Driver for 50Ω or 75Ω Systems.

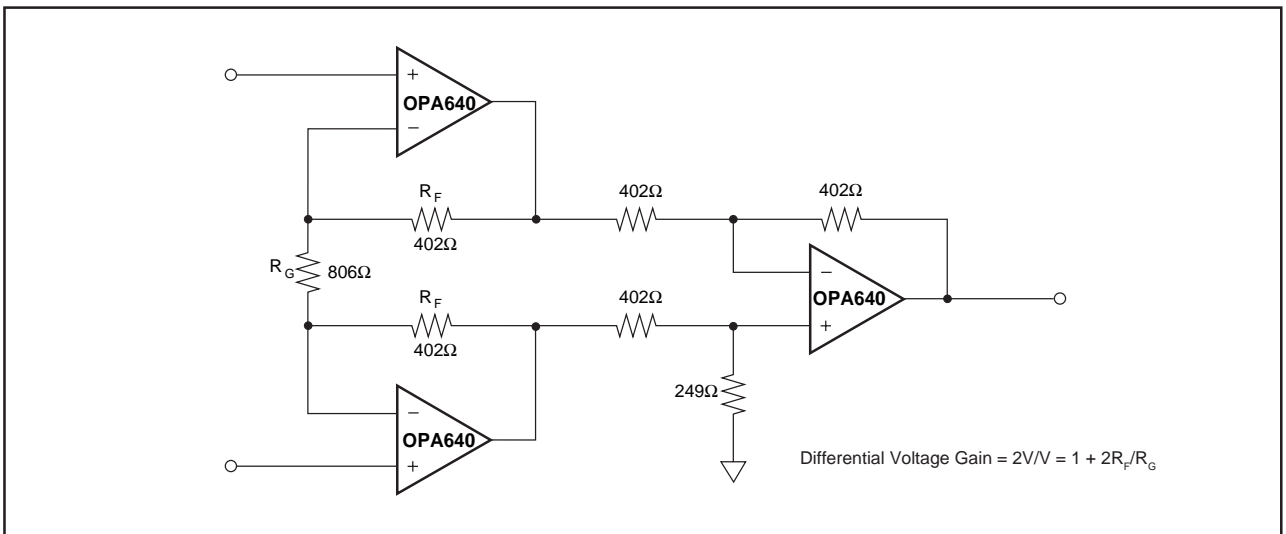


FIGURE 14. Wideband, Fast-Settling Instrumentation Amplifier.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.