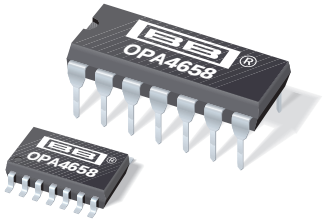
BURR - BROWN®



OPA4658

Quad Wideband, Low Power Current Feedback OPERATIONAL AMPLIFIER

FEATURES

- GAIN BANDWIDTH: 900MHz at G = 2
- GAIN OF 2 STABLE
- LOW POWER: 50mW PER AMP
- LOW DIFF GAIN/PHASE ERRORS: 0.015%/0.02°
- HIGH SLEW RATE: 1700V/µs
- PACKAGE: 14-Pin DIP and SO-14

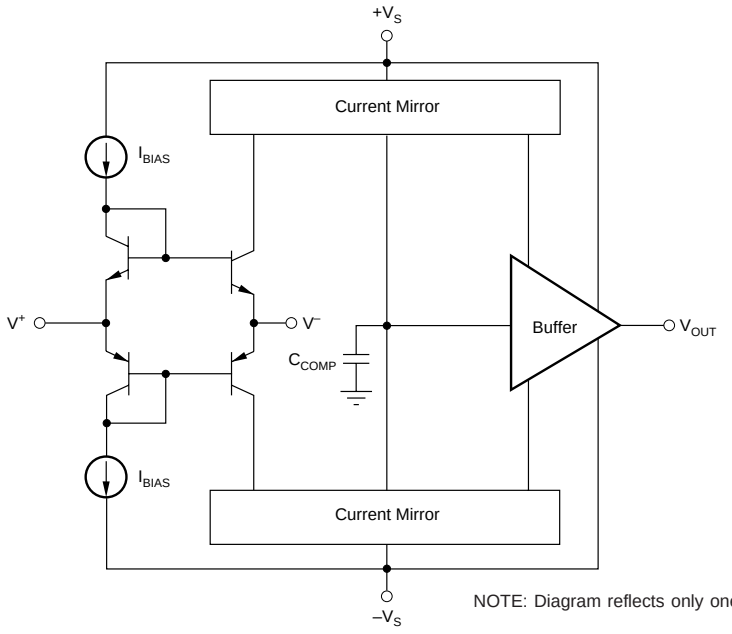
APPLICATIONS

- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

DESCRIPTION

The OPA4658 is a quad ultra-wideband, low power current feedback video operational amplifier featuring high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent current make the OPA4658 a perfect choice for numerous video, imaging and communications applications.

The OPA4658 is internally compensated for stability in gains of 2 or greater. The OPA4658 is also available in dual (OPA2658) and single (OPA658) configurations.



NOTE: Diagram reflects only one-fourth of the OPA4658.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1270C
Printed in U.S.A. March, 1998

SBOS047

SPECIFICATIONS

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, unless otherwise noted.

PARAMETER	CONDITION	OPA4658P, U			OPA4658UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Closed-Loop Bandwidth(2)	G = +2		450			*(1)		MHz
	G = +5		195			*		MHz
	G = +10		130			*		MHz
Slew Rate(3)	G = +2, 2V Step		1700		1000	*		V/µs
At Minimum Specified Temperature			1500		900	*		V/µs
Settling Time: 0.01%	G = +2, 2V Step		20			*		ns
0.1%	G = +2, 2V Step		15.1			*		ns
1%	G = +2, 2V Step		4.8			*		ns
Spurious Free Dynamic Range	f = 5MHz, G = +2, V_O = 2Vp-p		66			*		dBc
	f = 20MHz, G = +2, V_O = 2Vp-p		57			*		dBc
Third-Order Intercept Point	f = 10MHz		38			*		dBm
Differential Gain	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.015			*		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.02			*		degrees
Crosstalk	Input Referred, 5MHz, Three Active Channels		–74			*		dB
	Input Referred, 5MHz, Channel-to-Channel		–85			*		dB
OFFSET VOLTAGE								
Input Offset Voltage			±1.5	±5.5		±2	±5	mV
Over Temperature			±5	±8		±4	±8	mV
Power Supply Rejection	V_S = ±4.5 to ±5.5V	55	70		58	75		dB
INPUT BIAS CURRENT								
Non-Inverting	V_{CM} = 0V		±6.5	±30		*	±18	µA
Over Temperature			±10	±80		*	±35	µA
Inverting	V_{CM} = 0V		±1.1	±35		*	*	µA
Over Temperature			±30	±75		*	*	µA
NOISE								
Input Voltage Noise Density								
f = 100Hz			16			*		nV/√Hz
f = 10kHz			3.6			*		nV/√Hz
f = 1MHz			3.2			*		nV/√Hz
f_B = 100Hz to 200MHz			45			*		µVrms
Inverting Input Bias Current								
Noise Density: f = 10MHz			32			*		pA/√Hz
Non-Inverting Input Current								
Noise Density: f = 10MHz			12			*		pA/√Hz
Noise Figure (NF)	R_S = 100Ω		9.5			*		dBm
	R_S = 50Ω		11			*		dBm
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±2.9			*		V
Over Temperature		±2.5			*			V
Common-Mode Rejection	V_{CM} = ±1V	45	52		*	*		dB
INPUT IMPEDANCE								
Non-Inverting			500 || 1			*		kΩ ||pF
Inverting			25			*		Ω
OPEN-LOOP TRANSIMPEDANCE								
Open-Loop Transimpedance	V_O = ±2V, R_L = 100Ω	150	350		200	360		kΩ
Over Temperature	V_O = ±2V, R_L = 100Ω	100	290		150	300		kΩ
OUTPUT								
Voltage Output	No Load	±2.7	±3.0		*	*		V
Over Temperature		±2.5	±2.75		*	*		V
Voltage Output	R_L = 250Ω	±2.7	±3.0		*	*		V
Over Temperature		±2.5	±2.7		*	*		V
Voltage Output	R_L = 100Ω	±2.2	±2.7		*	*		V
Over Temperature		±2.0	±2.5		*	*		V
Output Current, Sourcing		80	120		*	*		mA
Over Temperature Range		70			*			mA
Output Current, Sinking		60	80		*	*		mA
Over Temperature Range		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	1MHz, G = +2		0.1			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current	All Channels, V_S = ±5V		±19	±31	±13	±20	±23	mA
Over Temperature			±20	±34		±21	±26	mA
TEMPERATURE RANGE								
Specification: P, U, UB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P			75			*		°C/W
U			75			*		°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Bandwidth can be affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

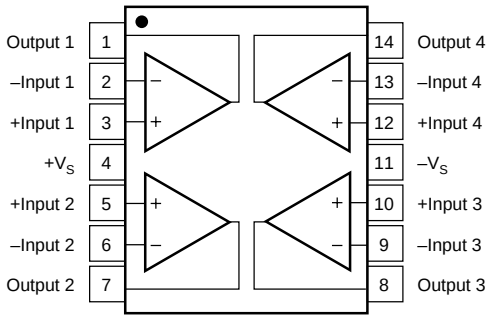
ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation[1]	See Applications Information
Differential Input Voltage	Total V_S
Input Voltage Range	See Applications Information
Storage Temperature Range: P, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PIN CONFIGURATION

Top View **DIP/SO-14**



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA4658P	14-Pin Plastic DIP	010
OPA4658U, UB	SO-14 Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION[1]

PRODUCT	PACKAGE	TEMPERATURE RANGE
OPA4658P	14-Pin Plastic DIP	–40°C to +85°C
OPA4658U, UB	SO-14 Surface Mount	–40°C to +85°C

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by pin 8. Refer to mechanical section for the location.

ELECTROSTATIC DISCHARGE SENSITIVITY

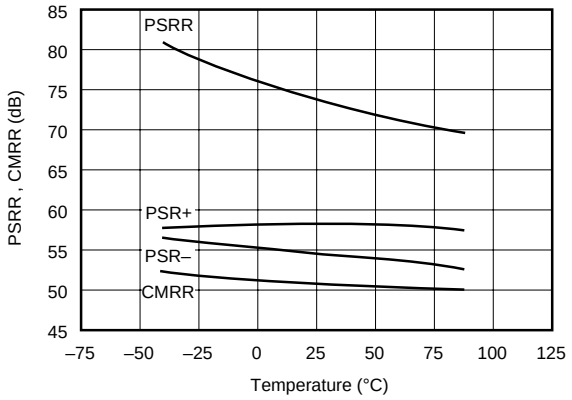
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

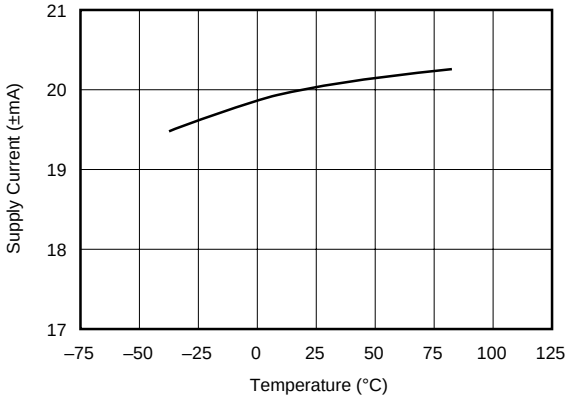
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, unless otherwise noted.

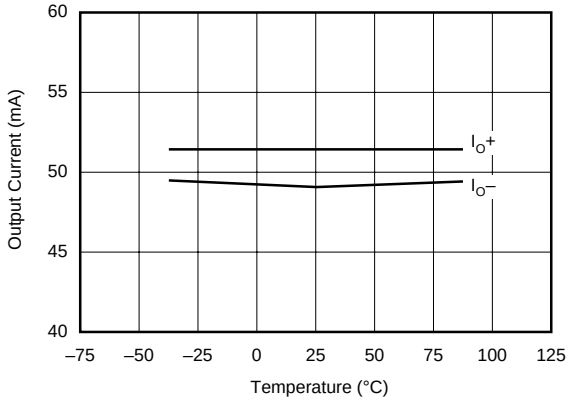
PSRR AND CMRR vs TEMPERATURE



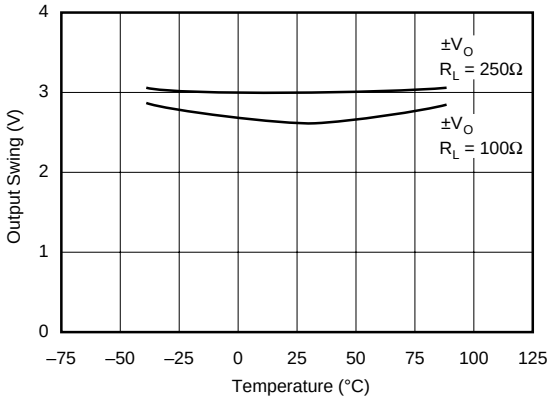
SUPPLY CURRENT vs TEMPERATURE
(Total of All Four Op Amps)



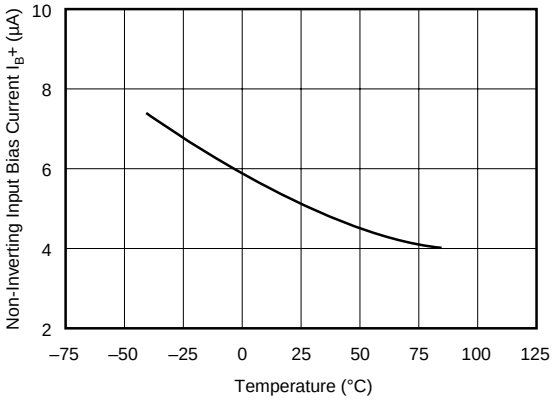
OUTPUT CURRENT vs TEMPERATURE



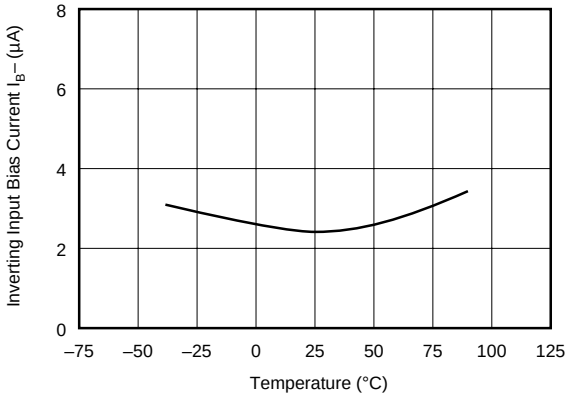
OUTPUT SWING vs TEMPERATURE



NON-INVERTING INPUT BIAS CURRENT
vs TEMPERATURE



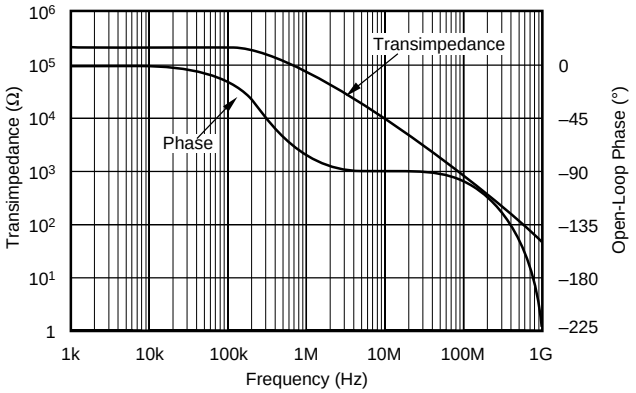
INVERTING INPUT BIAS CURRENT
vs TEMPERATURE



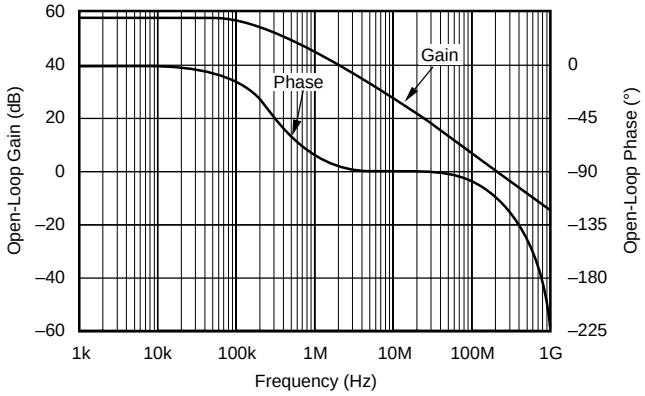
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, unless otherwise noted.

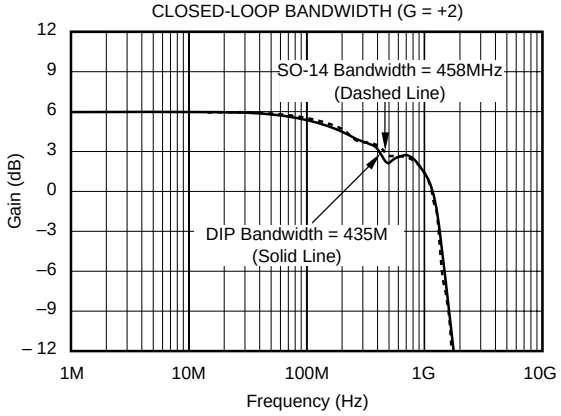
OPEN-LOOP TRANSIMPEDANCE AND PHASE vs FREQUENCY



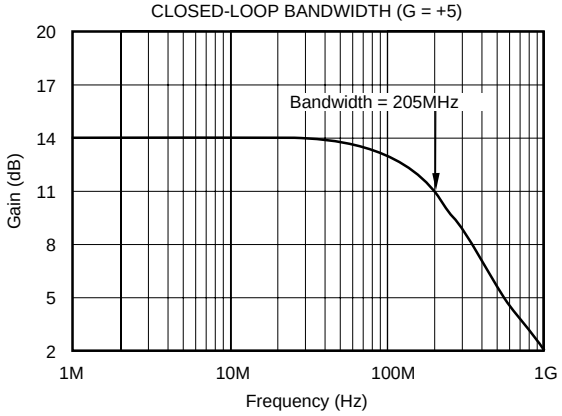
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



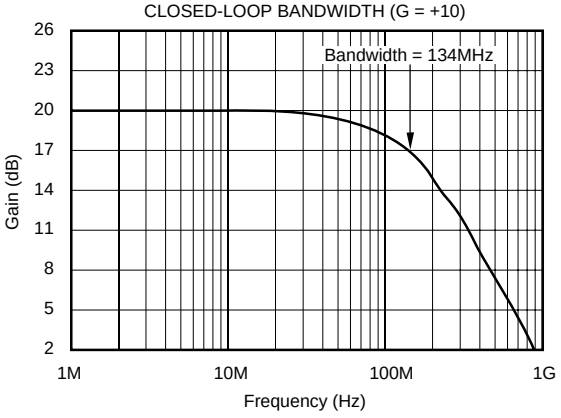
CLOSED-LOOP BANDWIDTH (G = +2)



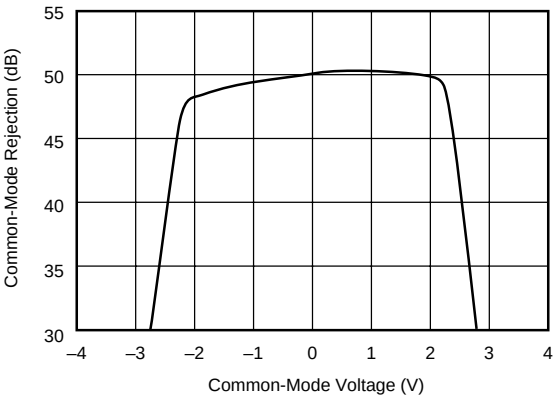
CLOSED-LOOP BANDWIDTH (G = +5)



CLOSED-LOOP BANDWIDTH (G = +10)



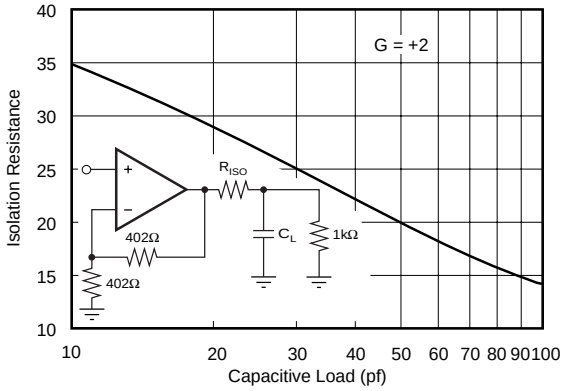
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



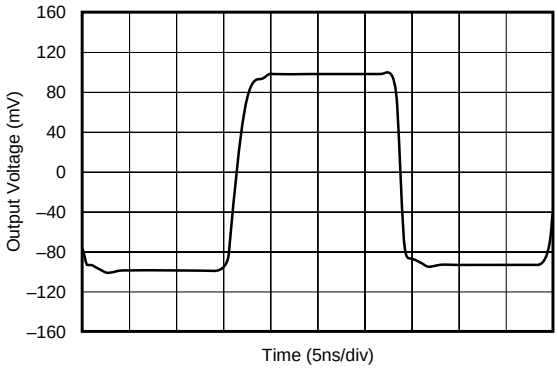
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, unless otherwise noted.

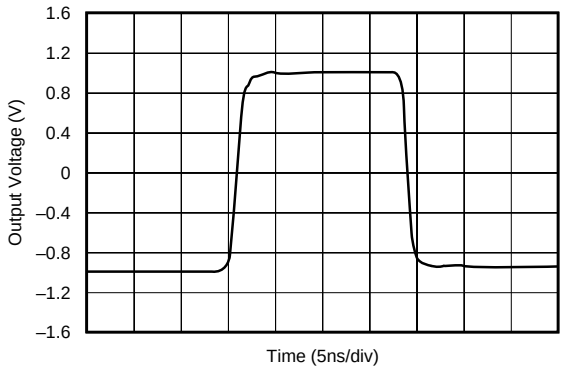
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



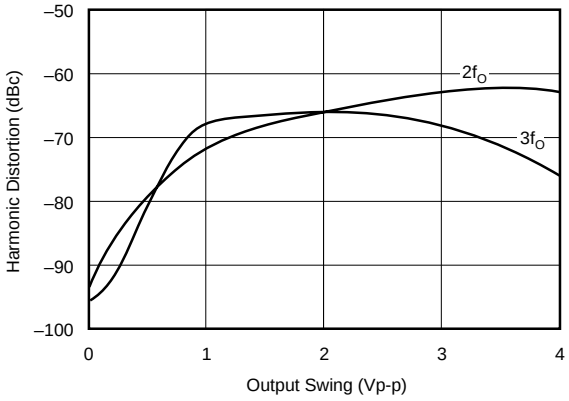
SMALL SIGNAL TRANSIENT RESPONSE (G = +2)



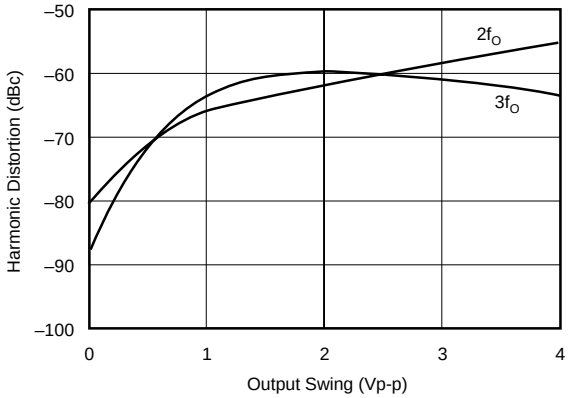
LARGE SIGNAL TRANSIENT RESPONSE (G = +2)



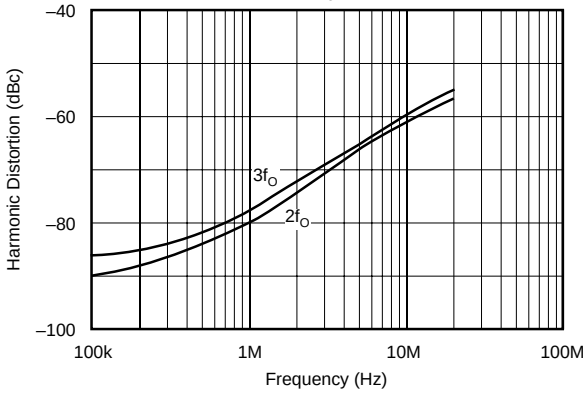
5MHz HARMONIC DISTORTION vs OUTPUT SWING (G = +2)



10MHz HARMONIC DISTORTION vs OUTPUT SWING (G = +2)



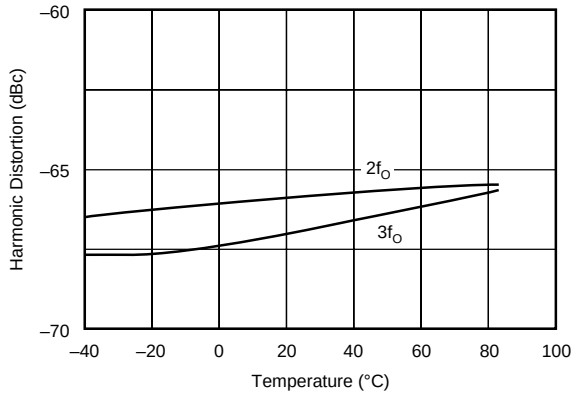
HARMONIC DISTORTION vs FREQUENCY (G = +2, V_O = 2Vp-p)



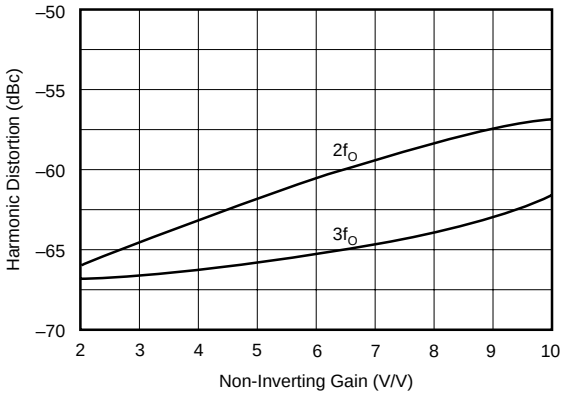
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, unless otherwise noted.

HARMONIC DISTORTION vs TEMPERATURE
(G = +2, V_O = 2Vp-p, f_O = 5MHz)



HARMONIC DISTORTION vs GAIN
(f_O = 5MHz, V_O = 2Vp-p)



APPLICATIONS INFORMATION

THEORY OF OPERATION

Conventional op amps depend on feedback to drive their inputs to the same potential, however the current feedback op amp's inverting and non-inverting inputs are connected by a unity gain buffer, thus enabling the inverting input to automatically assume the same potential as the non-inverting input. This results in very low impedance at the inverting input to sense the feedback as an error current signal.

DISCUSSION OF PERFORMANCE

The OPA4658 is a low-power, unity gain stable, current feedback operational amplifier which operates on ±5V power supply. The current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and (2) there is very little bandwidth degradation at higher gain settings.

The current feedback architecture of the OPA4658 provides the traditional strength of excellent large signal response plus wide bandwidth, making it a good choice for use in high resolution video, medical imaging and DAC I/V Conversion. The low power requirements make it an excellent choice for numerous portable applications.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to T_O x I_E. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

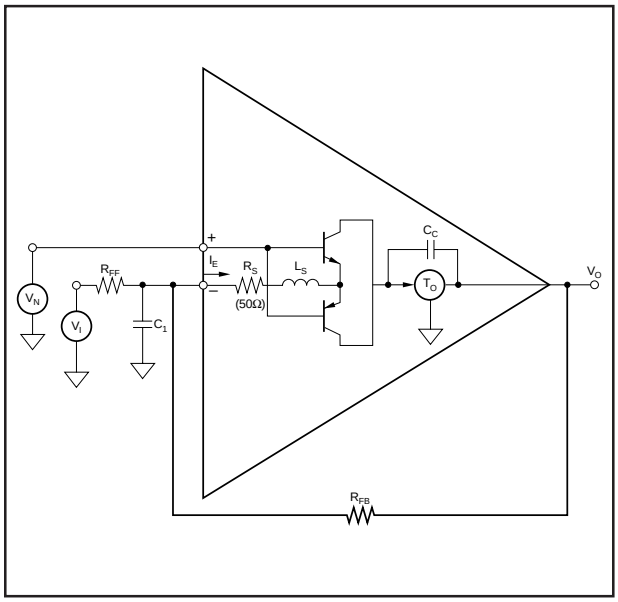


FIGURE 1. Equivalent Circuit.

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is $(1 + R_{FB}/R_{FF})$. Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA4658 can be calculated using the following equations:

$$\text{Inverting Gain} = \frac{-\left(\frac{R_{FB}}{R_{FF}}\right)}{1+\frac{1}{\text{Loop Gain}}} \quad (1)$$

$$\text{Non–Inverting Gain} = \frac{\left[1+\frac{R_{FB}}{R_{FF}}\right]}{1+\frac{1}{\text{Loop Gain}}} \quad (2)$$

$$\text{where Loop Gain} = \left[\frac{T_O}{R_{FB}+R_S\left(1+\frac{R_{FB}}{R_{FF}}\right)}\right]$$

At higher gains the small value inverting input impedance causes an apparent loss in bandwidth. This can be seen from the equation:

$$f_{\text{ACTUAL}}\ \text{BW} \approx \frac{\left[f_{(A_V=+2)}\ \text{BW}\right]\text{x}(1.25)}{\left[1+\left(\frac{R_S}{R_{FB}}\right)\times\left(1+\frac{R_{FB}}{R_{FF}}\right)\right]} \quad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 402Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input offset voltage and bias current errors. The output offset for non-inverting operation is calculated by the following equation:

$$\text{Output Offset Voltage} = \pm Ib_N \times R_N\left(1+\frac{R_{FB}}{R_{FF}}\right)\pm V_{IO}\left(1+\frac{R_{FB}}{R_{FF}}\right)\pm Ib_I \times R_{FB} \quad (4)$$

If all terms are divided by the gain $(1 + R_{FB}/R_{FF})$ it can be observed that input referred offsets improve as gain increases. The effective noise at the output can be determined by taking

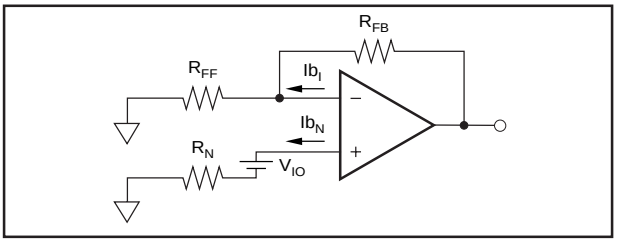


FIGURE 2. Output Offset Voltage Equivalent Circuit.

the root sum of the squares of equation (4) and applying the spectral noise values found in the Typical Performance Curve graph section. This applies to noise from the op amp only. Note that both the noise figure (NF) and the equivalent input offset voltages improve as the closed loop gain increases (by keeping R_{FB} fixed and reducing R_{FF} with $R_N = 0\Omega$).

INCREASING BANDWIDTH AT HIGH GAINS

The closed-loop bandwidth can be extended at high gains by reducing the value of the feedback resistor R_{FB}. This bandwidth reduction is caused by the feedback current being split between R_S and R_{FF} (refer to Figure 1). As the gain increases (for a fixed R_{FB}), more feedback current is shunted through R_{FF}, which reduces closed-loop bandwidth.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA4658 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA4658. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

The feedback resistor value acts as the frequency response compensation element for a current feedback type amplifier. The 402Ω used in setting the specification achieves a nominal maximally flat butterworth response while assuming a 2pF output pin parasitic. Increasing the feedback resistor will over compensate the amplifier, rolling off the frequency response, while decreasing it will decrease phase margin, peaking up the frequency response.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA4658 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high speed part like the OPA4658 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

ESD PROTECTION

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA4658.

OUTPUT DRIVE CAPABILITY

The OPA4658 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA4658 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA4658 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

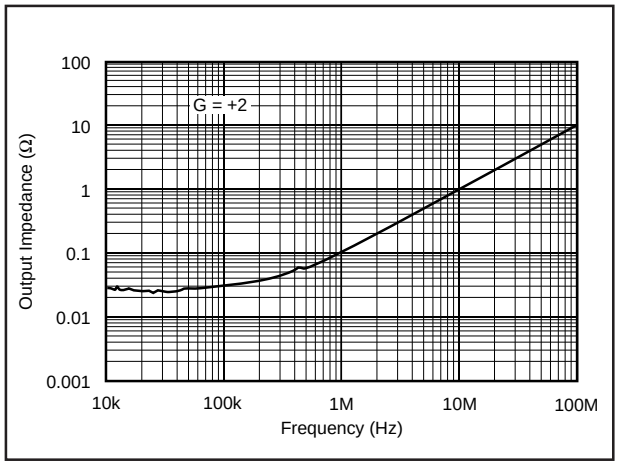


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA4658 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_S = \pm 5V$, $P_{DQ} = 10V \times 34mA = 340mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_S/2$, and is equal to P_{DL}, max = $(\pm V_S)^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA4658's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated with its characteristic impedance.

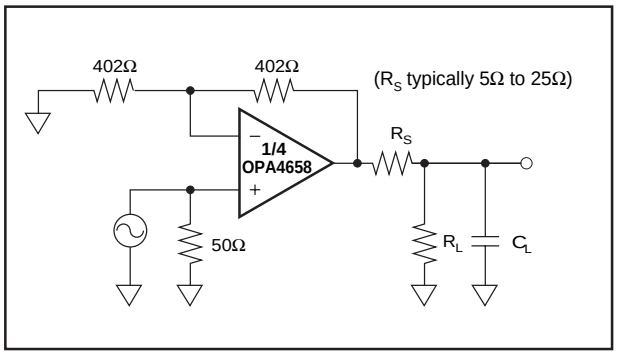


FIGURE 4. Driving Capacitive Loads.

COMPENSATION

The OPA4658 is internally compensated and is stable in gains of two or greater, with a phase margin of approximately 66° in a gain of +2V/V. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA4658 in a good layout is very flat with frequency.

DISTORTION

The OPA4658's Harmonic Distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

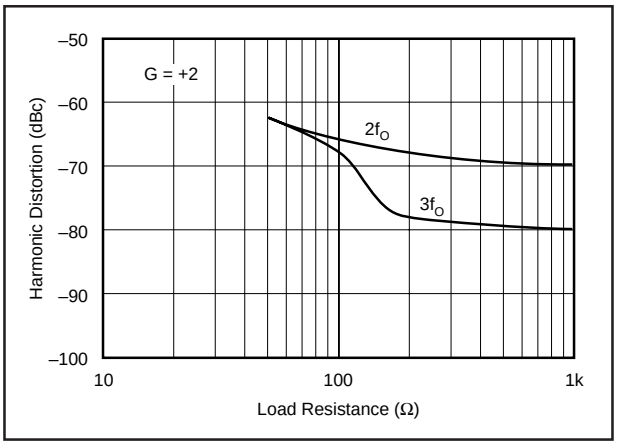


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept is an important parameter for many RF amplifier applications. Figure 6 shows the OPA4658's two tone, third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA4658 to operate in a gain of +2V/V and drive 2Vp-p into 100Ω at a frequency of 10MHz. Referring to Figure 6 we find that the intercept point is +38dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(OPI^3P - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level, dBm

For this case OPI^3P = 38dBm, P_O = 7dBm, and the third Harmonic = 2(38 – 7) = 62dB below the fundamental. The OPA4658's low distortion makes the device an excellent choice for a variety of RF signal processing applications.

CROSSTALK

Crosstalk is the undesired result of the signal of one channel mixing with and reproducing itself in the output of another channel or channels. Crosstalk is inclined to occur in most multichannel integrated circuits. In quad devices, the effect of crosstalk is measured by driving three channels and observing the output of the undriven channel over various frequencies. The magnitude of this effect is referenced in terms of channel-to-channel isolation and expressed in decibels. Input referred points to the fact that there is a direct correlation between gain and crosstalk, therefore at increased gain, crosstalk also increases by a factor equal to that of the gain. Figure 7 illustrates the measured effect of crosstalk in the OPA4658U.

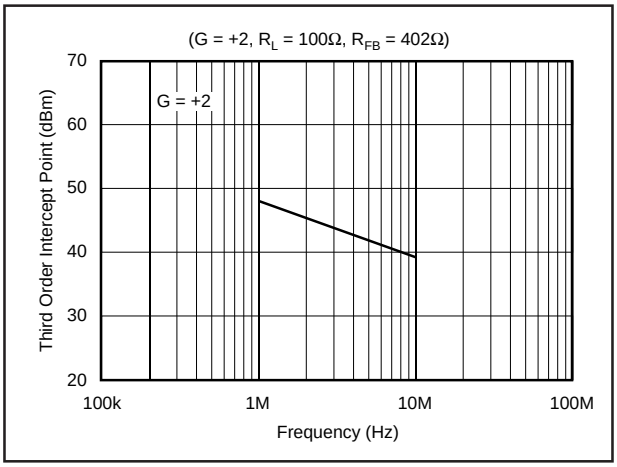


FIGURE 6. Third Order Intercept Point vs Frequency.

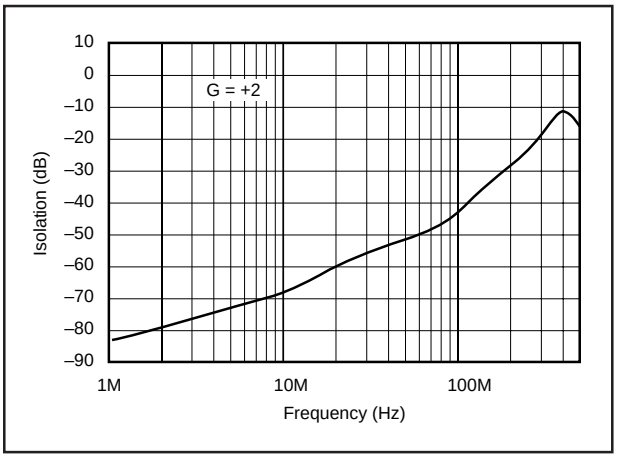


FIGURE 7. Channel-to-Channel Isolation (three active channels).

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are critical specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA4658 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 8 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer

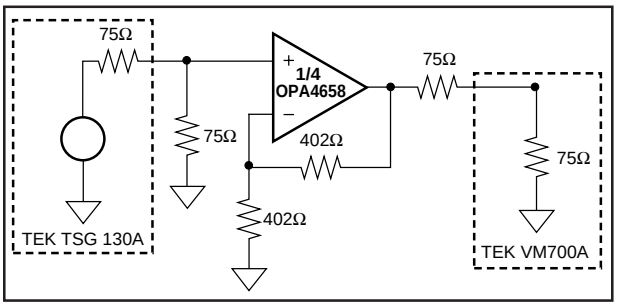


FIGURE 8. Configuration for Testing Differential Gain/Phase.

was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA4658 is 0.015% differential gain and 0.02° differential phase to both NTSC and PAL standards.

NOISE FIGURE

The OPA4658's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA4658's Noise Figure vs Source Resistance is shown in Figure 9.

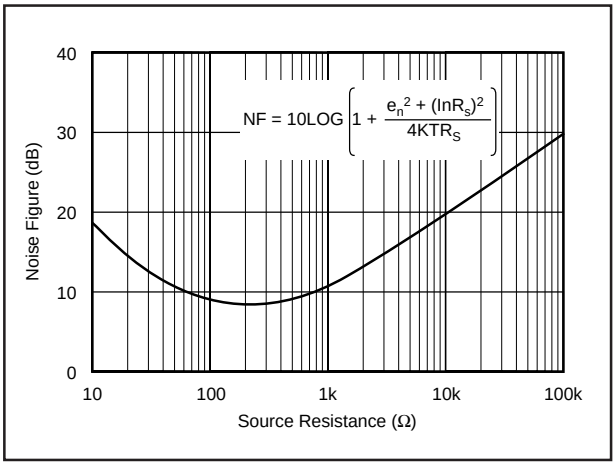


FIGURE 9. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA4658. Evaluation PC boards are also available. Contract Burr-Brown applications departments to receive a SPICE Diskette.

DEMONSTRATION BOARD	PACKAGE	PRODUCT
DEM-OPA465xP	8-Pin DIP	OPA4658P
DEM-OPA465xU	SO-8	OPA4658U OPA4658UB

TYPICAL APPLICATIONS

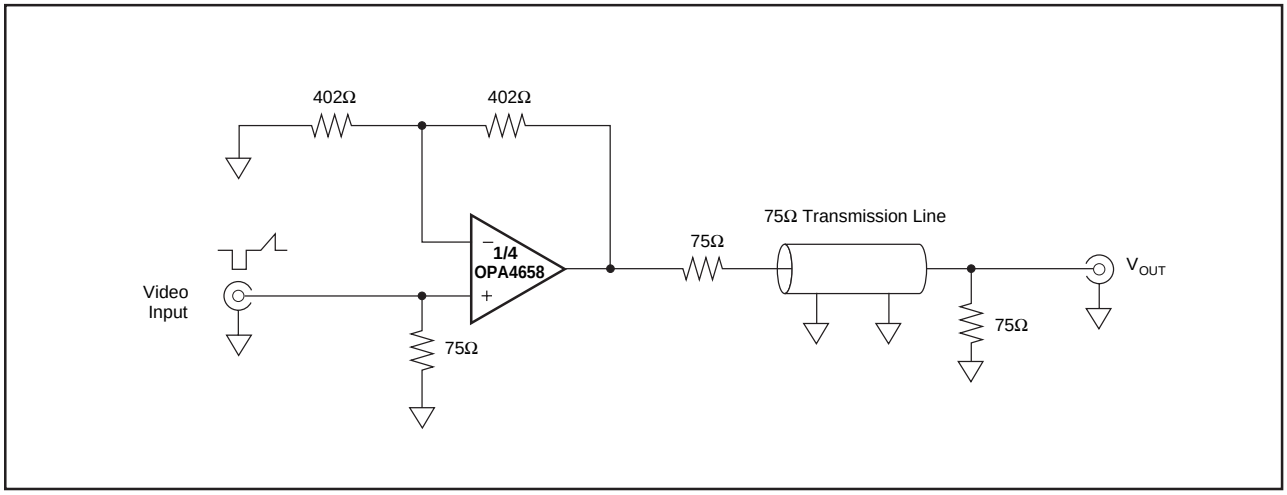


FIGURE 10. Low Distortion Video Amplifier.

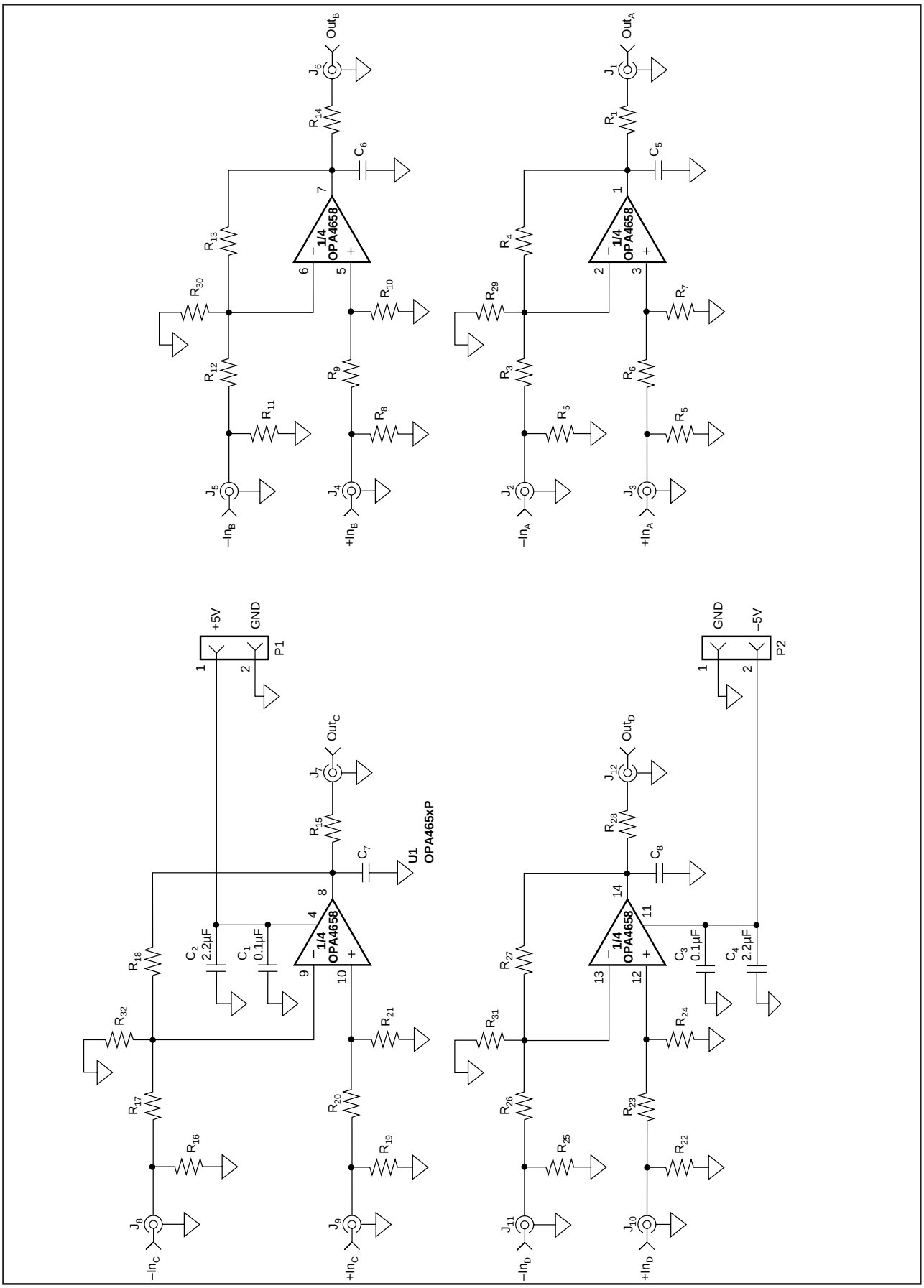
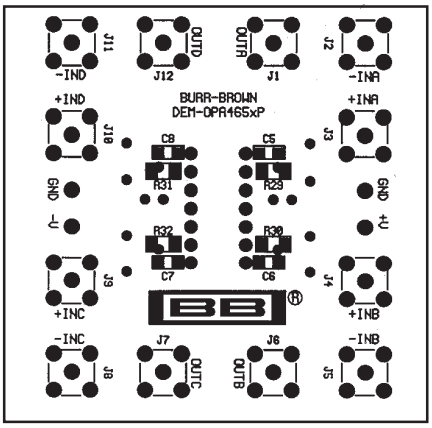
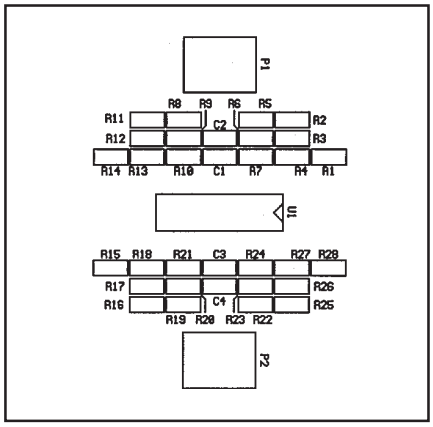


FIGURE 11. Circuit Detail for the PC Board Layout of Figure 12.

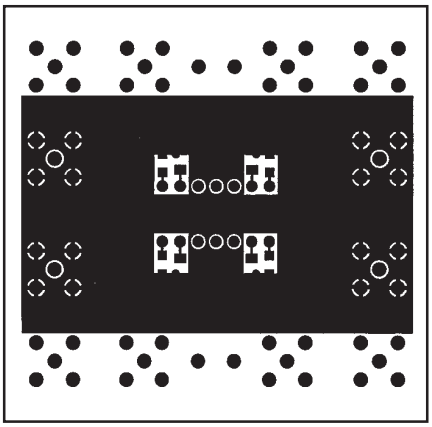
DEM-OPA465xP Demonstration Board Layout



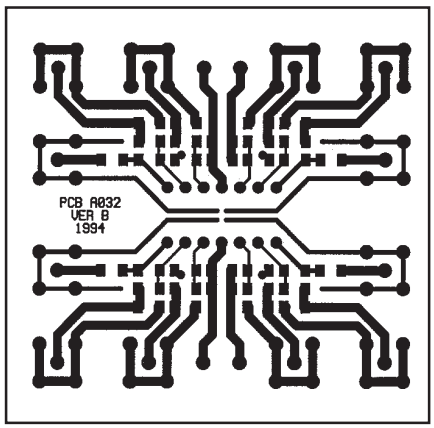
(A)



(B)



(C)



(D)

FIGURE 12a. Board Silkscreen (Bottom). 12b. Board Silkscreen (Top). 12c. Board Layout (Solder Side). 12d. Board Layout (Component Side).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA4658P	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
OPA4658U	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
OPA4658U/2K5	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265