## RENESAS Low Skew, 1-to-2, Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer

# ICS853S011CI

### DATA SHEET

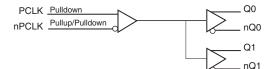
### **General Description**

The ICS853S011CI is a low skew, high performance 1-to-2 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer. The ICS853S011CI is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853S011CI ideal for those clock distribution applications demanding well defined performance and repeatability.

### **Features**

- Two differential 2.5V, 3.3V LVPECL/ECL outputs
- One differential PCLK, nPCLK input pair
- PCLK, nPCLK pairs can accept the following • differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: >2.5GHz
- ٠ Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Output skew: 20ps (maximum)
- Part-to-part skew: 150ps (maximum) ٠
- Propagation delay: 330ps (maximum)
- LVPECL mode operating voltage supply range:  $V_{CC} = 2.375V$  to 3.8V,  $V_{EE} = 0V$
- ECL mode operating voltage supply range:  $V_{CC}$  = 0V,  $V_{EE}$  = -3.8V to -2.375V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

### Block Diagram



### Pin Assignment

Q0 🗖 1	8 🗆 Vcc
nQ0 🗖 2	7 🗖 PCLK
Q1 🗖 3	6 🗖 nPCLK
nQ1 🛛 4	5 🗖 Vee

#### ICS853S011CI

8-Lead SOIC, 150MIL 3.90mm x 4.90mm x 1.37mm package body M Package **Top View** 

8-Lead TSSOP, 118MIL 3.0mm x 3.0mm x 0.97mm package body **G** Package **Top View** 

### **Pin Description and Pin Characteristic Tables**

#### Table 1. Pin Descriptions

Number	Name	Т	уре	Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL/ECL interface levels.
5	V <sub>EE</sub>	Power		Negative supply pin.
6	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. When left floating, defaults to $^{2}$ / $_{3}$ V <sub>CC</sub> .
7	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
8	V <sub>CC</sub>	Power		Positive supply pin.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

#### Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			75		kΩ
R <sub>PULLUP</sub>	Pullup Resistors			37		kΩ

## **Absolute Maximum Ratings**

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating	
Supply Voltage, V <sub>CC</sub>	4.6V (LVPECL mode, V <sub>EE</sub> = 0V)	
Negative Supply Voltage, V <sub>EE</sub>	-4.6V (ECL mode, V <sub>CC</sub> = 0V)	
Inputs, V <sub>I</sub> (LVPECL mode)	-0.5V to V <sub>CC</sub> + 0.5V	
Inputs, V <sub>I</sub> (ECL mode)	0.5V to V <sub>EE</sub> – 0.5V	
Outputs, I <sub>O</sub> Continuos Current Surge Current	50mA 100mA	
Operating Temperature Range, T <sub>A</sub>	-40°C to +85°C	
Package Thermal Impedance, $\theta_{JA}$ (Junction-to-Ambient) for 8 Lead SOIC	102°C/W (0 mps)	
Package Thermal Impedance, θ <sub>JA</sub> (Junction-to-Ambient) for 8 Lead TSSOP	145.4°C/W (0 mps)	
Storage Temperature, T <sub>STG</sub>	-65°C to 150°C	

### **DC Electrical Characteristics**

Table 3A. Power Supply DC Characteristics,  $V_{CC} = 2.375V$  to 3.8V;  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>CC</sub>	Positive Supply Voltage		2.375	3.3	3.8	V
I <sub>EE</sub>	Power Supply Current				24	mA

#### Table 3B. LVPECL DC Characteristics, $V_{CC} = 3.3V$ ; $V_{EE} = 0V$ , $T_A = -40^{\circ}C$ to $85^{\circ}C$

				-40°C			25°C			85°C		
Symbol	Parameter		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Units
V <sub>OH</sub>	Output High Voltage; NOTE 1		2.2575	2.36	2.4625	2.2275	2.33	2.4325	2.2075	2.31	2.4125	V
V <sub>OL</sub>	Output Low Voltage; NOTE 1		1.405	1.54	1.6775	1.3725	1.51	1.6475	1.3625	1.50	1.6375	V
V <sub>PP</sub>	Peak-to-Peak NOTE 2	Input Voltage;	150	800	1200	150	800	1200	150	800	1200	mV
V <sub>CMR</sub>	Input High Vol Mode Range;		1.2		3.3	1.2		3.3	1.2		3.3	V
I <sub>IH</sub>	Input High Current	PCLK, nPCLK			200			200			200	μA
	Input	PCLK	-10			-10			-10			μA
۱	Low Current	nPCLK	-200			-200			-200			μA

NOTE: Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50  $\Omega$  to V\_{CC} – 2V.

NOTE 2:  $V_{IL}$  should not be less than -0.3V.

NOTE 3: Common mode voltage is defined as V<sub>IH</sub>.

			-40°C		25°C 85°C							
Symbol	Parameter		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Units
V <sub>OH</sub>	Output High Voltage; NOTE 1		1.4675	1.57	1.6725	1.4475	1.55	1.6525	1.4375	1.54	1.6425	V
V <sub>OL</sub>	Output Low Vo	oltage; NOTE 1	0.6265	0.76	0.9015	0.6125	0.75	0.8875	0.6025	0.74	0.8775	V
V <sub>PP</sub>	Peak-to-Peak NOTE 2	Input Voltage;	150	800	1200	150	800	1200	150	800	1200	mV
V <sub>CMR</sub>	Input High Vol Mode Range;		1.2		2.5	1.2		2.5	1.2		2.5	V
IIH	Input High Current	PCLK, nPCLK			200			200			200	μA
	Input	PCLK	-10			-10			-10			μA
ιL	Low Current	nPCLK	-200			-200			-200			μA

#### Table 3C. LVPECL DC Characteristics, V\_{CC} = 2.5V; V\_{EE} = 0V, T\_A = -40^{\circ}C to $85^{\circ}C$

NOTE: Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50  $\Omega$  to V\_CC – 2V.

NOTE 2:  $V_{IL}$  should not be less than -0.3V.

NOTE 3: Common mode voltage is defined as VIH.

#### Table 3D. ECL DC Characteristics, $V_{CC} = 0V$ ; $V_{EE} = -3.8V$ to -2.375V, $T_A = -40^{\circ}C$ to $85^{\circ}C$

				-40°C			25°C			85°C		
Symbol	Parameter		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Units
V <sub>OH</sub>	Output High V	oltage; NOTE 1	-1.0425	-0.94	-0.8375	-1.0725	-0.8675	-0.97	-1.0925	-0.8875	-0.99	V
V <sub>OL</sub>	Output Low Vo	oltage; NOTE 1	-1.8975	-1.76	-1.6225	-1.9275	-1.79	-1.6525	-1.9375	-1.80	-1.6625	V
V <sub>PP</sub>	Peak-to-Peak NOTE 2	Input Voltage;	150	800	1200	150	800	1200	150	800	1200	mV
V <sub>CMR</sub>	Input High Vol Mode Range;	tage Common NOTE 2, 3	V <sub>EE</sub> +1.2		0	V <sub>EE</sub> +1.2		0	V <sub>EE</sub> +1.2		0	V
I <sub>IH</sub>	Input High Current	PCLK, nPCLK			200			200			200	μA
	Input	PCLK	-10			-10			-10			μA
۱L	Low Current	nPCLK	-200			-200			-200			μA

NOTE: Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.925V to -0.5V. NOTE 1: Outputs terminated with 50 $\Omega$  to V<sub>CC</sub> – 2V.

NOTE 2:  $V_{IL}$  should not be less than -0.3V.

NOTE 3: Common mode voltage is defined as  $V_{IH}$ .

### **AC Electrical Characteristics**

Table 4. AC Characteristics,  $V_{CC}$  = -3.8V to -2.375V or ,  $V_{CC}$  = 2.375V to 3.8V;  $V_{EE}$  = 0V,  $T_A$  = -40°C to 85°C

				-40°C		25°C		85°C				
Symbol	Parameter		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Units
f <sub>MAX</sub>	Output Frequence	су			>2.5			>2.5			>2.5	GHz
t <sub>PD</sub>	Propagation Del	ay; NOTE 1	170		320	180		330	190		345	ps
<i>t</i> sk(o)	Output Skew; No	OTE 2, 4			20			20			20	ps
<i>t</i> sk(pp)	Part-to-Part Ske	w; NOTE 3, 4			150			150			150	ps
<i>t</i> jit	Buffer Additive F RMS; refer to Ac Jitter Section	,		0.035			0.035			0.035		ps
t <sub>R</sub> / t <sub>F</sub>	Output Rise/Fall Time	20% to 80%	50		200	50		200	50		200	ps
odc	Output Duty Cyc	le	48		52	48		52	48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters are measured at  $f \leq 1.4 GHz,$  unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

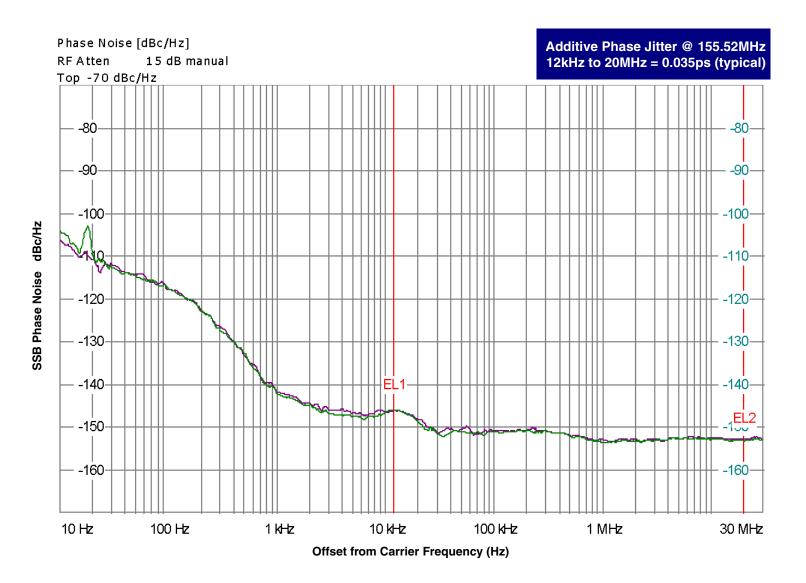
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

## **Additive Phase Jitter**

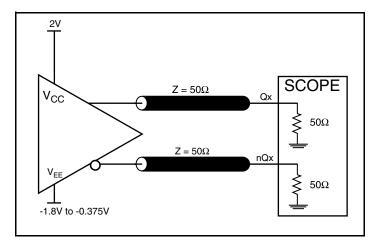
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

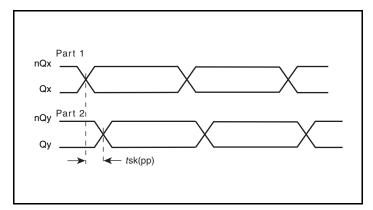


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

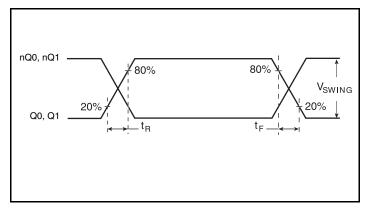
### **Parameter Measurement Information**



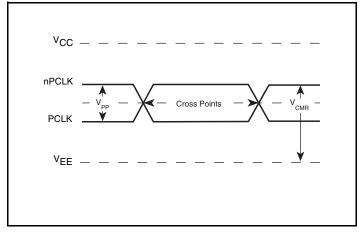
LVPECL Output Load Test Circuit



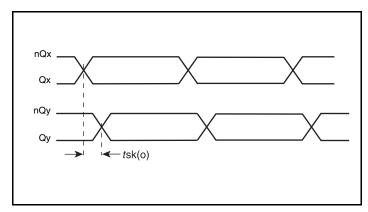
Part-to-Part Skew



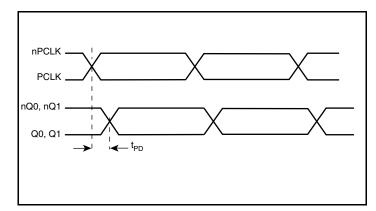
**Output Rise/Fall Time** 



Differential Input Level

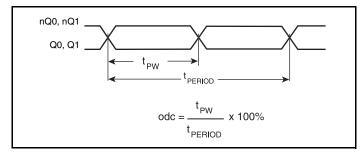


**Output Skew** 





## Parameter Measurement Information, continued



**Output Duty Cycle/Pulse Width/Period** 

### **Application Information**

#### **Recommendations for Unused Output Pins**

#### **Outputs:**

#### **LVPECL Outputs**

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V<sub>1</sub> in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V<sub>CC</sub> = 3.3V, R1 and R2 value should be adjusted to set V<sub>1</sub> at 1.25V. The values below are for when both the single ended swing and V<sub>CC</sub> are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V<sub>IL</sub> cannot be less than -0.3V and V<sub>IH</sub> cannot be more than V<sub>CC</sub> + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

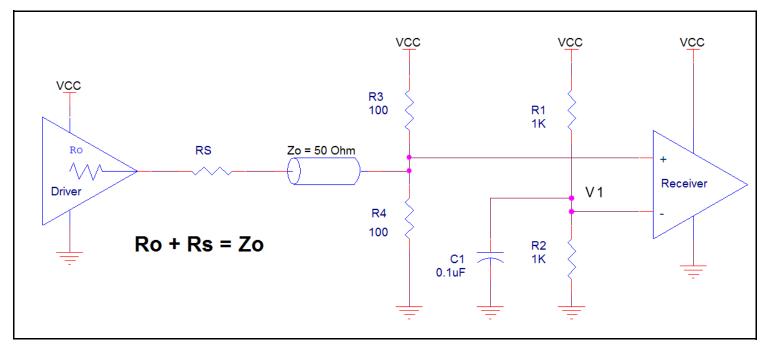


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

### LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both V<sub>SWING</sub> and V<sub>OH</sub> must meet the V<sub>PP</sub> and V<sub>CMR</sub> input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

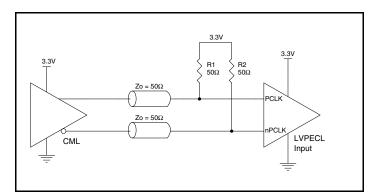


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

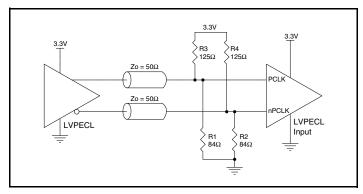


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

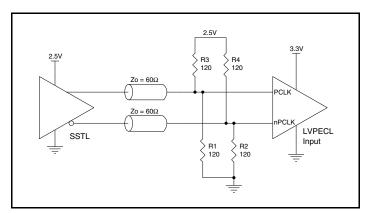


Figure 2E.PCLK/nPCLK Input Driven by an SSTL Driver

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

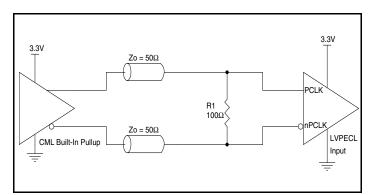


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

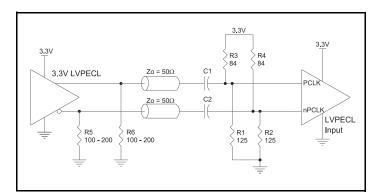


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

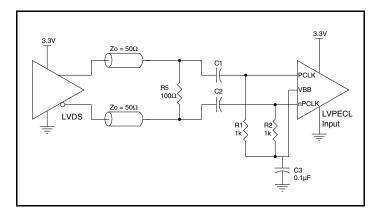


Figure 2F. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

### **Termination for 3.3V LVPECL Outputs**

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive  $50\Omega$ 

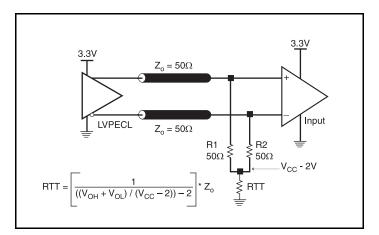


Figure 3A. 3.3V LVPECL Output Termination

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

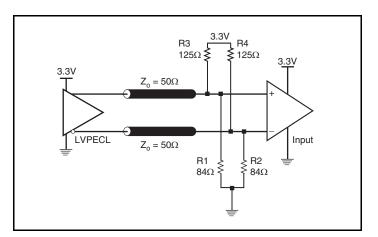


Figure 3B. 3.3V LVPECL Output Termination

### **Termination for 2.5V LVPECL Outputs**

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to V<sub>CC</sub> – 2V. For V<sub>CC</sub> = 2.5V, the V<sub>CC</sub> – 2V is very close to ground

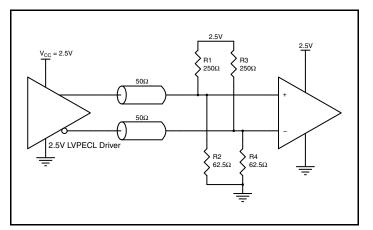


Figure 4A. 2.5V LVPECL Driver Termination Example

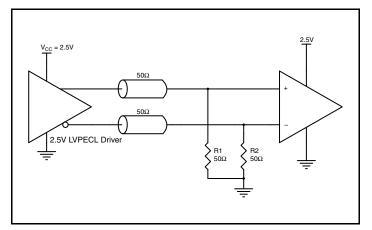


Figure 4C. 2.5V LVPECL Driver Termination Example

level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C*.

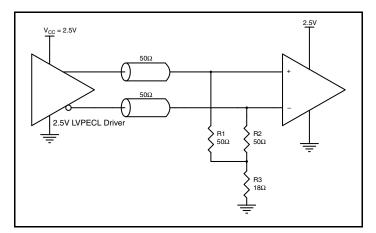


Figure 4B. 2.5V LVPECL Driver Termination Example

### **Power Considerations**

This section provides information on power dissipation and junction temperature for the ICS853S011CI. Equations and example calculations are also provided.

#### 1. Power Dissipation.

The total power dissipation for the ICS853S011CI is the sum of the core power plus the power dissipation due to loading. The following is the power dissipation for  $V_{CC} = 3.8V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation due to loading.

- Power (core)<sub>MAX</sub> = V<sub>CC MAX</sub> \* I<sub>EE MAX</sub> = 3.8V \* 24mA = 91.2mW
- Power (outputs)<sub>MAX</sub> = 31.22mW/Loaded Output pair If all outputs are loaded, the total power is 2 \* 31.22mW = 62.44mW

Total Power\_MAX (3.8V, with all outputs switching) = 91.2mW + 62.44mW = 153.64mW

#### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj =  $\theta_{JA}$  \* Pd\_total + T<sub>A</sub>

Tj = Junction Temperature

 $\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd\_total = Total Device Power Dissipation (example calculation is in section 1 above)

 $T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 145.4°C/W per Table 5A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

 $85^{\circ}C + 0.154W * 145.4^{\circ}C/W = 107.4^{\circ}C$ . This is below the limit of  $125^{\circ}C$ .

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

#### Table 5A. Thermal Resistance $\theta_{\text{JA}}$ for 8 Lead TSSOP, Forced Convection

θ <sub>JA</sub> by Velocity								
Meters per Second	0	1	2.5					
Multi-Layer PCB, JEDEC Standard Test Boards	145.4°C/W	141.3°C/W	139.3°C/W					

#### Table 5B. Thermal Resistance $\theta_{\text{JA}}$ for 8 Lead SOIC, Forced Convection

$\theta_{JA}$ by Velocity								
Meters per Second	0	1	2.5					
Multi-Layer PCB, JEDEC Standard Test Boards	102.0°C/W	95.0°C/W	90.6°C/W					

#### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in Figure 5.

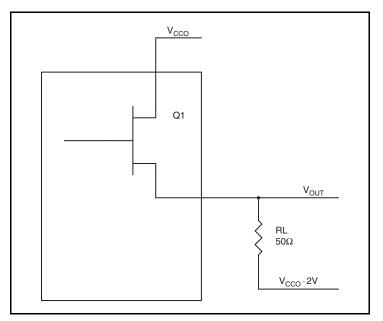


Figure 5. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50 $\Omega$  load, and a termination voltage of V<sub>CC</sub> – 2V.

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} 0.99V$ ( $V_{CC\_MAX} - V_{OH\_MAX}$ ) = 0.99V
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} 1.6625V$ ( $V_{CC\_MAX} - V_{OL\_MAX}$ ) = 1.6625V

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

 $\mathsf{Pd}_{-}\mathsf{H} = [(\mathsf{V}_{\mathsf{OH}\_\mathsf{MAX}} - (\mathsf{V}_{\mathsf{CCO}\_\mathsf{MAX}} - 2\mathsf{V}))/\mathsf{R}_{\mathsf{L}}] * (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OH}\_\mathsf{MAX}}) = [(2\mathsf{V} - (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OH}\_\mathsf{MAX}}))/\mathsf{R}_{\mathsf{L}}] * (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OH}\_\mathsf{MAX}}) = [(2\mathsf{V} - 0.99\mathsf{V})/50\Omega] * 0.99\mathsf{V} = \mathbf{20}\mathsf{mW}$ 

 $\begin{array}{l} \mathsf{Pd}_{\mathsf{L}} = [(\mathsf{V}_{\mathsf{OL}\_\mathsf{MAX}} - (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - 2\mathsf{V}))/\mathsf{R}_{\mathsf{L}}] * (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OL}\_\mathsf{MAX}}) = [(2\mathsf{V} - (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OL}\_\mathsf{MAX}}))/\mathsf{R}_{\mathsf{L}}] * (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OL}\_\mathsf{MAX}}) = [(2\mathsf{V} - 1.6625\mathsf{V})/50\Omega] * 1.6625\mathsf{V} = 11.22\mathsf{mW} \end{array}$ 

Total Power Dissipation per output pair = Pd\_H + Pd\_L = **31.22mW** 

### **Reliability Information**

### Table 6A. $\theta_{\text{JA}}$ vs. Air Flow Table for a 8 Lead SOIC

$\theta_{JA}$ vs. Air Flow								
Meters per Second	0	1	2.5					
Multi-Layer PCB, JEDEC Standard Test Boards	102.0°C/W	95.0°C/W	90.6°C/W					

#### Table 6B. $\theta_{\text{JA}}$ vs. Air Flow Table for a 8 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	145.4°C/W	141.3°C/W	139.3°C/W

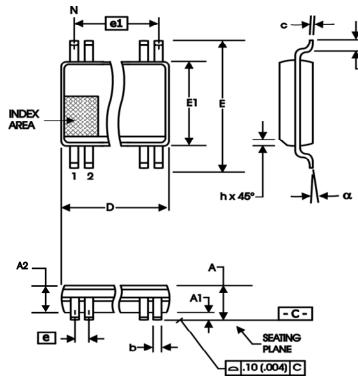
#### Transistor Count

The transistor count for ICS853S011CI is: 208

This device is pin compatible with and is the suggested replacement for the ICS853011B and ICS853011C.

## Package Outlines and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP



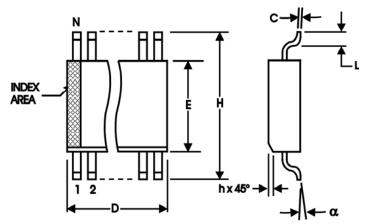
#### Table 7A. Package Dimensions

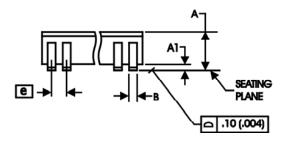
All Dimensions in Millimeters				
Symbol	Minimum Maximum			
N	8			
Α	1.10			
A1	0	0.15		
A2	0.79	0.97		
b	0.22	0.38		
С	0.08	0.23		
D	3.00 Basic			
E	4.90 Basic			
E1	3.00 Basic			
е	0.65 Basic			
e1	1.95 Basic			
L	0.40	0.80		
α	0°	8°		
aaa	0.10			

Reference Document: JEDEC Publication 95, MO-187

Package Outline - M Suffix for 8 Lead SOIC

ı.





#### Table 7B. Package Dimensions

All Dimensions in Millimeters				
Symbol	Symbol Minimum Maxim			
N		8		
Α	1.35	1.75		
A1	0.10	0.25		
В	0.33	0.51		
С	0.19	0.25		
D	4.80	5.00		
E	3.80	4.00		
е	1.27 Basic			
Н	5.80	6.20		
h	0.25	0.50		
L	0.40	1.27		
α	0°	<b>8</b> °		

Reference Document: JEDEC Publication 95, MS-012

## **Ordering Information**

### Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S011CMILF	3S011CIL	"Lead Free" 8 Lead SOIC	Tube	-40°C to 85°C
853S011CMILFT	3S011CIL	"Lead Free" 8 Lead SOIC	Tape & Reel	-40°C to 85°C
853S011CGILF	1CIL	"Lead Free" 8 Lead TSSOP	Tube	-40°C to 85°C
853S011CGILFT	1CIL	"Lead Free" 8 Lead TSSOP	Tape & Reel	-40°C to 85°C

Revision	History	Sheet

Rev	Table	Page	Description of Change	Date
А		9 10	Updated Wiring the Differential Input to Accept Single-ended Levels section. Updated LVPECL Clock Input Interface section.	6/7/10
A	T3B - T3C T3D T4	4 5 5	LVPECL DC Characteristics Tables - corrected heading from 80°C to 85°C. ECL DC Characteristics Table - corrected heading from 80°C to 85°C. AC Characteristics Tables - corrected heading from 80°C to 85°C.	10/12/10
A	T3B:T3B T3C	3 4 9 17	<ul> <li>3 LVPECL DC Characteristics Tables - corrected V<sub>pp</sub> unit from "V" to "mV".</li> <li>4 ECL DC Characteristics Table - corrected V<sub>pp</sub> unit from "V" to "mV".</li> <li>9 Updated application note <i>Wiring the Differential Levels to Accept Singe-ended Levels.</i></li> </ul>	



#### IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

#### **Corporate Headquarters**

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

#### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

#### **Contact Information**

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit <u>www.renesas.com/contact-us/</u>.