HARRIS SEMICONDUCTOR

# HFA-0005

## High Slew Rate Operational Amplifier

March 1993



## Features

- **Unity Gain Bandwidth .................... 300MHz**
- **Full Power Bandwidth .................... 22MHz**
- **High Slew Rate .......................... 420V/µs**
- **High Output Drive ....................... ±50mA**
- **Monolithic Bipolar Construction**

## Applications

- **RF/IF Processors**
- **Video Amplifiers**
- **Radar Systems**
- **Pulse Amplifiers**
- **High Speed Communications**
- **Fast Data Acquisition Systems**

## Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| HFA2-0005-5 | 0°C to +75°C | 8 Pin Can |
| HFA2-0005-9 | -40°C to +85°C | 8 Pin Can |
| HFA3-0005-5 | 0°C to +75°C | 8 Lead Plastic DIP |
| HFA3-0005-9 | -40°C to +85°C | 8 Lead Plastic DIP |
| HFA7-0005-5 | 0°C to +75°C | 8 Lead Ceramic Sidebraze DIP |
| HFA7-0005-9 | -40°C to +85°C | 8 Lead Ceramic Sidebraze DIP |
| HFA9P0005-5 | 0°C to +75°C | 8 Lead SOIC |
| HFA9P0005-9 | -40°C to +85°C | 8 Lead SOIC |

## Description

The HFA-0005 is an all bipolar op amp featuring high slew rate (420V/µs), and high unity gain bandwidth (300MHz). These features combined with fast settling time (20ns) make this product very useful in high speed data acquisition systems as well as RF, video, and pulse amplifier designs.

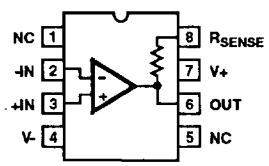
Other outstanding characteristics include low bias currents (15µA), low offset current (6µA), and low offset voltage (6mV). These high performance characteristics are achieved with only 40mA of supply current.

The HFA-0005 offers high performance at low cost. It can replace hybrids and RF transistor amplifiers, simplifying designs while providing increased reliability due to monolithic construction. To enhance the ease of design, the HFA-0005 has a 50Ω ±20% resistor connected from the output of the op amp to a separate pin. This can be used when driving 50Ω strip line, microstrip, or coax cable.

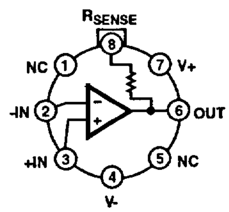
For MIL-STD-883 compliant product consult the HFA-0005/883 datasheet.

## Pinouts

**HFA-0005 (PDIP, CDIP, SOIC)**
TOP VIEW




**HFA-0005 (TO-99 METAL CAN)**
TOP VIEW




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.



File Number **2918.1**

## Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals .................... 12V
Differential Input Voltage ................................ 5V
Input Voltage ........................................... ±4V
Output Current ........................................ ±60mA
Junction Temperature ............................... +175°C
Junction Temperature (Plastic Packages) ............... +150°C
Lead Temperature (Soldering 10 Sec.) .................. 300°C

## Operating Conditions

Operating Temperature Range
HFA-0005-9 .......................... -40°C ≤ $T_A$ ≤ +85°C
HFA-0005-5 ............................ 0°C ≤ $T_A$ ≤ +75°C
Storage Temperature Range .............. -65°C ≤ $T_A$ ≤ +150°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified

| PARAMETERS | TEMP | HFA-0005-9 | | | HFA-0005-5 | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| INPUT CHARACTERISTICS | | | | | | | | |
| Offset Voltage | +25°C | - | 6 | 15 | - | 6 | 30 | mV |
| | Full | - | 11 | 45 | - | 11 | 35 | mV |
| Average Offset Voltage Drift | Full | - | 100 | - | - | 100 | - | µV/°C |
| Bias Current | +25°C | - | 15 | 50 | - | 15 | 100 | µA |
| | Full | - | 20 | 50 | - | 20 | 100 | µA |
| Offset Current | +25°C | - | 6 | 25 | - | 6 | 50 | µA |
| | Full | - | 12 | 50 | - | 12 | 50 | µA |
| Common Mode Range | Full | ±3 | - | - | ±3 | - | - | V |
| Differential Input Resistance | +25°C | - | 10 | - | - | 10 | - | kΩ |
| Input Capacitance | +25°C | - | 2 | - | - | 2 | - | pF |
| Input Noise Voltage | | | | | | | | |
| 0.1Hz to 10Hz | +25°C | - | 2.5 | - | - | 2.5 | - | $\mu V_{RMS}$ |
| 10Hz to 1MHz | +25°C | - | 5.8 | - | - | 5.8 | - | $\mu V_{RMS}$ |
| Input Noise Voltage | | | | | | | | |
| $f_O$ = 10Hz | +25°C | - | 450 | - | - | 450 | - | $nV/\sqrt{Hz}$ |
| $f_O$ = 100Hz | +25°C | - | 160 | - | - | 160 | - | $nV/\sqrt{Hz}$ |
| $f_O$ = 100kHz | +25°C | - | 5 | - | - | 5 | - | $nV/\sqrt{Hz}$ |
| Input Noise Current | | | | | | | | |
| $f_O$ = 10Hz | +25°C | - | 2.0 | - | - | 2.0 | - | $nA/\sqrt{Hz}$ |
| $f_O$ = 100Hz | +25°C | - | 0.57 | - | - | 0.57 | - | $nA/\sqrt{Hz}$ |
| $f_O$ = 1000Hz | +25°C | - | 0.11 | - | - | 0.11 | - | $nA/\sqrt{Hz}$ |
| TRANSFER CHARACTERISTICS | | | | | | | | |
| Large Signal Voltage Gain (Note 2) | +25°C | 150 | 230 | - | 150 | 230 | - | V/V |
| | High | 150 | 180 | - | 150 | 180 | - | V/V |
| | Low | 150 | 250 | - | 150 | 250 | - | V/V |
| Common Mode Rejection Ratio (Note 3) | Full | 45 | 47 | - | 42 | 45 | - | dB |
| Unity Gain Bandwidth | +25°C | - | 300 | - | - | 300 | - | MHz |
| Minimum Stable Gain | Full | 1 | - | - | 1 | - | - | V/V |
| OUTPUT CHARACTERISTICS | | | | | | | | |
| Output Voltage Swing | | | | | | | | |
| $R_L$ = 100Ω | +25°C | - | ±3.5 | - | - | ±3.5 | - | V |
| $R_L$ = 1kΩ | Full | ±3.5 | ±4.0 | - | ±3.5 | ±4.0 | - | V |
| Full Power Bandwidth (Note 5) | +25°C | - | 22 | - | - | 22 | - | MHz |
| Output Resistance, Open Loop | +25°C | - | 3.0 | - | - | 3.0 | - | Ω |
| Output Current | Full | ±25 | ±50 | - | ±25 | ±50 | - | mA |

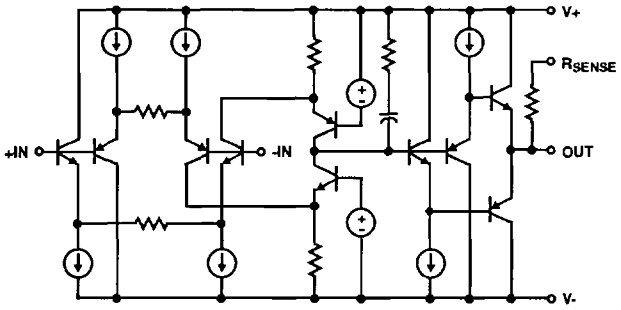
**Electrical Specifications** V+ = +5V, V- = -5V, Unless Otherwise Specified **(Continued)**

| PARAMETERS | TEMP | HFA-0005-9 | | | HFA-0005-5 | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| TRANSIENT RESPONSE | | | | | | | | |
| Rise Time (Note 4, 6) | +25°C | - | 480 | - | - | 480 | - | ps |
| Slew Rate (Note 7) | +25°C | - | 420 | - | - | 420 | - | V/µs |
| Settling Time (3V Step) 0.1% | +25°C | - | 20 | - | - | 20 | - | ns |
| Overshoot (Note 4, 6) | +25°C | - | 30 | - | - | 30 | - | % |
| POWER SUPPLY CHARACTERISTICS | | | | | | | | |
| Supply Current | +25°C | - | 35 | 40 | - | 35 | 40 | mA |
| | Full | - | 37 | 40 | - | 37 | 45 | mA |
| Power Supply Rejection Ratio (Note 8) | +25°C | 40 | 42 | - | 37 | 40 | - | dB |

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. $V_{OUT}$ = 0 to ±2V, $R_L$ = 1kΩ.
3. $\Delta V_{CM}$ = ±2V.
4. $R_L$ = 100Ω.
5. Full Power Bandwidth is calculated by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}, V_{PEAK} = 3.0V$.
6. $V_{OUT}$ = ±200mV, $A_V$ = +1.
7. $V_{OUT}$ = ±3V, $A_V$ = +1.
8. $\Delta V_S$ = ±4V to ±6V.
9. See Thermal Constants in "Applications Information" section. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below +175°C for hermetic packages, and below +150°C for plastic packages.

## Simplified Schematic Diagram




## Die Characteristics

| Thermal Constants (°C/W) | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| CAN | 120 | 37 |
| PDIP | 98 | 36 |
| CDIP | 75 | 13 |
| SOIC | 158 | 43 |

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OPERATIONAL AMPLIFIERS

## Test Circuits

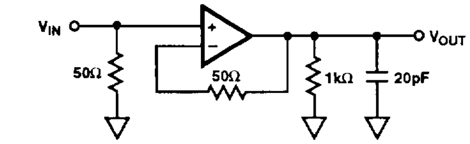



FIGURE 1. LARGE SIGNAL RESPONSE TEST CIRCUIT

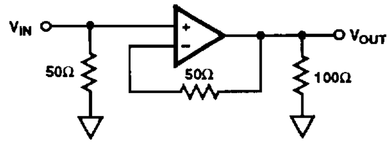
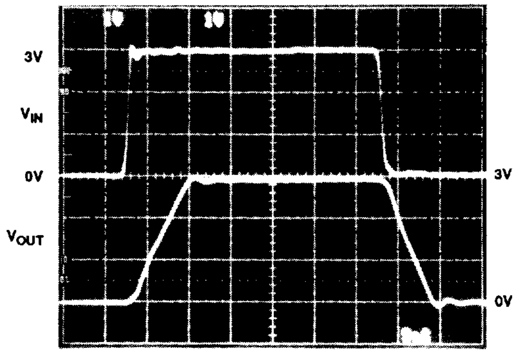
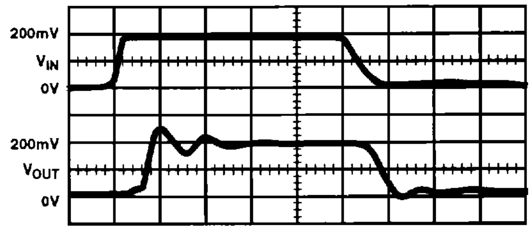



FIGURE 2. SMALL SIGNAL RESPONSE TEST CIRCUIT

**LARGE SIGNAL RESPONSE**
$V_{OUT}$ = 0 to 3V
Vertical Scale: 1V/Div. Horizontal Scale: 5ns/Div.

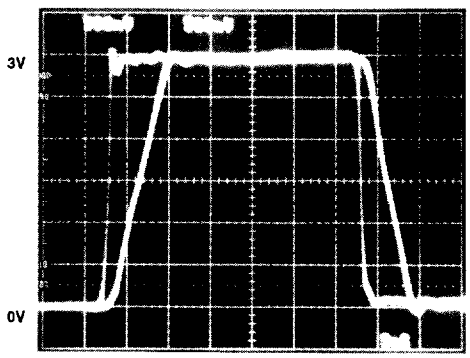



**SMALL SIGNAL RESPONSE**
$V_{OUT}$ = 0 to 200mV
Vertical Scale: 100mV/Div. Horizontal Scale: 2ns/Div.




NOTE: Initial step in output is due to fixture feedthrough

**PROPAGATION DELAY**
Vertical Scale: 500mV/Div. Horizontal Scale: 5ns/Div.
$A_V$ = +1, $R_L$ = 1kΩ, $V_{OUT}$ = 0 to 3V




NOTE: Test fixture delay of 450ps is included

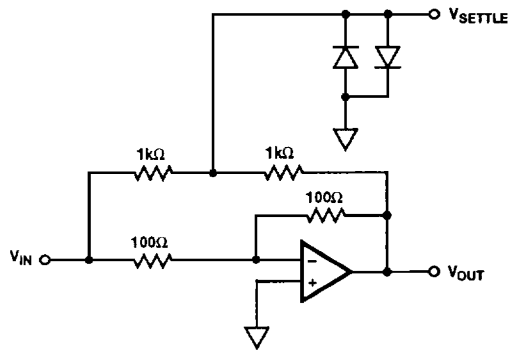



FIGURE 3. SETTLING TIME SCHEMATIC

## *Typical Performance Curves* $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified

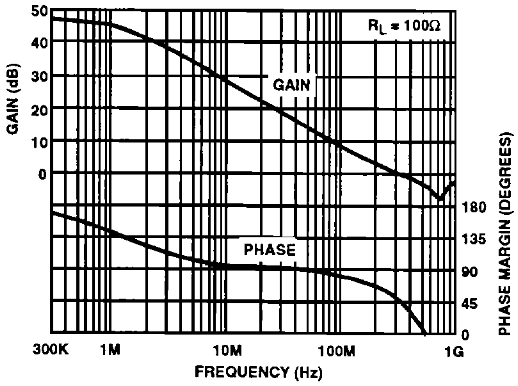



FIGURE 4. OPEN LOOP GAIN AND PHASE vs FREQUENCY

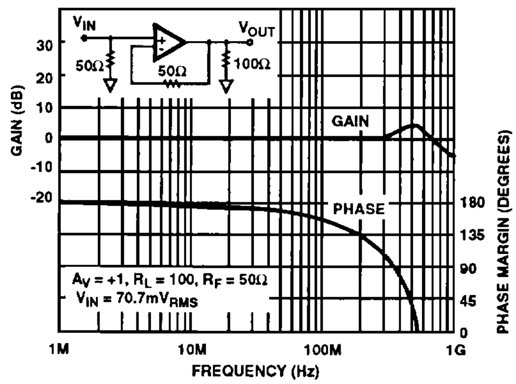



FIGURE 5. CLOSED LOOP GAIN vs FREQUENCY

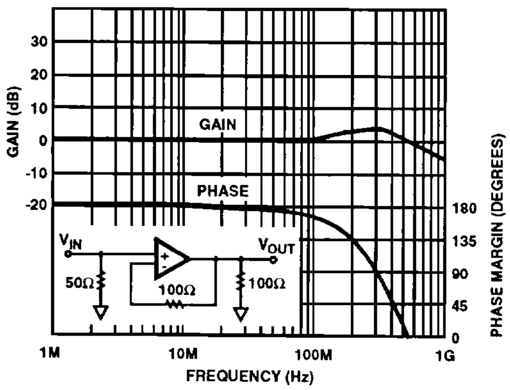



FIGURE 6. CLOSED LOOP GAIN vs FREQUENCY

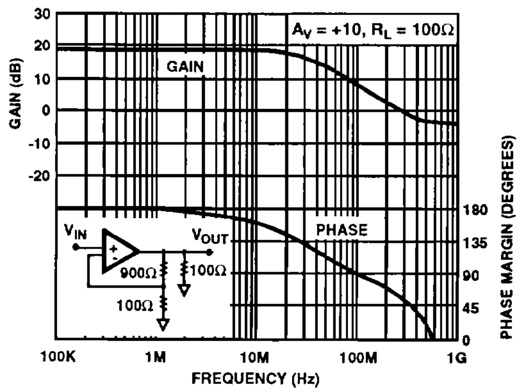



FIGURE 7. CLOSED LOOP GAIN vs FREQUENCY

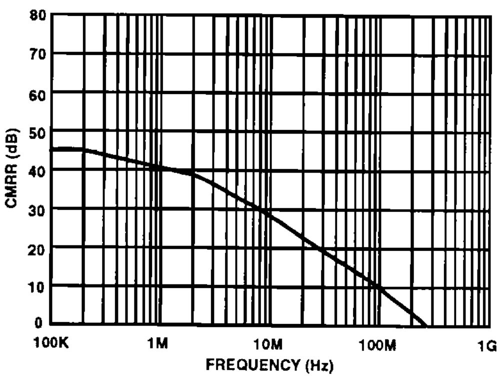



FIGURE 8. CMRR vs FREQUENCY

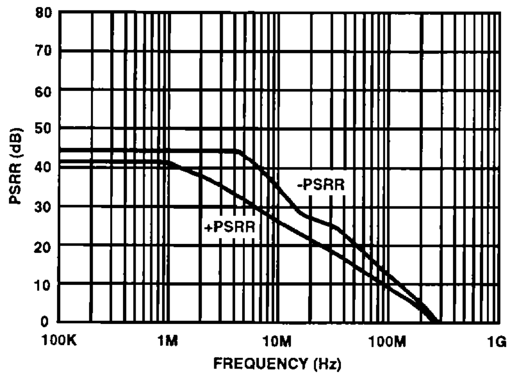



FIGURE 9. PSRR vs FREQUENCY

## *Typical Performance Curves* $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified **(Continued)**

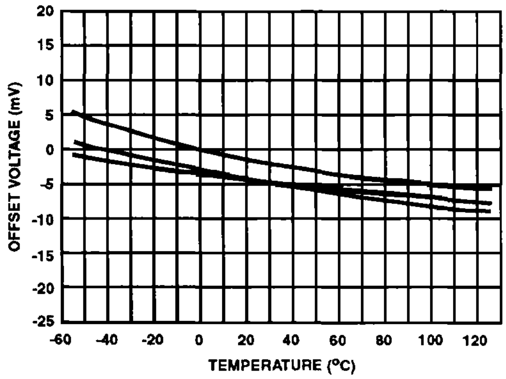



FIGURE 10. OFFSET VOLTAGE vs TEMPERATURE (3 REPRESENTATIVE UNITS)

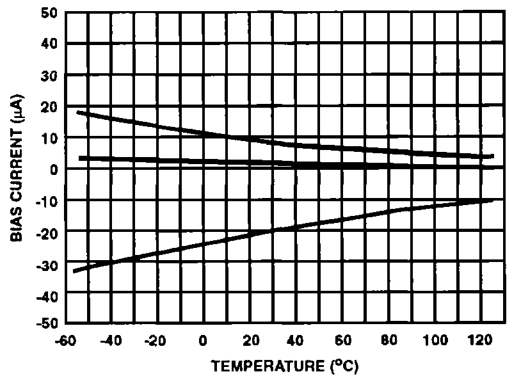



FIGURE 11. BIAS CURRENT vs TEMPERATURE (3 REPRESENTATIVE UNITS)

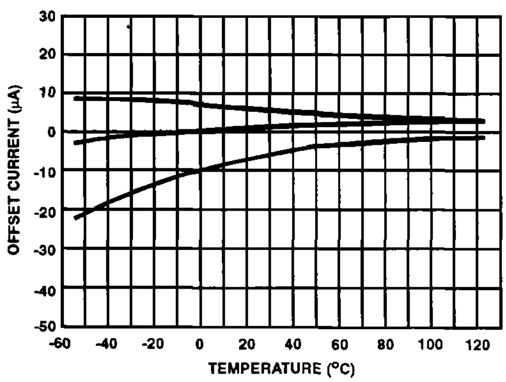



FIGURE 12. OFFSET CURRENT vs TEMPERATURE (3 REPRESENTATIVE UNITS)

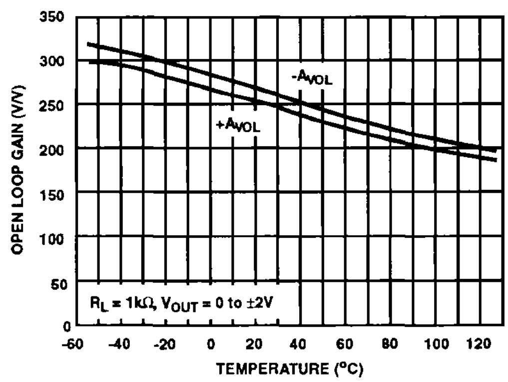



FIGURE 13. OPEN LOOP GAIN vs TEMPERATURE

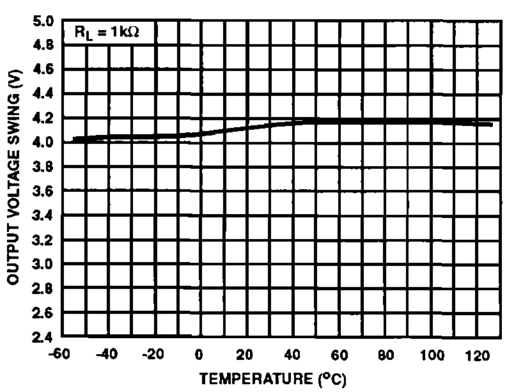



FIGURE 14. OUTPUT VOLTAGE SWING vs TEMPERATURE

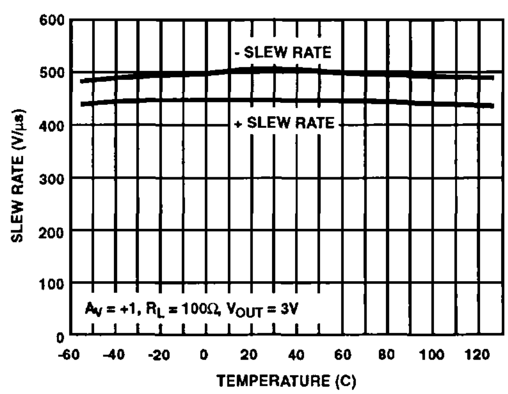



FIGURE 15. SLEW RATE vs TEMPERATURE

## *Typical Performance Curves* $V_S$ = ±5V, $T_A$ = +25°C, Unless Otherwise Specified **(Continued)**

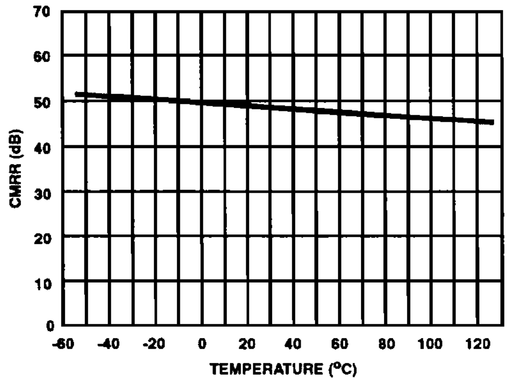



FIGURE 16. CMRR vs TEMPERATURE

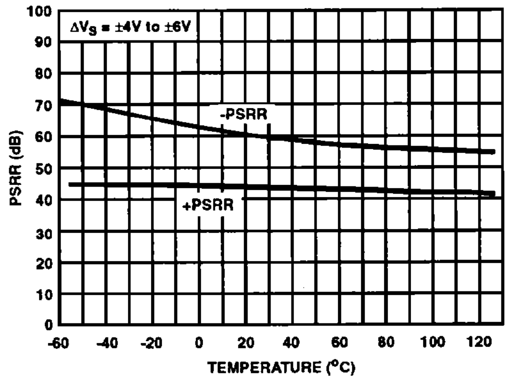



FIGURE 17. PSRR vs TEMPERATURE

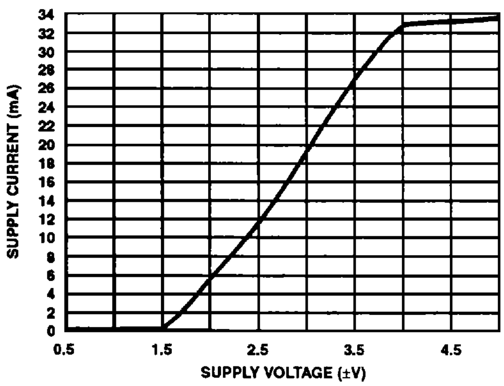



FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE

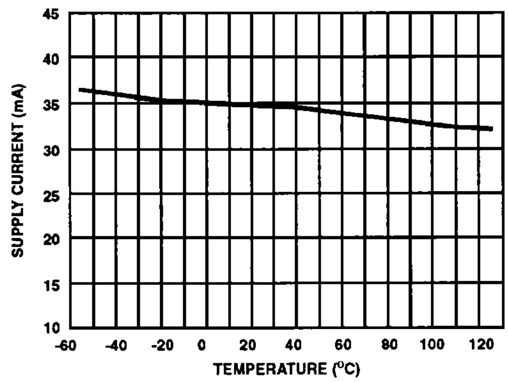



FIGURE 19. SUPPLY CURRENT vs TEMPERATURE

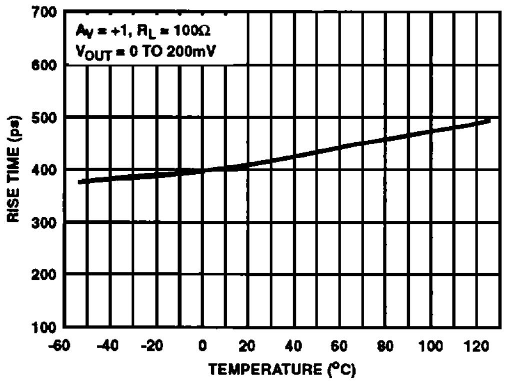



FIGURE 20. RISE TIME vs TEMPERATURE

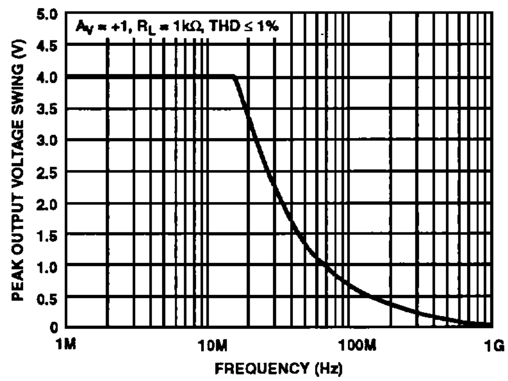



FIGURE 21. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

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## *Typical Performance Curves* $V_S = \pm 5V$, $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

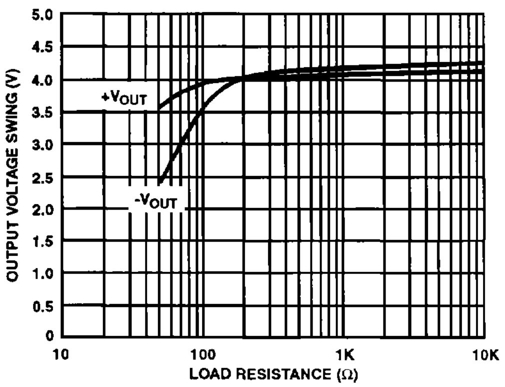



FIGURE 22. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

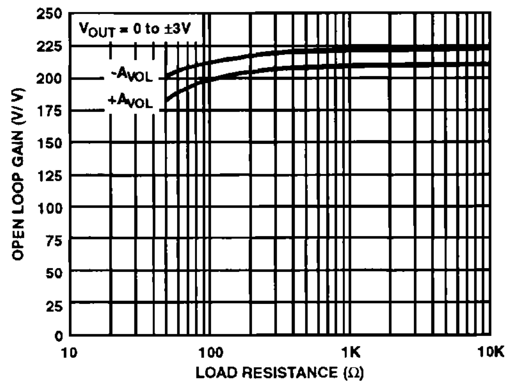



FIGURE 23. OPEN LOOP GAIN vs LOAD RESISTANCE

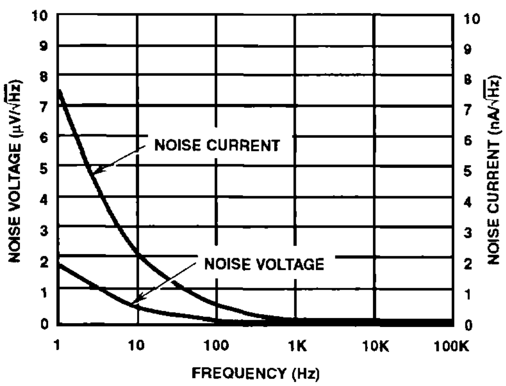



FIGURE 24. INPUT NOISE vs FREQUENCY

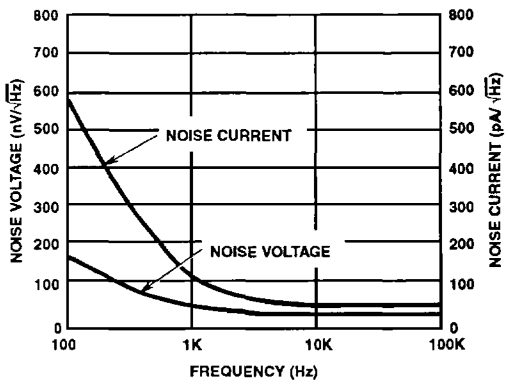



FIGURE 25. INPUT NOISE vs FREQUENCY

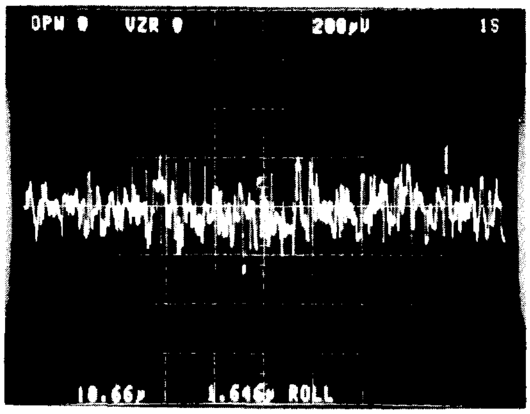



FIGURE 26. INPUT NOISE VOLTAGE
$A_V = 50$, Noise Voltage = $1.646\mu V_{RMS}$ (RTI)

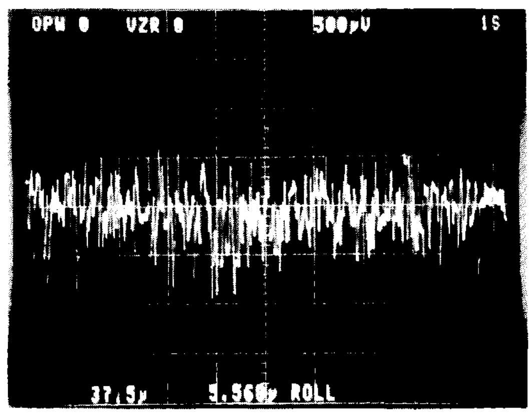
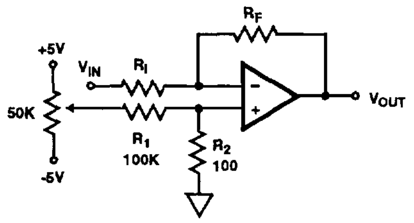



FIGURE 27. INPUT NOISE VOLTAGE
$A_V = 50$, Noise Voltage = $5.568\mu V_{RMS}$ (RTI)

## *Applications Information*

### Offset Adjustment

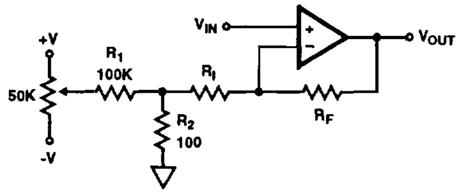
When applications require the offset voltage to be as low as possible, the figure below shows two possible schemes for adjusting offset voltage.




$$\text{Adjustment Range} \cong \pm V\left(\frac{R_2}{R_1}\right)$$

FIGURE 28. INVERTING GAIN

For a voltage follower application, use the circuit in Figure 29 without $R_2$ and with $R_I$ shorted. $R_1$ should then be 1MΩ to 10MΩ, so the adjustment resistors will cause only a very small gain error.




$$\text{Adjustment Range} \cong \pm V\left(\frac{R_2}{R_1}\right) \quad \text{Gain} \cong 1 + \left(\frac{R_F}{R_I + R_2}\right)$$

FIGURE 29. NON-INVERTING GAIN

### PC Board Layout Guidelines

When designing with the HFA-0005, good high frequency (RF) techniques should be used when making a PC board. A massive ground plane should be used to maintain a low impedance ground. Proper shielding and use of short interconnection leads are also very important.

To achieve maximum high frequency performance, the use of low impedance transmission lines with impedance matching is recommended: 50Ω lines are common in communications and 75Ω lines in video systems. Impedance matching is important to minimize reflected energy therefore minimizing transmitted signal distortion. This is accomplished by using a series matching resistor (50Ω or 75Ω), matched transmission line (50Ω or 75Ω), and a matched terminating resistor, as shown in Figure 30. Note that there will be a 6dB loss from input to output. The HFA-0005 has an integral 50Ω ±20% resistor connected to the op amp's output with the other end of the resistor pinned out. This 50Ω resistor can be used as the series resistor instead of an external resistor.

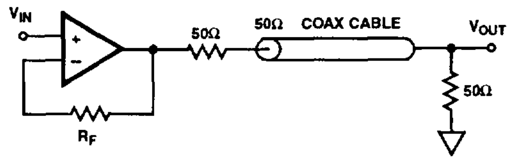



FIGURE 30.

PC board traces can be made to look like a 50Ω or 75Ω transmission line, called microstrip. Microstrip is a PC board trace with a ground plane directly beneath, on the opposite side of the board, as shown in Figure 31.

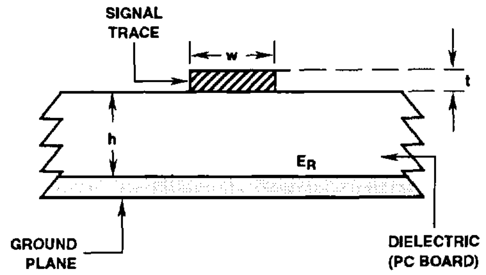



FIGURE 31.

When manufacturing pc boards the trace width can be calculated based on a number of variables.

The following equation is reasonably accurate for calculating the proper trace width for a 50Ω transmission line.

$$Z_0 = \frac{87}{\sqrt{E_R + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \Omega$$

Power supply decoupling is essential for high frequency op amps. A 0.01μF high quality ceramic capacitor at each supply pin in parallel with a 1μF tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance. The figures that follow illustrate two different decoupling schemes. Figure 33 improves the PSRR because the resistor and capacitors create low pass filters. Note that the supply current will create a voltage drop across the resistor.

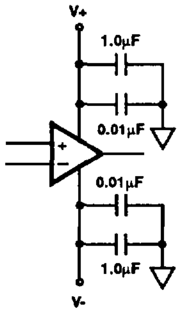



FIGURE 32.

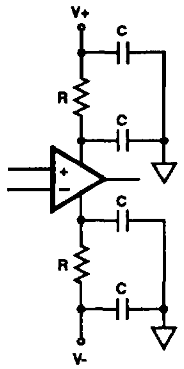



FIGURE 33.

**Saturation Recovery**

When an op amp is over driven output devices can saturate and sometimes take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time from 25% overdrive is 20ns and 30ns from 50% overdrive.