HARRIS

HA-5147/883

Ultra-Low Noise, Precision, High Slew Rate Wideband Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Slew Rate ..... 28V/μs (Min)
- Wide Gain Bandwidth ($A_V \geq 10$) ..... 100MHz (Min)
- Low Noise (@1kHz)..... 4.5nV/$\sqrt{Hz}$ (Max)
- Low Offset Voltage ..... 100μV (Max)
- Low Offset Drift With Temperature .. 1.8μV/°C (Max)
- High CMRR..... 100dB (Min)
- High Voltage Gain ..... 700V/mV (Min)

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Description

The HA-5147/883 monolithic operational amplifier features an unparalleled combination of precision D.C. and wideband high speed characteristics. Utilizing the Harris D.I. technology and advanced processing techniques, this unique design unites low noise precision instrumentation performance with high speed wideband capability.

This amplifier's impressive list of features include low V_{OS}, wide gain-bandwidth, high open loop gain, and high CMRR. Additionally, this flexible device operates over a wide supply range while consuming only 120mW of power.

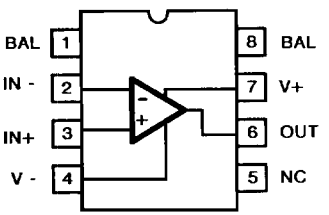
Using the HA-5147/883 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

This device is ideally suited for low level transducer signal amplifer circuits. Other applications which can utilize the HA-5147/883's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

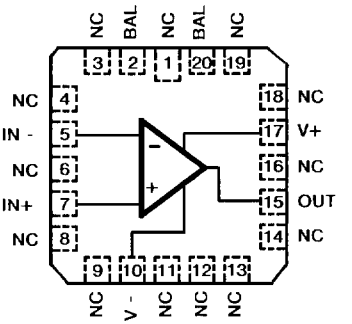
This device can easily be used as a design enhancement by directly replacing the 725, OP-25, OP-06, OP-07, OP-27 and OP-37 where gains are greater than ten. The HA-5147/883 is available in TO-99 Metal Can, Ceramic 8 Pin Mini-DIP, and 20 Pin Ceramic LCC packages.

Pinouts

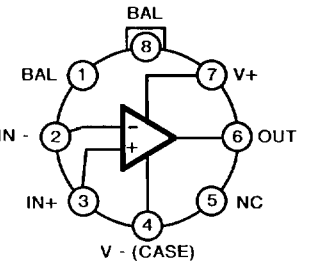
HA7-5147/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5147/883 (CERAMIC LCC)
TOP VIEW



HA2-5147/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 6) 0.7V
Voltage at Either Input Terminal ..... V+ to V-
Input Current 25mA
Differential Output Current ..... Full Short Circuit Protection
Junction Temperature (T_J) ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... < 2000V
Lead Temperature (Soldering 10 sec) ..... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	25°C/W
Ceramic LCC Package	84°C/W	25°C/W
Metal Can Package	98°C/W	30°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq +175°C$
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.19W
Metal Can Package 1.02W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 12.2mW/°C
Ceramic LCC Package ..... 11.9mW/°C
Metal Can Package ..... 10.2mW/°C

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±15V

$V_{INcm} \leq 1/2\ (V+ - V-)$
$R_L \geq 600\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-100	100	µV
			2, 3	+125°C, -55°C	-300	300	µV
Input Bias Current	I_B	$V_{CM} = 0V$, $R_S = 10k\Omega, 50\Omega$, $\left(\frac{\lvert+I_B\rvert+\lvert-I_B\rvert}{2}\right)$	1	+25°C	-	80	nA
			2, 3	+125°C, -55°C	-	150	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-135	135	nA
Common Mode Range	+CMR	V+ = 4.7V, V- = -25.3V	1	+25°C	10.3	-	V
			2, 3	+125°C, -55°C	10.3	-	V
	-CMR	V+ = 25.3V, V- = -4.7V	1	+25°C	-	-10.3	V
			2, 3	+125°C, -55°C	-	-10.3	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and $+10V$, $R_L = 2k\Omega$	4	+25°C	700	-	kV/V
			5, 6	+25°C, -55°C	300	-	kV/V
	$-A_{VOL}$	$V_{OUT} = 0V$ and $-10V$, $R_L = 2k\Omega$	4	+25°C	700	-	kV/V
			5, 6	+125°C, -55°C	300	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +11V$	1	+25°C	100	-	dB
		$\Delta V_{CM} = +10V$	2, 3	+125°C, -55°C	100	-	dB
	-CMRR	$\Delta V_{CM} = -11V$	1	+25°C	100	-	dB
		$\Delta V_{CM} = -10V$	2, 3	+125°C, -55°C	100	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	4	+25°C	11.5	-	V
			5, 6	+125°C, -55°C	11.5	-	V
	$-V_{OUT1}$	R_L = 2kΩ	4	+25°C	-	-11.5	V
			5, 6	+125°C, -55°C	-	-11.5	V
	$+V_{OUT2}$	R_L = 600Ω	4	+25°C	10	-	V
	$-V_{OUT2}$	R_L = 600Ω	4	+25°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	16.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-16.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	4	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	4	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25°C	-4	-	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-4	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 14V	1	+25°C	86	-	dB
		ΔV_{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV_{SUP} = 14V	1	+25°C	86	-	dB
		ΔV_{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
Offset Voltage Adjustment	$+V_{IO}$Adj	Note 5	1	+25°C	V_{IO} -1	-	mV
			2, 3	+125°C, -55°C	V_{IO} -1	-	mV
	$-V_{IO}$Adj	Note 5	1	+25°C	V_{IO} +1	-	mV
			2, 3	+125°C, -55°C	V_{IO} +1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} =50pF, A_{VCL} = +10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -4V to +4V	7	+25°C	28	-	V/µs
	-SR	V_{OUT} = +4V to -4V	7	+25°C	28	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	50	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	50	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	1	-55°C to +125°C	-	1.8	µV/°C
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	0.8	-	MΩ
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.25	μV_{p-p}
Input Noise Voltage Density	E_n	R_S = 20Ω, f_O = 10Hz	1, 4	+25°C	-	8.0	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 100Hz	1, 4	+25°C	-	5.6	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 1kHz	1, 4	+25°C	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_O = 10Hz	1,4	+25°C	-	4.0	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 100Hz	1, 4	+25°C	-	2.3	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 1kHz	1, 4	+25°C	-	0.6	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	V_O = 100mV, f_O = 10kHz	1	+25°C	120	-	MHz
		V_O = 100mV, f_O = 1MHz	1	+25°C	100	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	445	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	±10	-	V/V
Settling Time	T_S	To 0.1% for a 10V Step	1	+25°C	-	600	µs
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	100	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	120	mW

NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/(2πV_{PEAK}).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.
5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.
6. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

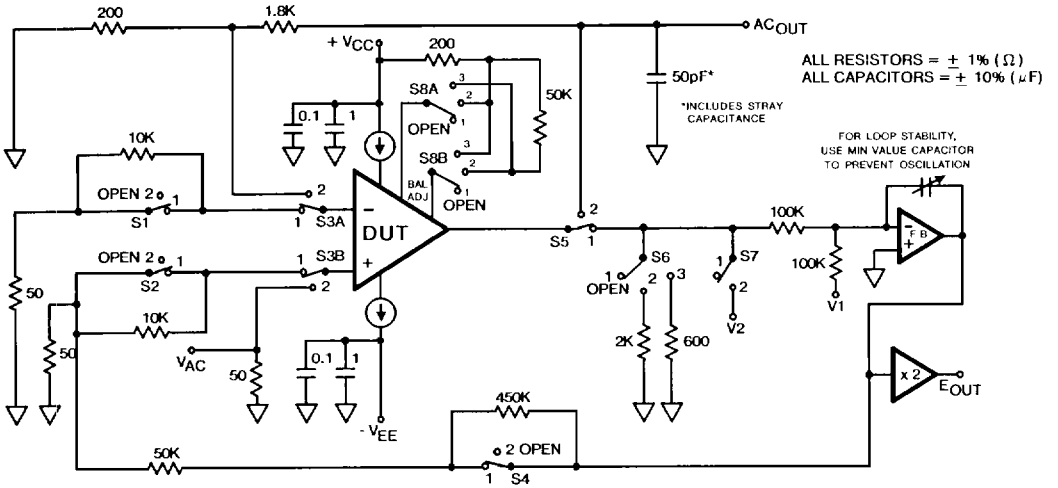
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/135, with the exception of V_{IO}, which is Subgroups 1, 2, and 3.

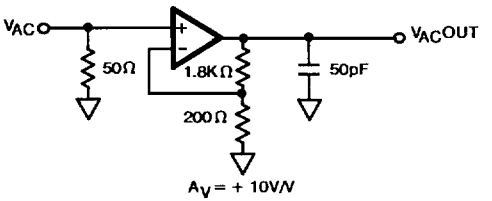
Test Circuit (Applies to Tables 1 and 2)



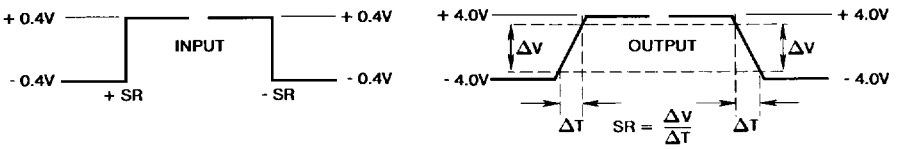
For Op-Amp Test Circuits and Conditions, Refer to the Harris Tech Brief "HA-5147 Op-Amp Test Methods". The HA-5147/883 is A.C. Tested (Table 2) at A_V = +10V/V.

Test Waveforms

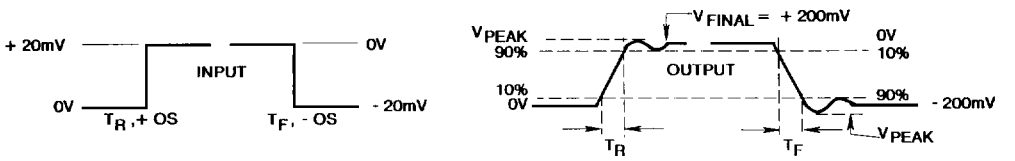
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORM



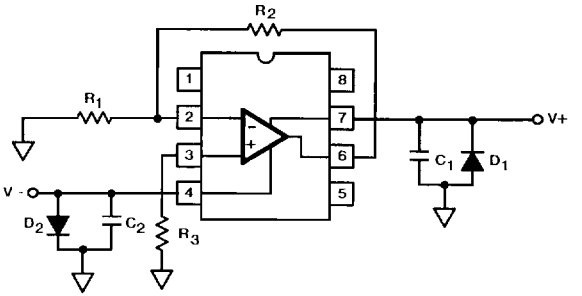
TRANSIENT RESPONSE WAVEFORM



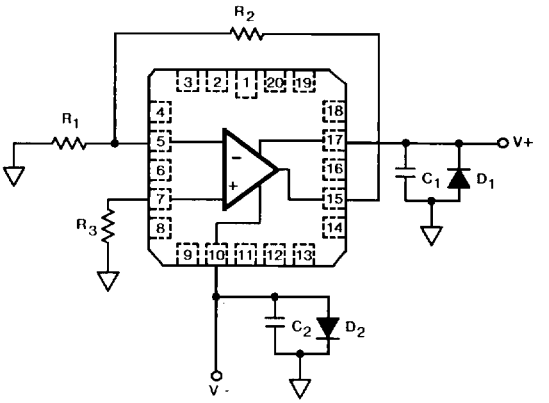
NOTE: Measured on Both positive and negative transitions.

Burn-In Circuits

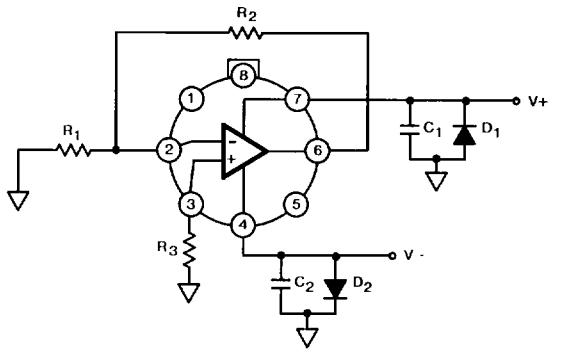
HA7-5147/883 CERAMIC DIP



HA4-5147/883 CERAMIC LCC



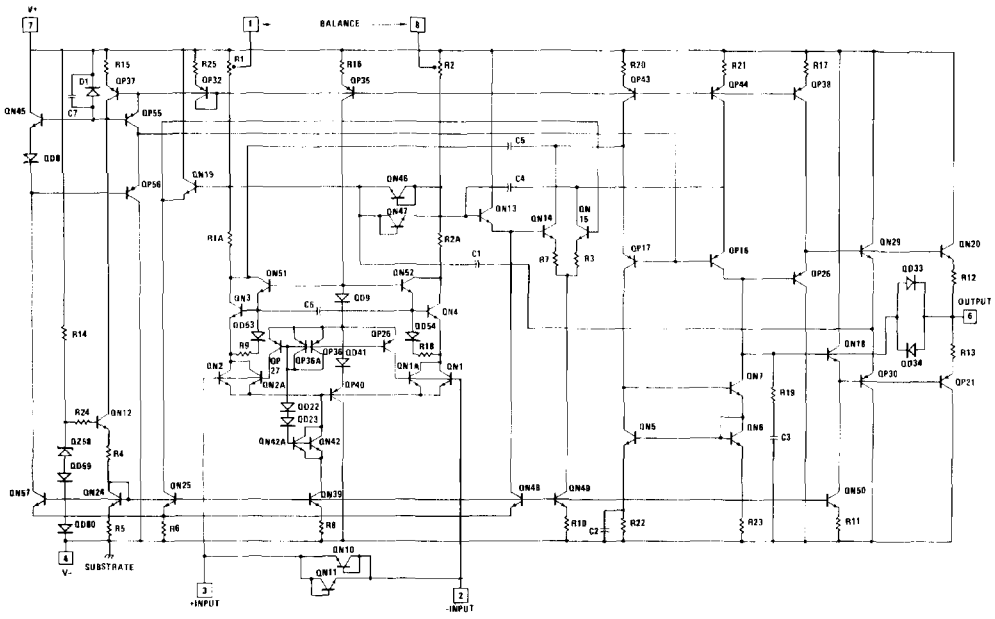
HA2-5147/883 (TO-99) METAL CAN



NOTES:

R_1 = R3 = 1kΩ, ±5%, 1/4W (Min)
R_2 = 10kΩ ±5%, 1/4W (Min)
C_1 = C_2 = 0.01μF/ per Socket (Min) or 0.1μF/Row (Min)
D_1 = D_2 = IN4002 or Equivalent/Board
|(V+) - (V-)| = 30V

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
104.3 x 65 x 19 mils
(2650 x 1650 x 483 µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$3.6 \times 10^5 A/cm^2$ @15mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Silox
Thickness: 7kÅ ± 0.7kÅ

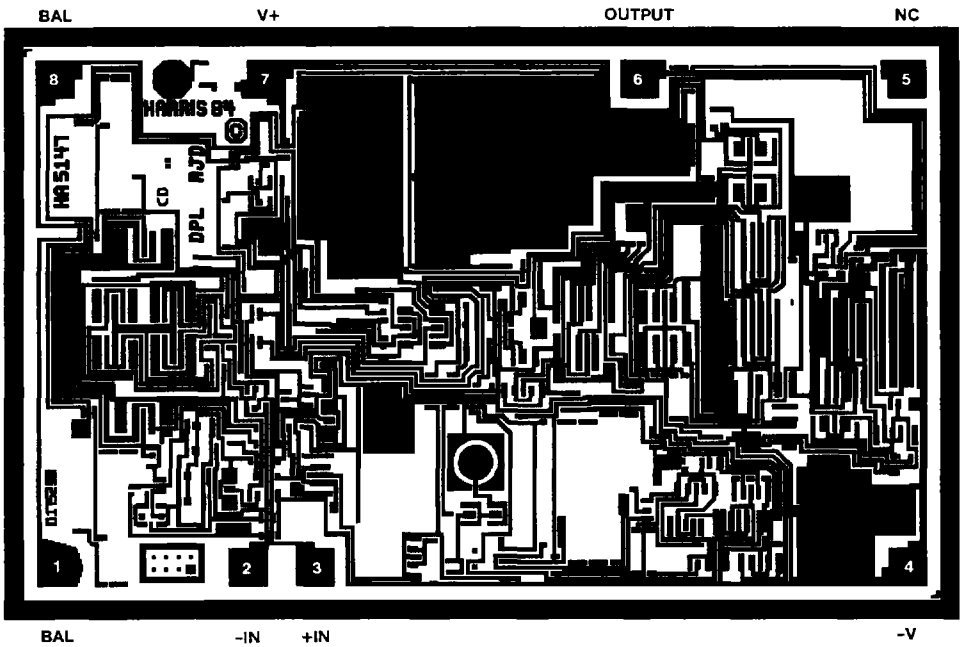
TRANSISTOR COUNT: 63

PROCESS: HFHB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

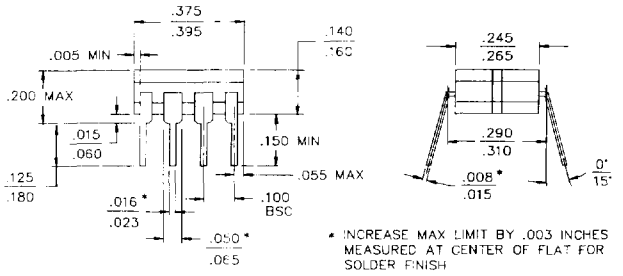
HA-5147/883



NOTE: Pin Numbers Correspond to 8 Pin Metal Can and Mini-DIP Package Only.

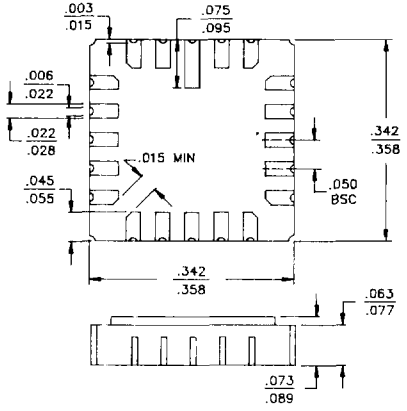
Packaging †

8 PIN CERAMIC DIP



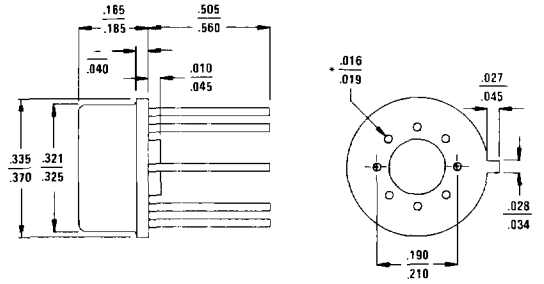
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

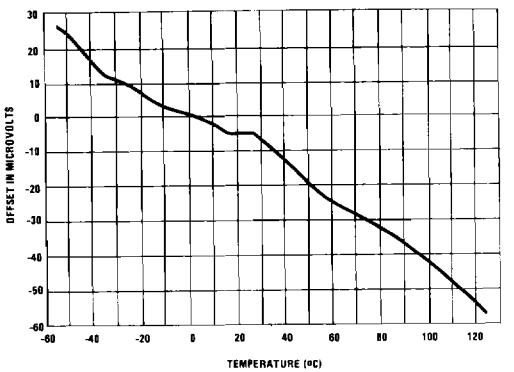
NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

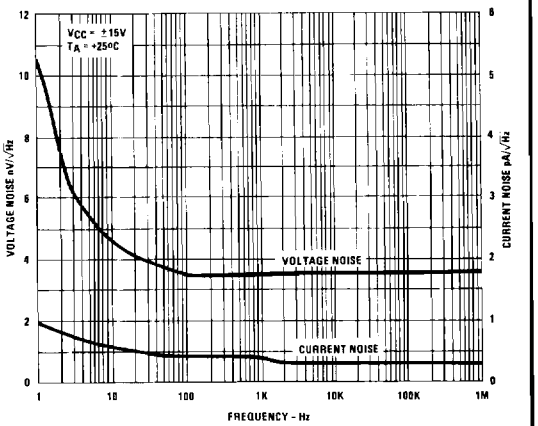
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

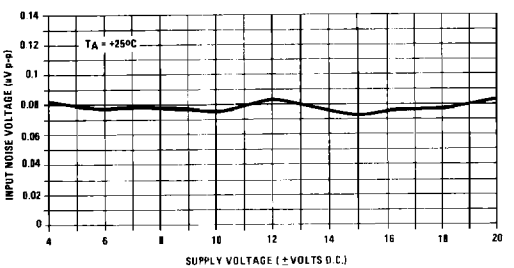
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



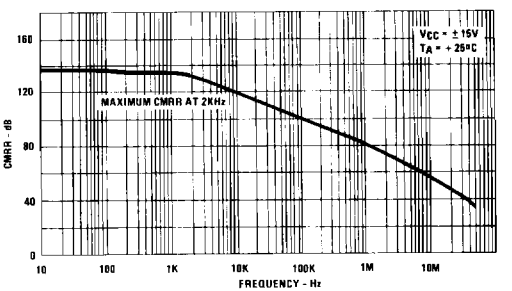
NOISE CHARACTERISTICS



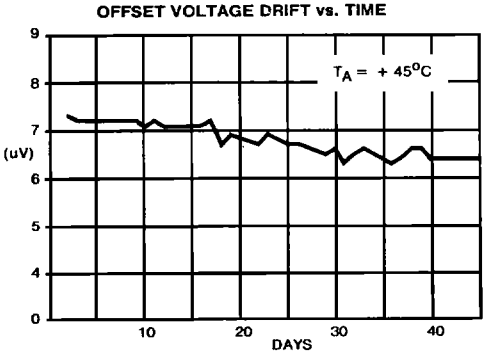
NOISE vs. SUPPLY VOLTAGE



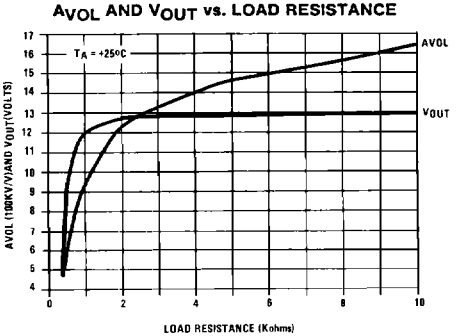
CMRR vs. FREQUENCY



OFFSET VOLTAGE DRIFT vs. TIME



A_{VOL} AND V_{OUT} vs. LOAD RESISTANCE

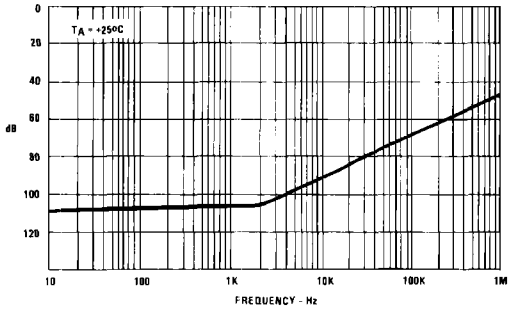


DESIGN INFORMATION (Continued)

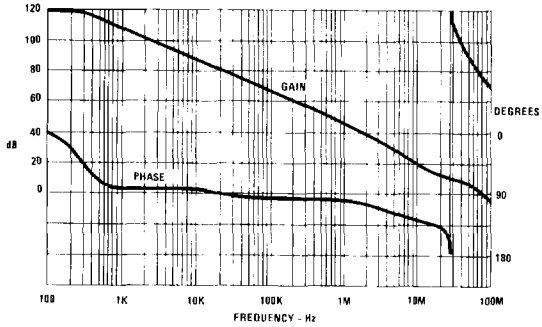
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

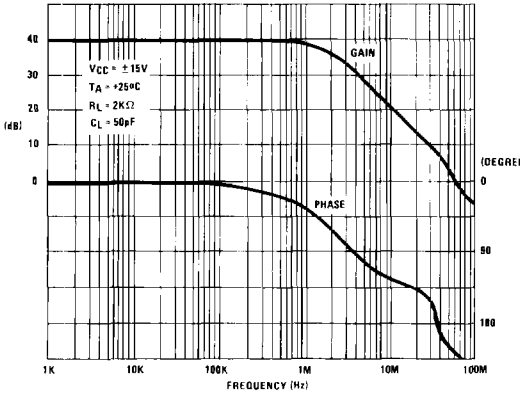
PSRR vs. FREQUENCY



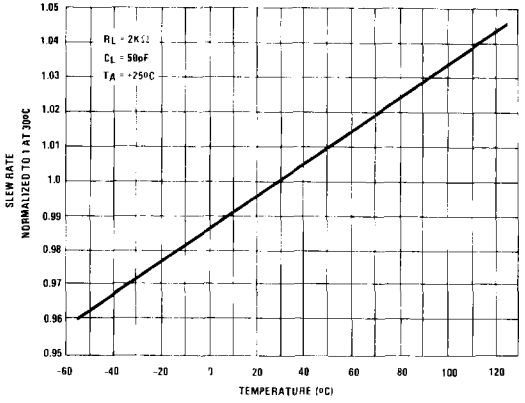
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



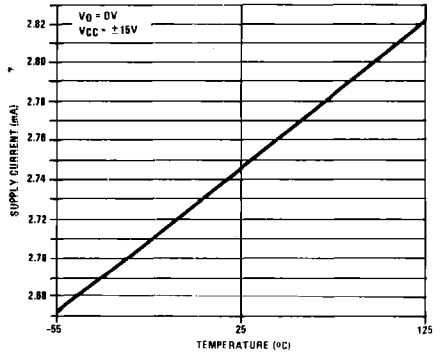
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



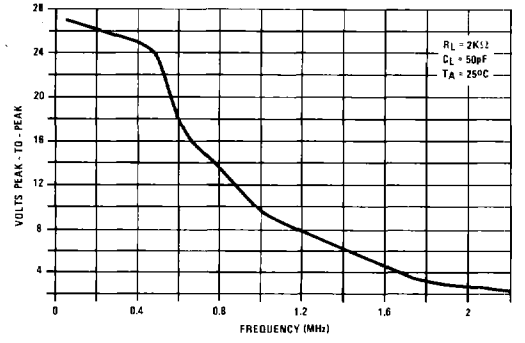
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



V_{OUT} MAX vs. FREQUENCY UNDISTORTED SINEWAVE OUTPUT

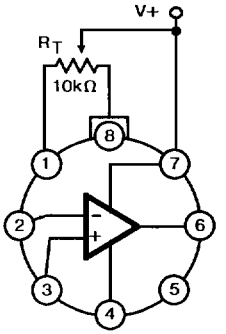


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

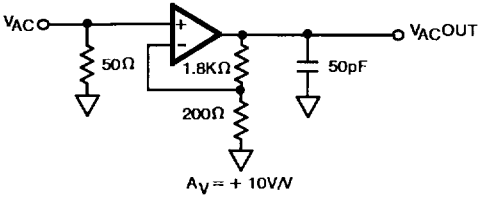
Typical Performance Information Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

SUGGESTED OFFSET VOLTAGE ADJUSTMENT

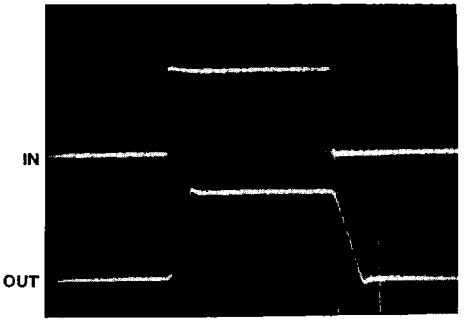


Tested Offset Adjustment Range is $|V_{OS}$ +mV$|$ minimum referred to output. Typical Range is ±4mV with R_T = 10kΩ.

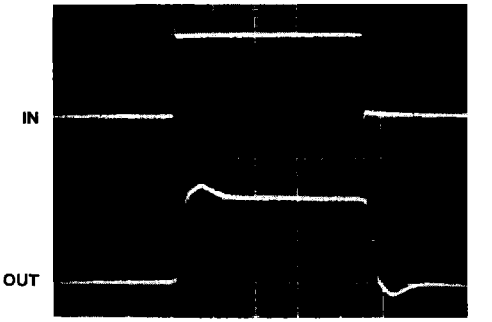
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 0.5V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)



MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 10mV/Div)
(Volts: Output = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)

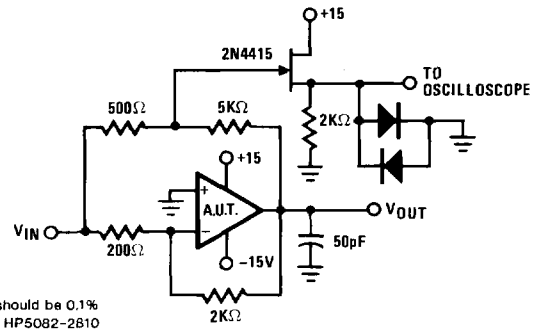


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

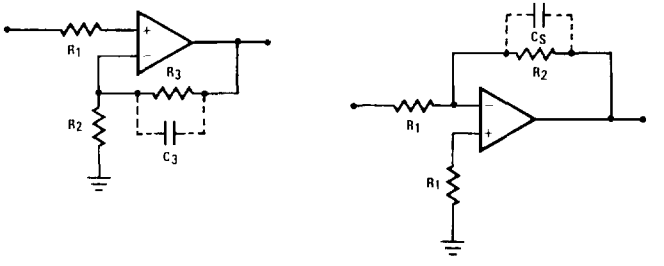
Typical Performance Information Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

SETTLING TIME TEST CIRCUIT



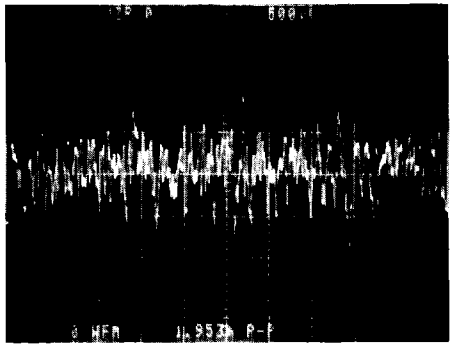
- $A_V = -10$
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional. HP5082-2810 recommended

SUGGESTED STABILITY CIRCUITS



Low resistances are preferred for low noise applications as a 1kΩ resistor has $4nV/\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{VCL}= 25,000V/V
Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
$0.08\mu V_{p-p}$ RTI



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	30	Table 1	µV
		Full	70	Table 1	µV
Offset Voltage Drift	Versus Temperature	Full	0.4	Table 3	µV/°C
	Versus Time	+45°C	0.71	1.5	µV/Month
Bias Current	V_{CM} = 0V	+25°C	±15	Table 1	nA
		Full	±35	Table 1	nA
Differential Input Resistance		+25°C	6	Table 3	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	4.4	Table 3	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	3.4	Table 3	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	3.2	Table 3	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	1.7	Table 3	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.0	Table 3	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.4	Table 3	$pA/\sqrt{Hz}$
Voltage Gain	V_{OUT} = ±10V	+25°C	1.8	Table1	MV/V
		Full	1.2	Table 1	MV/V
CMRR	ΔV = ±10V	Full	126	Table 1	dB
PSRR	V_S = ±4 to ±18V	Full	110	Table 1	dB
Slew Rate	V_{OUT} = ±5V	+25°C	35	Table 2	V/µs
Overshoot	V_{OUT} = ±200mV	+25°C	20	Table 2	%
Settling Time	10V to 0.1%	+25°C	400	Table 3	ns
	10V to 0.01%	+25°C	800	1000	ns
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±4	±5	V