HARRIS HA-2544/883

January 1989

Video Operational Amplifier

Features

- This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Unity Gain Bandwidth .... 45MHz (Min)
- High Slew Rate .... 100V/µs (Min)
- Low Supply Current .... 12mA (Max)
- Differential Gain Error .... 0.04dB (Max)
- Differential Phase Error .... 0.11% (Max)
- Gain Tolerance @ 3.58MHz or 4.43MHz .... 0.15dB (Max)
- Fast Settling Time (10V to 0.1%) ....120ns (Typ)

Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits
- Data Acquisition Systems

Description

The HA-2544/883 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (3.5kV/V min, 6kV/V typ), wide unity gain bandwidth of 45MHz minimum and phase margin of 65 degrees (open loop). Built from high quality Dielectric Isolation, the HA-2544/883 is another addition to the Harris series of high speed, wideband op amps, and offers true video performance combined with the versatility of an op amp.

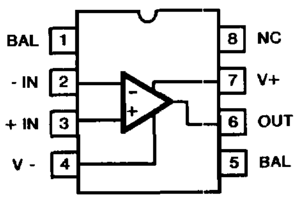
The primary features of the HA-2544/883, include wide bandwidth, 150V/µs (typ) slew rate, < 0.05dB differential gain error, < 0.11 degrees differential phase error and gain tolerance of just 0.15dB at 3.58 MHz and 4.43MHz, therefore proving to be sufficient for video amplification. High performance and low power requirements are met with a supply current of only 10mA typically and 12mA over the full temperature range.

Uses of the HA-2544/883 range from video test equipment guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544/883 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

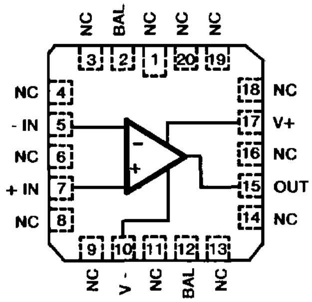
The HA-2544/883 is guaranteed over the military range of -55°C to +125°C and is offered in the 8 pin TO-99 Metal Can and Ceramic Mini-DIP or the 20 pad LCC.

Pinouts

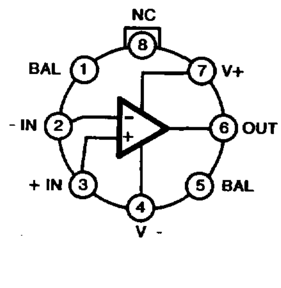
HA1-2544/883 (CERAMIC DIP)
TOP VIEW



HA4-2544/883 (CERAMIC LCC)
TOP VIEW



HA2-2544/883 (METAL CAN)
TOP VIEW



Case tied to V-

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 33V
Differential Input Voltage (Note 8) 6V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current (< 10% Duty Cycle) 40mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	129°C/W	47°C/W
Ceramic LCC Package	92°C/W	32°C/W
Metal Can Package	116°C/W	35°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq 175°C$
Ceramic DIP Package 780mW
Ceramic LCC Package 1.1W
Metal Can Package 860mW

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 7.8mW/°C
Ceramic LCC Package .... 11mW/°C
Metal Can Package .... 8.6mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$V_{INcm} \leq 1/2 (V+ - V-)$
$R_L \geq 1k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 10\Omega$, $R_{LOAD} = 500k\Omega$, $C_{LOAD} \leq 10pF$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-15	15	mV
			2, 3	+125°C, -55°C	-20	20	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$, $+R_S = 1k\Omega$, $-R_S = 10\Omega$	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-20	20	µA
	$-I_B$	$V_{CM} = 0V$, $+R_S = 10\Omega$, $-R_S = 1k\Omega$	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-20	20	µA
Input Offset Current	I_{IO}	$V_{CM} = 0V$, $+R_S = 1k\Omega$, $-R_S = 1k\Omega$	1	+25°C	-2	2	µA
			2, 3	+125°C, -55°C	-3	3	µA
Common Mode Range	+CMR	V+ = 5V, V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V, V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V, $R_L = 1k\Omega$	4	+25°C	3.5	-	kV/V
			5, 6	+125°C, -55°C	2.5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V, $R_L = 1k\Omega$	4	+25°C	3.5	-	kV/V
			5, 6	+125°C, -55°C	2.5	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +10V$, +V = +5V, -V = -25V, $V_{OUT} = -10V$	1	+25°C	75	-	dB
			2, 3	+125°C, -55°C	75	-	dB
	-CMRR	$\Delta V_{CM} = -10V$, +V = +25V, -V = -5V, $V_{OUT} = +10V$	1	+25°C	75	-	dB
			2, 3	+125°C, -55°C	75	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 10Ω, R_{LOAD} = 500kΩ, $C_{LOAD} \leq$ 10pF, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	$+V_{OUT}$	R_L = 1kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT}$	R_L = 1kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	1	+25°C	25	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	1	+25°C	-	-25	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	12	mA
			2, 3	+125°C, -55°C	-	12	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-12	-	mA
			2, 3	+125°C, -55°C	-12	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 6	1	+25°C	V_{IO}-1	-	mV
	$-V_{IO}Adj$	Note 6	1	+25°C	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, V_{OUT} = 1V/V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	V_{OUT} = -3V to +3V	7	+25°C	100	-	V/μs
	-SR	V_{OUT} = +3V to -3V	7	+25°C	100	-	V/μs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, A_V = 1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Gain	dA_V	R_S = 50Ω, R_L = 1kΩ f_O = 3.58MHz and 4.43MHz	1, 5, 7, 9, 11	+25°C	-	0.04	dB
Differential Phase	d0	R_S = 50Ω, R_L = 1kΩ f_O = 3.58MHz and 4.43MHz	1, 5, 7, 9	+25°C	-	0.11	Degrees
Unity Gain Bandwidth	UGBW	V_O = 200mV_{RMS}, f @ -3dB	1, 5	+25°C	45	-	MHz
Gain Tolerance	ΔA_V	V_O = 200mV_{RMS}, f_O = 5MHz	1, 5, 7	+25°C	-0.15	0.15	dB
		V_O = 200mV_{RMS}, f_O = 10MHz	1, 5, 7	+25°C	-0.35	0.35	dB
Full Power Bandwidth	FPBW	V_{PEAK} = 1V	1, 2	+25°C	15.9	-	MHz
		V_{PEAK} = 5V	1, 2	+25°C	3.2	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 1kΩ, $C_L \leq$ 1pF	1, 5	-55°C to +125°C	1	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	15	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	15	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	20	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	20	%
Settling Time	T_S	To 0.1% for a 10V Step	1	+25°C	-	150	ns
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	40	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	360	mW

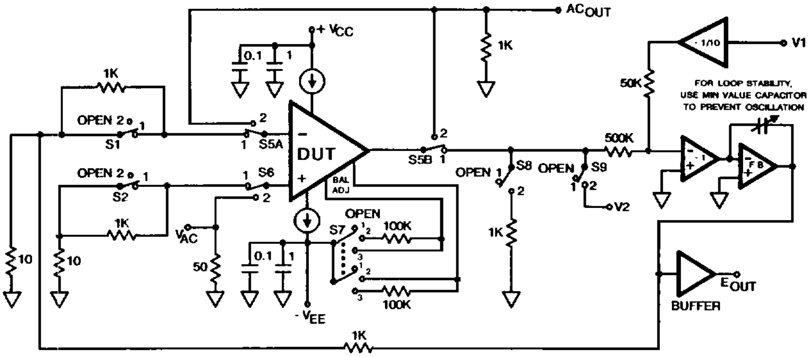
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Measured between 10% and 90% points.
5. Sample tested on every lot.
6. Offset adjustment range is [$V_{IO\ (Measured)}$ ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.
7. The video parameter specifications will degrade as the output load resistance decreases.
8. To achieve optimum AC performance, the input stage was designed without protective diode clamps. Exceeding the maximum differential input voltage results in reverse breakdown to the base-emitter junction of the input transistors and probable degradation of the input parameters especially V_{OS}, I_{OS} and Noise.
9. Test signal used is 200mV_{RMS} at each frequency on a 0 and 1 volt offset. For adaquate test repeatability, a minimum warm-up of 2 minutes is suggested.
10. C-L Gain and C-L Delay was less than the resolution to the test equipment used which is 0.1dB and 7ns, respectively.
11. $A_D(\%) = \left[10^{\frac{A_D\,(dB)}{20}} - 1\right] \times 100$

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Table 1)

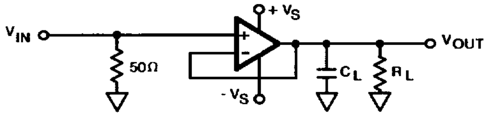


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-2544/883 Test Tech Brief

Test Waveforms

SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL RESPONSE (Applies to Tables 2 and 3)



$V_S = \pm 15V$, $A_V = +1$
$R_L = 1k\Omega$, $C_L \leq 10pF$
V_{IN} for Large Signal = ±3V,
V_{IN} for Small Signal = 0 to +200mV and 0 to -200mV

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (2V/Div.)
Horizontal Scale: Time: 20ns/Div.

INPUT

OUTPUT

$A_V = +1V/V$, $R_L = 1k\Omega$

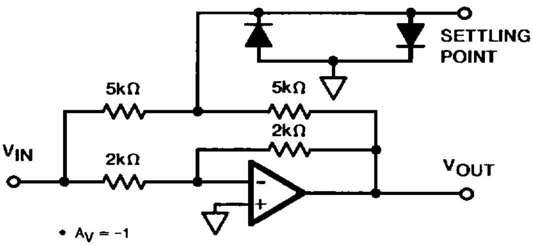
MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (100mV/Div.)
Horizontal Scale: Time: 20ns/Div.

INPUT

OUTPUT

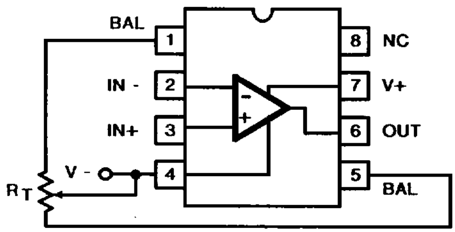
$A_V = +1V/V$, $R_L = 1k\Omega$
Note: Tested on both positive and negative edges.

SETTLING TIME TEST CIRCUIT FOR TABLE 3



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%).
- HP5082-2810 Clipping Diodes Recommended.
- Tektronix P6201 FET Probe Used At Settling Point.

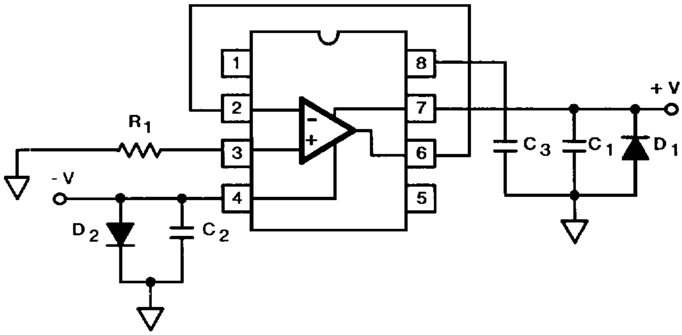
OFFSET VOLTAGE ADJUSTMENT CONNECTIONS



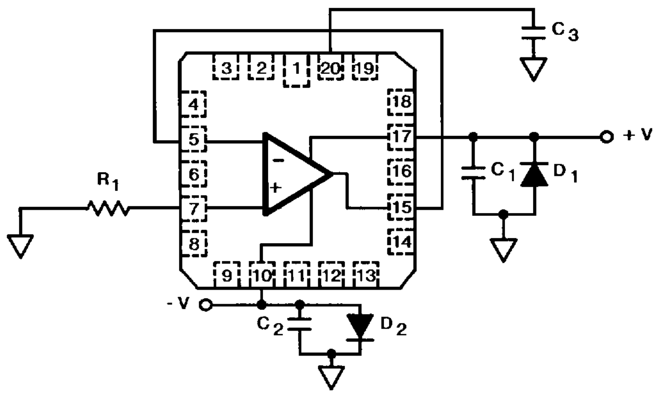
Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ Minimum Referred To Output. Typical Range For $R_T = 20k\Omega$ is Approximately ±30mV.

Burn-In Circuits

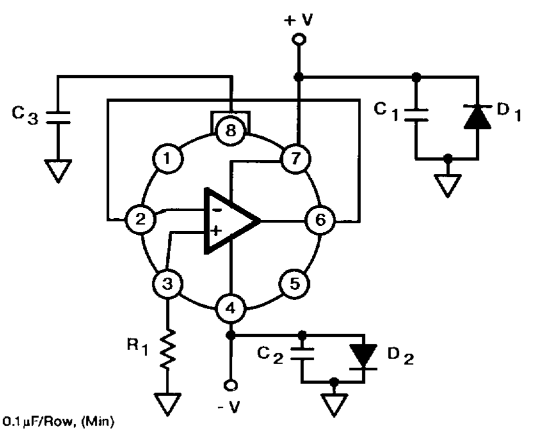
HA7-2544/883 CERAMIC DIP



HA4-2544/883 CERAMIC LCC



HA2-2544/883 TO-99 METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)

C_1 = C_2 = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

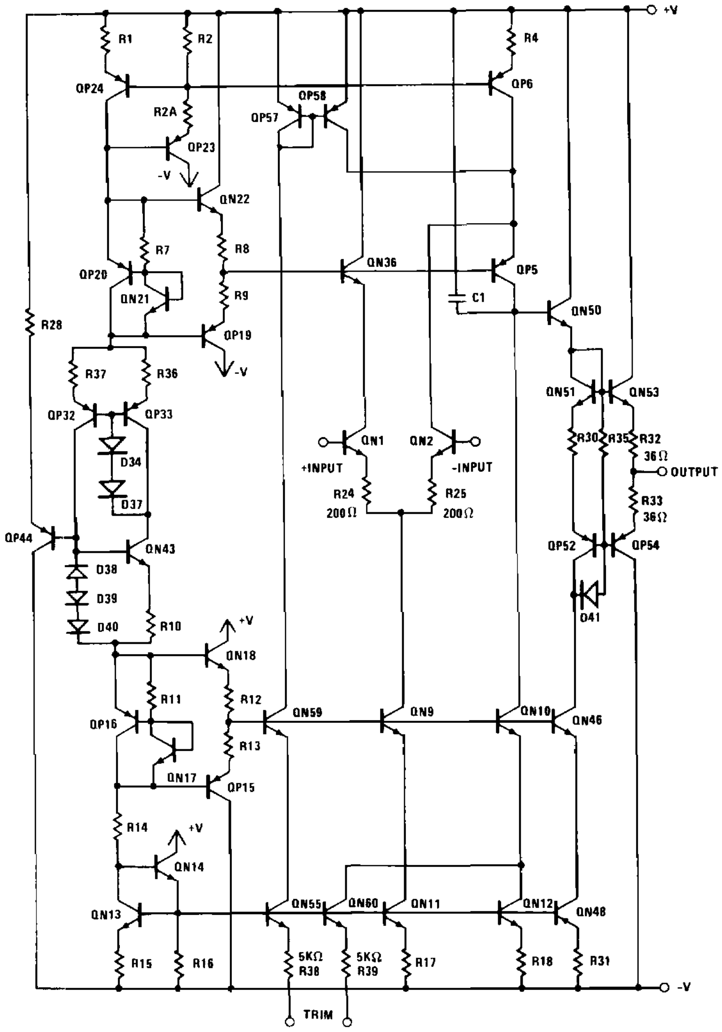
C_3 = 0.01μF/Socket, 10%

D_1 = D_2 = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

(C_3 is not required for HA-2544/883 compensation. It is shown here as standard pinout fixturing from B.I. boards used.)

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
79.9 x 64.2 x 19 mils
(2030 x 1630 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.3 \times 10^5 A/cm^2$

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

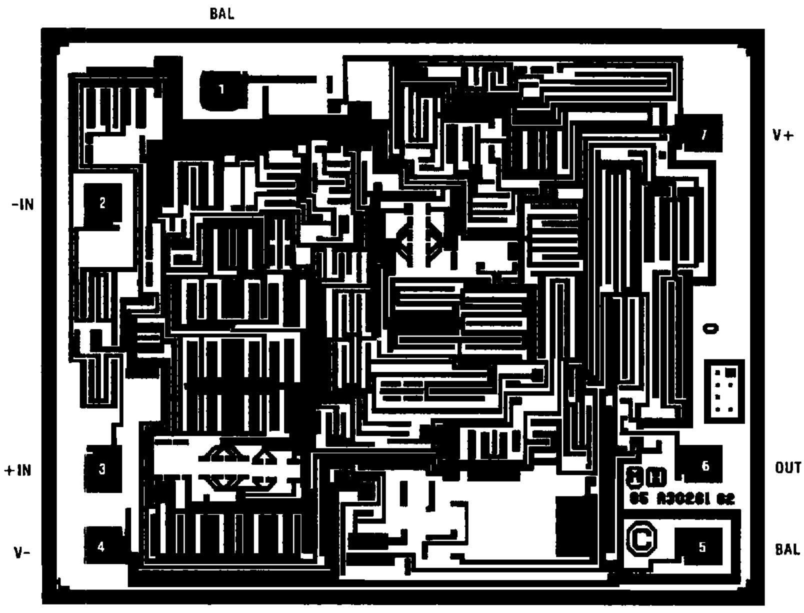
TRANSISTOR COUNT: 44

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

HA-2544/883

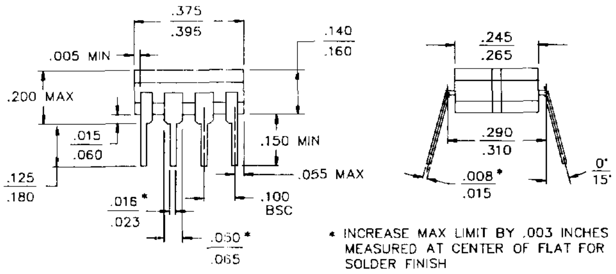


NOTE: Pin Numbers Correspond to Ceramic Mini-DIP and 8 Pin (TO-99) Metal Can Packages Only.

3
OP AMPs & COMPARATORS

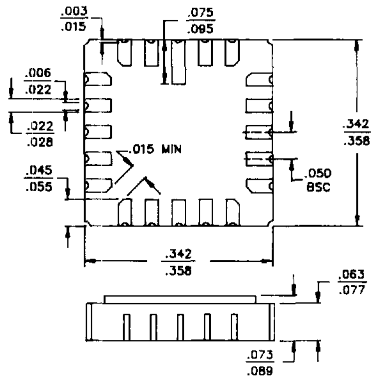
Packaging †

8 PIN CERAMIC DIP



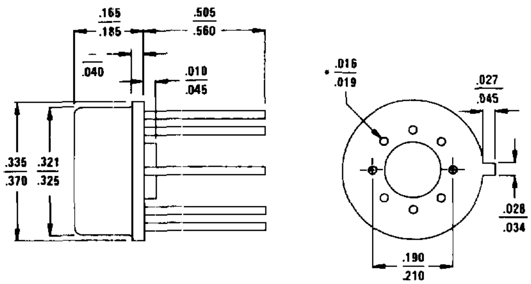
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

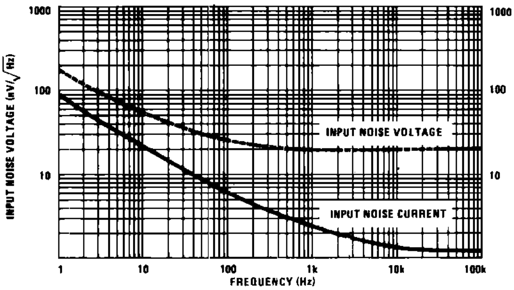
DESIGN INFORMATION

Video Operational Amplifier

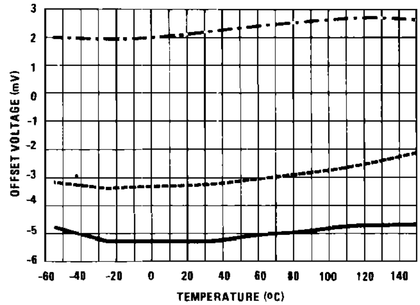
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

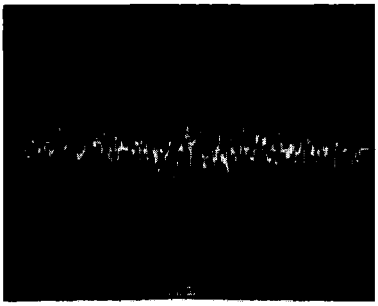
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



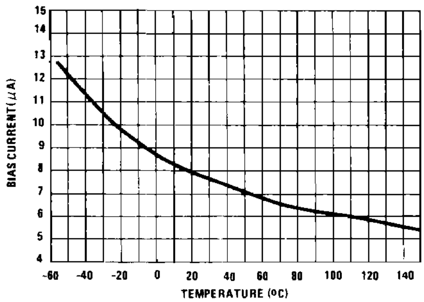
INPUT OFFSET VOLTAGE vs. TEMPERATURE
3 Typical Units



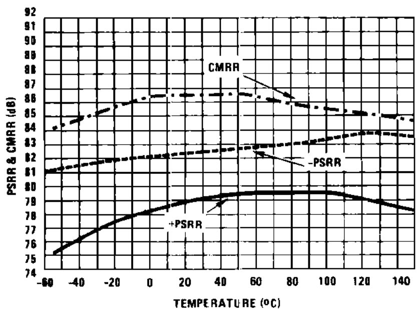
BROADBAND NOISE
$A_V = 1000$, 0.1Hz to 10Hz, Noise Voltage = $0.97\mu V_{p-p}$



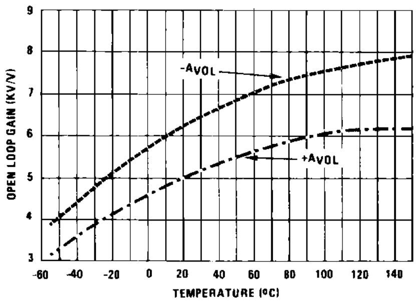
INPUT BIAS CURRENT vs. TEMPERATURE
$V_S = \pm15V$, $R_L = 1k\Omega$



PSRR AND CMRR vs. TEMPERATURE
$V_S = \pm15V$, $R_L = 1k\Omega$



OPEN LOOP GAIN vs. TEMPERATURE
$V_S = \pm15V$, $R_L = 1k\Omega$



3
OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

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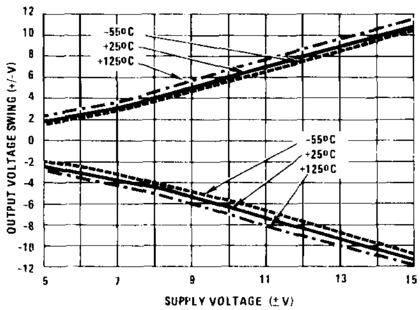
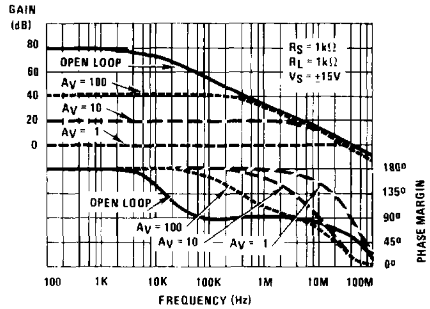
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

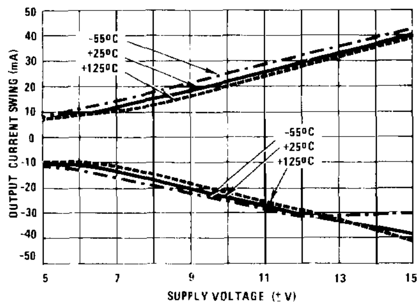
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
(Over Full Temperature)



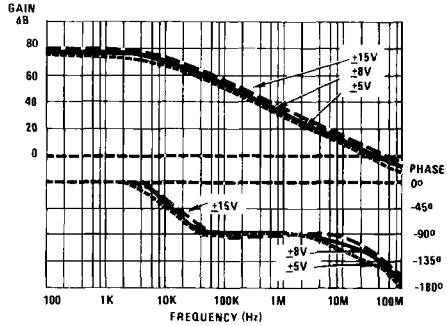
FREQUENCY RESPONSE AT VARIOUS GAINS
$R_S = 1k\Omega$, $R_L = 1k\Omega$, $V_S = \pm15V$



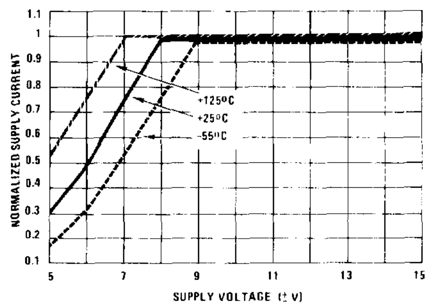
OUTPUT CURRENT vs. SUPPLY VOLTAGE
(Over Full Temperature)



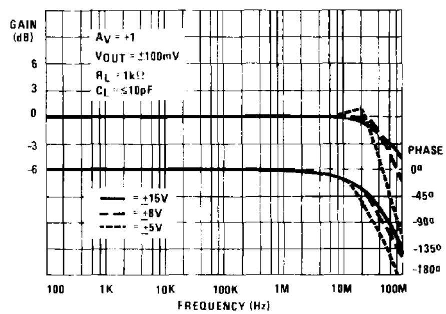
OPEN LOOP RESPONSE vs. SUPPLY VOLTAGE
$V_{OUT} = \pm100mV$



SUPPLY CURRENT vs. SUPPLY VOLTAGE
Normalized at $V_S = \pm15V$ at $+25^oC$



VOLTAGE FOLLOWER RESPONSE vs. SUPPLY VOLTAGE
$A_V = +1$, $R_L = 1K$, $C_L \leq 10pF$



DESIGN INFORMATION (Continued)

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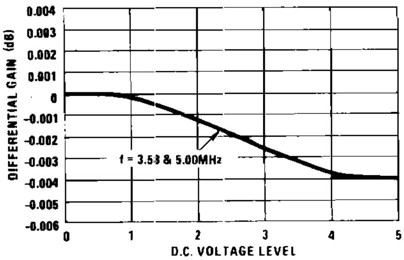
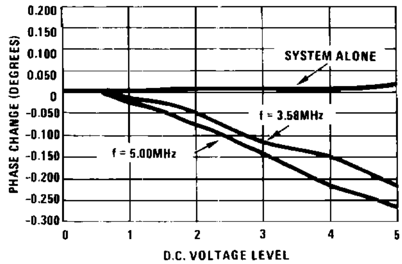
Typical Video Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

A.C. GAIN VARIATION vs. D.C. OFFSET LEVELS
(Differential Gain)

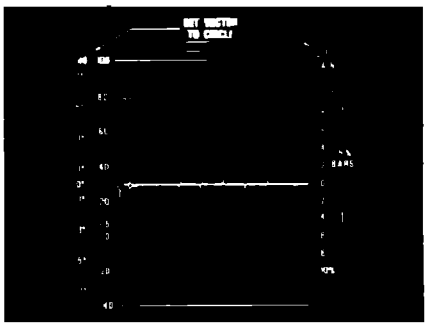


A.C. PHASE VARIATION vs. D.C. OFFSET LEVELS
(Differential Phase)

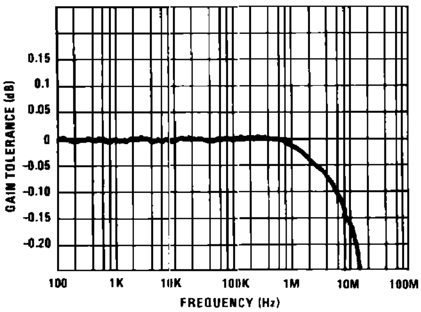


DIFFERENTIAL GAIN
NTSC Method, $R_L = 1k\Omega$
Differential Gain < 0.05% at $T_A = +75^oC$
No Visual Difference at $T_A = -55^oC$ of $+125^oC$

DIFFERENTIAL PHASE
NTSC Method, $R_L = 1k\Omega$
Differential Phase < 0.05 Degree at $T_A = +75^oC$
No Visual Difference at $T_A = -55^oC$ or $+125^oC$



GAIN TOLERANCE
$A_V = +1$, $V_{IN} = \pm100mV$
$R_L = 1K$, $C_L \leq 10pF$



CHROMINANCE TO LUMINANCE DELAY
NTSC Method, $R_L = 1k\Omega$
C-L Delay < 7ns at $T_A = +75^oC$
No Visual Difference at $T_A = -55^oC$ or $+125^oC$

Vertical Scale: Input = 100mV/Div.
Output = 50mV/Div.
Horizontal Scale: 500ns/Div.

DESIGN INFORMATION (Continued)

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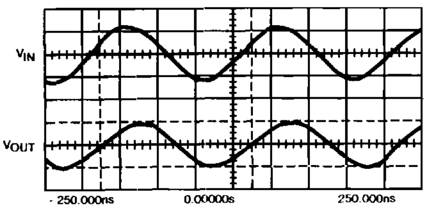
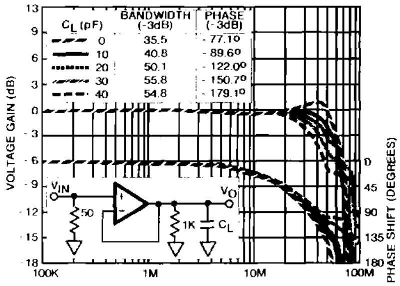
Typical Video Performance Curves (Continued) Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

±2 VOLT OUTPUT SWING
With $R_{LOAD} = 75\Omega$ (frequency = 5.00MHz)



V_{IN} = 2.0V/Div., V_{OUT} = 2.0V/Div.
Timebase = 50ns/Div.

BANDWIDTH vs. LOAD CAPACITANCE
$A_V = +1$, $V_S = \pm15V$, $R_L = 1k\Omega$



Applications And Product Guidelines

The HA-2544 is a true differential op amp that is as versatile as any op amp but offers the advantages of high unity gain bandwidth, high speed and low supply current. More important than its' general purpose applications is that the HA-2544 was especially designed to meet the requirements found in a video amplifier system. These requirements include fine picture resolution and accurate color rendition, and must meet broadcast quality standards.

In a video signal, the video information is carried in the amplitude and phase as well as in the D.C. level. The amplifier must pass the 30Hz line rate luminance level and the 3.58MHz (NTSC) or 4.43MHz (PAL) color band without altering phase or gain. The HA-2544's key specifications aimed at meeting this include high bandwidth (50MHz), very low gain tolerance (< ±0.15dB at 5MHz), near unmeasurable differential gain and differential phase (< 0.04dB and 0.11 degrees), and low noise ($20nV/\sqrt{Hz}$). The HA-2544 meets these quidelines and are sample tested for standard grade product (/883, -2, -7, -5) at 5 and/or 10MHz. If a customer wishes to 100% test these specifications, arrangement can be made.

The HA-2544 also offers the advantage of a full output voltage swing of ±10V into a 1K ohm load. This equates to a full power bandwidth of 2.4MHz for this ±10V signal. If video signal levels of ±2V maximum is used (with R_L = 1K ohm), the full power bandwidth would be 11.9MHz without clipping distortion. Another usage might be required for a direct 50 ohm or 75 ohm load where the HA-2544 will still swing this ±2V signal as shown in the above display. One important note that must be realized is that as load resistance decreases the video parameters are also degraded. For optimal video performance a 1kΩ load is recommended.

If lower supply voltage are required, such as ±5V, many of the characterization curves indicate where the parameters vary. As shown the bandwidth, slew rate and supply current are still very well maintained.

Prototyping and PC Board Layout

When designing with the HA-2544 video op amp as with any high performance device, care should be taken to use high frequency layout techniques to avoid unwanted parasitic effects. Short lead lengths, low source impedance and lower value feedback resistors help reduce unwanted poles or zeros. This layout would also include ground plane construction and power supply decoupling as close to the supply pins with suggested parallel capacitors of 0.1μF and 0.001μF ceramic to ground.

In the noninverting configuration, the amplifier is sensitive to stray capacitance (< 40pF) to ground at the inverting input. Therefore, the inverting node connections should be kept to a minimum. Phase shift will also be introduced as load parasitic capacitance is increased. A small series resistor (20 ohm to 100 ohm) before the capacitance effectively decouples this effect.

Stability/Phase Margin/Compensation

The HA-2544 has not sacrificed unity gain stability in achieving its superb AC performance. For this device, the phase margin exceeds 60 degrees at the unity crossing point of the open loop frequency response. Large phase margin is critical in order to reduce the differential phase and differential gain errors caused by most other op amps. Because this part is unity gain stable, no compensation pin is brought out. If compensation is desired to reduce the noise bandwidth, most standard methods may be used. One method suggested for an inverting scheme would be a series R-C from the inverting node to ground which will reduce bandwidth, but not effect slew rate. If the user wishes to achieve even higher bandwidth (> 50MHz), and can tolerate some slight gain peaking and lower phase margin, experimenting with various load capacitance can be done.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, $C_L \leq$ 10pF, A_V = 1V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	6	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	15	µV/°C
Bias Current	V_{CM} = 0V	+25°C	7	Table 1	µA
Average Bias Current Drift	Versus Temperature	Full	0.04	0.1	µA/°C
Offset Current	V_{CM} = 0V	+25°C	0.2	Table 1	µA
		Full	0.8	Table 1	µA
Common Mode Range		Full	±11.5	Table 1	V
Differential Input Resistance		+25°C	90	50	kΩ
Differential Input Capacitance		+25°C	3	4	pF
Input Noise Voltage Density	$f_O \geq$ 1kHz	+25°C	20	24	nV/√Hz
Input Noise Current Density	$f_O \geq$ 1kHz	+25°C	2.4	4	pA/√Hz
Large Signal Voltage Gain	V_{OUT} = ±5V	+25°C	6	Table 1	kV/V
		Full	3.5	Table 1	kV/V
CMRR	ΔV_{CM} = ±10V	Full	89	Table 1	dB
Gain Bandwidth Product		+25°C	50	45	MHz
Phase Margin	0dB GBWP Crossing	+25°C	65	55	Degrees
Output Voltage Swing		Full	±11	Table 1	V
Full Power Bandwidth	V_{PEAK} = 5V	+25°C	4.2	3.5	MHz
Peak Output Current	Note A	+25°C	±35	Table 1	mA
Output Resistance	Open Loop	+25°C	20	40	Ω
Rise/Fall Time	V_{OUT} = +200mV, -200mV	+25°C	7	Table 3	ns
± Overshoot	V_{OUT} = +200mV, -200mV	+25°C	10	Table 3	%
+ Slew Rate	V_{OUT} = -5V to +5V	+25°C	+165	Table 2	V/µs
- Slew Rate	V_{OUT} = +5V to -5V	+25°C	-125	Table 2	V/µs
Settling Time	A_V = -1V/V, 10V to 0.1%	+25°C	110	140	ns
	A_V = -1V/V, 10V to 0.01%	+25°C	120	150	ns
Differential Phase	R_S = 50Ω to 75Ω, Notes 7 and 9	+25°C	0.05	Table 3	Degrees
	R_S = 1kΩ, Notes 7 and 9	+25°C	0.4	0.6	Degrees
Differential Gain	R_S = 50Ω to 75Ω, Notes 7, 9, 11	+25°C	0.02	Table 3	dB
	R_S = 1kΩ, Notes 7, 9, 11	+25°C	0.15	0.3	dB
Chrominance to Luminance Gain	Note 10	+25°C	0.1	N/A	dB
Chrominance to Luminance Delay	Note 10	+25°C	7	N/A	ns
Gain Tolerance	5MHz	+25°C	-0.10	Table 3	dB
	10MHz	+25°C	-0.12	Table 3	dB
Supply Current	I_{OUT} = 0mA	Full	10	Table 1	mA
PSRR	ΔV_S = ±10V to ±20V	Full	80	Table 1	dB
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±6	V
Saturation Recovery Time	Full Saturation	+25°C	0.6	1.1	µs