

**OBSOLETE PRODUCT  
NO RECOMMENDED REPLACEMENT**  
contact our Technical Support Center at  
1-888-INTERSIL or www.intersil.com/tsc

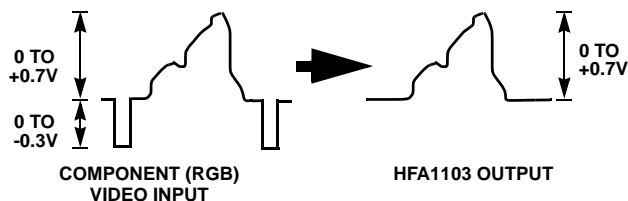
**200MHz, Video Op Amp with High Speed Sync Stripper**

The HFA1103 is a high-speed, wideband, fast settling current feedback op amp with a sync stripping function. The HFA1103 is a basic op amp with a modified output stage that enables it to strip the sync from a component video signal. The output stage has an open emitter NPN transistor that prevents the output from going low during the sync pulse. Removing the sync signal benefits digitizing systems because only the active video information is applied to the A/D converter. This enables the full dynamic range of the A/D converter to be used to process the video signal. The HFA1103 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

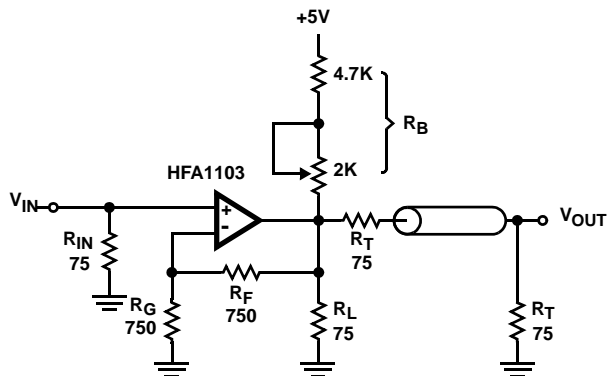
**Part # Information**

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1103IB (H1103I)	-40 to 85	8 Ld SOIC	M8.15

**Sync Stripper Waveforms**



**Application Schematic**



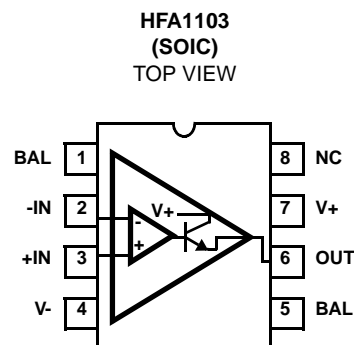
**Features**

- Removes Sync Signal From Component Video
- Low Residual Sync. . . . . 8mV (Typ)
- -3dB Bandwidth . . . . . 200MHz
- Very Fast Slew Rate. . . . . 600V/μs
- Fast Settling Time (0.1%) . . . . . 9ns
- Excellent Gain Flatness, 32MHz . . . . . ±0.1dB
- Overdrive Recovery . . . . . <12ns

**Applications**

- RGB Video Sync Stripping
- RGB Video Distribution Amplifier for Workstations and PC Networks
- Video Conferencing Systems
- RGB Video Monitor Preamp
- Fiberoptic Receivers

**Pinout**



**Absolute Maximum Ratings**

Voltage Between V+ and V- .....	12V
Input Voltage .....	V <sub>SUPPLY</sub>
Differential Input Voltage .....	.5V
Output Current (50% Duty Cycle) .....	60mA

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
SOIC Package .....	170
Maximum Junction Temperature (Plastic Package) .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C (Lead Tips Only)

**Operating Conditions**

Temperature Range .....

-40°C to 85°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications** V<sub>SUPPLY</sub> = ±5V, A<sub>V</sub> = +2, R<sub>F</sub> = 750Ω, R<sub>L</sub> = 50Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
<b>DC CHARACTERISTICS</b>						
Residual Sync (Note 2)	V <sub>IN</sub> = -300mV, A <sub>V</sub> = +1	25	-	8	10	mV
		Full	-	-	12	mV
Output Offset Voltage (Notes 3, 5)		25	-	10	30	mV
		Full	-	-	40	mV
Output Offset Voltage Drift (Note 3)		Full	-	10	-	μV/°C
V <sub>OS</sub> PSRR	ΔV <sub>S</sub> = ±1.25V	25	39	45	-	dB
		Full	35	-	-	dB
Non-Inverting Input Bias Current	+IN = 0V	25	-	5	40	μA
		Full	-	-	65	μA
Inverting Input Bias Current	-IN = 0V	25	-	5	50	μA
		Full	-	-	60	μA
-I <sub>BIAS</sub> Adjust Range (Notes 4, 6)		25	100	200	-	μA
Non-Inverting Input Resistance		25	25	50	-	kΩ
Inverting Input Resistance		25	-	16	30	Ω
Input Capacitance		25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±3.0	-	V
Input Noise Voltage	100kHz	25	-	4	-	nV/√Hz
+Input Noise Current	100kHz	25	-	18	-	pA/√Hz
-Input Noise Current	100kHz	25	-	21	-	pA/√Hz
<b>TRANSFER CHARACTERISTICS</b> A <sub>V</sub> = +2, Unless Otherwise Specified						
Open Loop Transimpedance		25	-	500	-	kΩ
-3dB Bandwidth	V <sub>OUT</sub> = 1.0V <sub>P-P</sub> , A <sub>V</sub> = +2	25	-	200	-	MHz
Gain Flatness	T <sub>0</sub> ±0.1dB	25	-	32	-	MHz
Minimum Stable Gain		Full	1	-	-	V/V
<b>OUTPUT CHARACTERISTICS</b> A <sub>V</sub> = +2, Unless Otherwise Specified						
Output Voltage (Note 3)		25, 85	2.5	3.0	-	V
		-40°C	1.75	2.5	-	V
Output Current		25, 85	50	60	-	mA
		-40°C	35	50	-	mA
Linearity Near Zero		25	-	0.01	-	%
<b>TRANSIENT RESPONSE</b> A <sub>V</sub> = +2, Unless Otherwise Specified						
Rise Time	V <sub>OUT</sub> = 2.0V Step	25	-	2	-	ns

**Electrical Specifications**  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +2$ ,  $R_F = 750\Omega$ ,  $R_L = 50\Omega$ , Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Overshoot	$V_{OUT} = 2.0V$ Step	25	-	10	-	%
Slew Rate	$A_V = +2$ , $V_{OUT} = 0$ to $2V$ , $+2V$ to $0V$	25	-	600	-	$V/\mu s$
0.1% Settling	$V_{OUT} = 2V$ to $0V$	25	-	9	-	ns
Overdrive Recovery Time	2X Overdrive	25	-	12	-	ns
<b>POWER SUPPLY CHARACTERISTICS</b>						
Supply Voltage Range		Full	$\pm 4.5$	-	$\pm 5.5$	V
Supply Current (No Load)		25	-	11	16	mA
		Full	-	-	23	mA

NOTES:

- The residual sync is specified at the output of a doubly terminated circuit (see page 1 of this data sheet).
- Since the HFA1103 has an open emitter NPN output stage, this measurement is only valid for positive values.
- The  $-I_{BIAS}$  current can be used to adjust the offset voltage to zero, but  $-I_{BIAS}$  does not flow bidirectionally because the HFA1103 output stage is an open emitter NPN transistor.
- $V_{OS}$  includes the error contribution of  $I_{BSN}$  at  $R_F = 750\Omega$ .
- This is the minimum change in inverting input bias current when a BAL pin is connected to V- through a  $50\Omega$  resistor.

**Test Circuit**

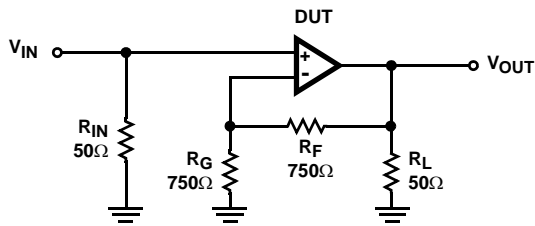


FIGURE 1. TEST CIRCUIT

**Application Information**

**Offset Adjustment**

The HFA1103 allows for adjustment of the inverting input bias current to null the output offset voltage.  $-I_{BIAS}$  flows through  $R_F$ , so any change in bias current forces a corresponding change in output voltage. The amount of adjustment is a function of  $R_F$ . With  $R_F = 750\Omega$ , the typical adjust range is 150mV. For offset adjustment connect a 10kΩ potentiometer between pins 1 and 5 with the wiper connected to V-.

**PC Board Layout**

The frequency performance of these amplifiers depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value ( $10\mu F$ ) tantalum in parallel with a small value chip ( $0.1\mu F$ ) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and

may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

**Evaluation Board**

The HFA1100 series evaluation board may be used for the HFA1103 with minor modifications. The evaluation board may be ordered using part number HFA11XXEVAL. Please note that an HFA1103 sample is not included with the evaluation board and must be ordered separately.

The layout and schematic of the board are shown below:

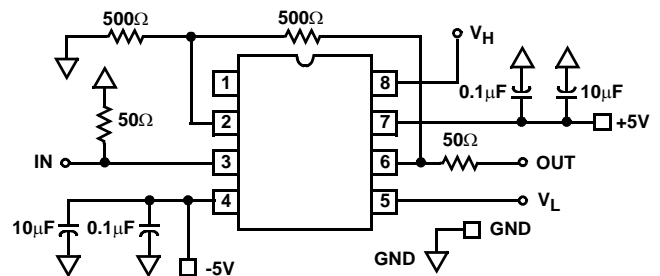


FIGURE 2. EVALUATION BOARD SCHEMATIC

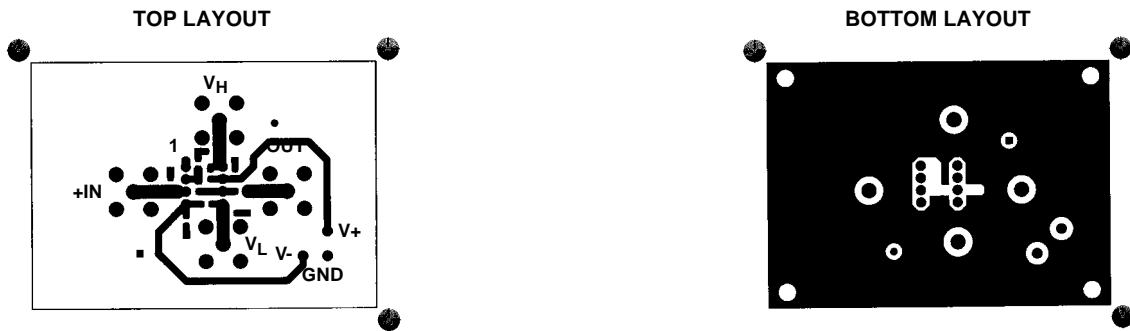


FIGURE 3. EVALUATION BOARD ARTWORK

**Typical Application**

A circuit which performs the sync stripper and DC restore functions is shown in Figure 4. Please reference Intersil Application Note AN9514, titled "Video Amplifier with Sync Stripper and DC Restore", for details on this circuit.

The standard output of a VM700 video measurement set is shown in Figure 5. The output, after passing through the Applications Schematic shown on the first page of this data sheet, is shown in Figure 6.

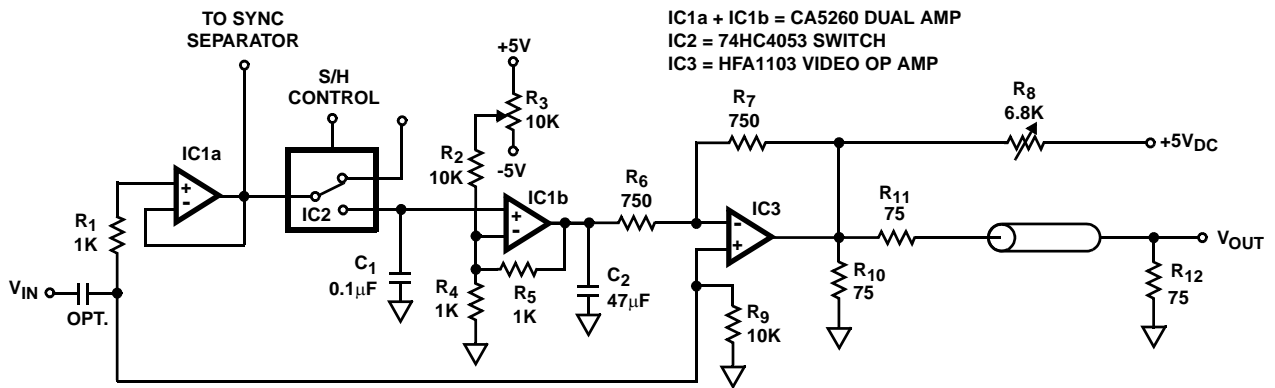


FIGURE 4. VIDEO AMPLIFIER WITH SYNC STRIPPER AND DC RESTORE

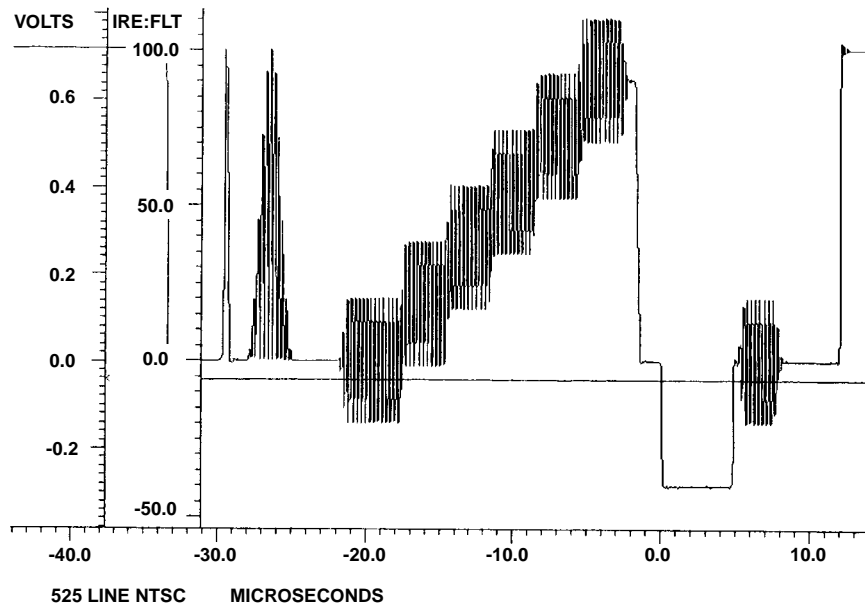


FIGURE 5. OUTPUT OF VM700 VIDEO MEASUREMENT SET

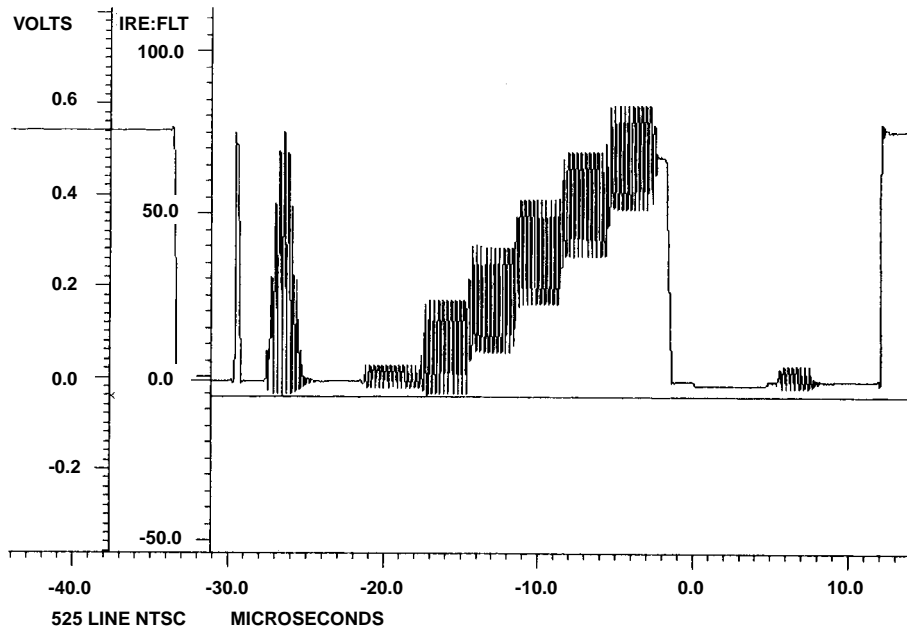


FIGURE 6. OUTPUT OF HFA1103 SYNC STRIPPER CONFIGURED AS ON THE FIRST PAGE OF THIS DATA SHEET

**Die Characteristics**

**DIE DIMENSIONS:**

63 mils x 44 mils x 19 mils  
 1600µm x 1130µm x 483µm

**METALLIZATION:**

Type: Metal 1: AlCu (2%)/TiW  
 Thickness: Metal1: 8kÅ ±0.4kÅ  
 Type: Metal 2: AlCu (2%)  
 Thickness: 16kÅ ±0.8kÅ

**SUBSTRATE POTENTIAL (POWERED UP):**

Floating (Recommend Connection to V-)

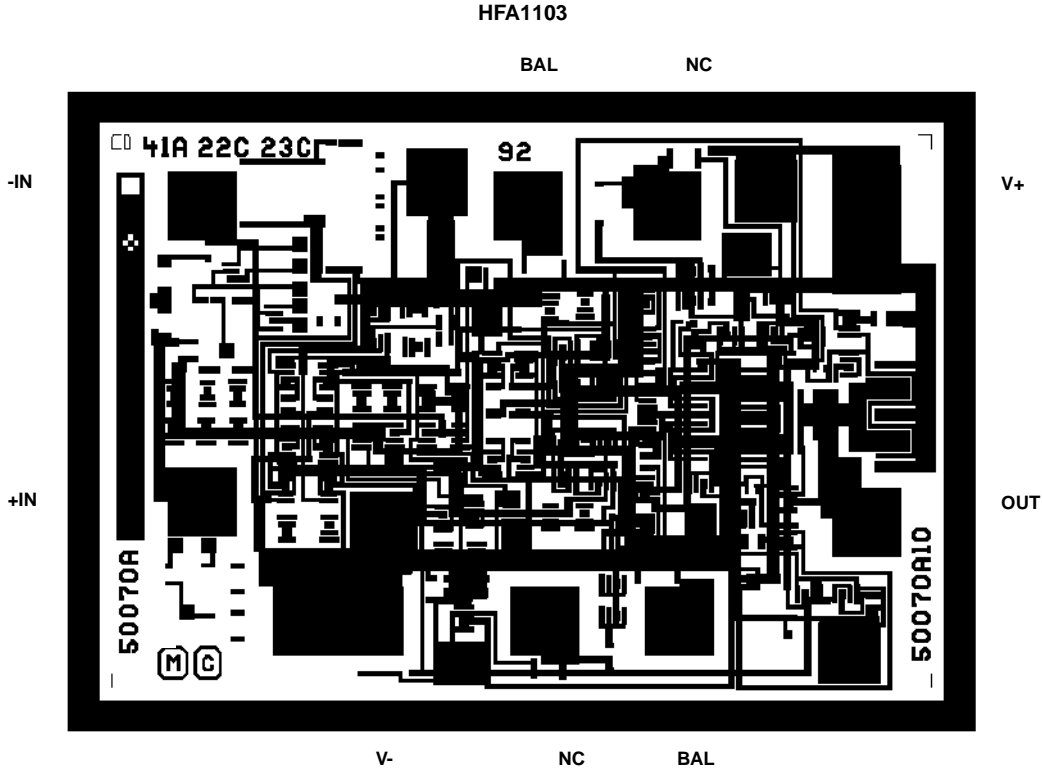
**PASSIVATION:**

Type: Nitride  
 Thickness: 4kÅ ±0.5kÅ

**TRANSISTOR COUNT:**

50

**Metallization Mask Layout**



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site [www.intersil.com](http://www.intersil.com)

**Sales Office Headquarters**

**NORTH AMERICA**

Intersil Corporation  
 P. O. Box 883, Mail Stop 53-204  
 Melbourne, FL 32902  
 TEL: (321) 724-7000  
 FAX: (321) 724-7240

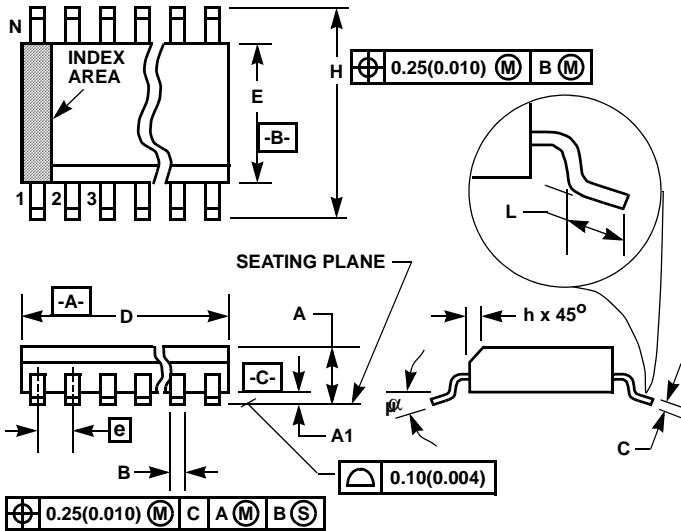
**EUROPE**

Intersil SA  
 Mercure Center  
 100, Rue de la Fusee  
 1130 Brussels, Belgium  
 TEL: (32) 2.724.2111  
 FAX: (32) 2.724.22.05

**ASIA**

Intersil (Taiwan) Ltd.  
 7F-6, No. 101 Fu Hsing North Road  
 Taipei, Taiwan  
 Republic of China  
 TEL: (886) 2 2716 9310  
 FAX: (886) 2 2715 3029

Small Outline Plastic Packages (SOIC)



**M8.15 (JEDEC MS-012-AA ISSUE C)**  
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
$\alpha$	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>