



T-79-08  
**CA3440A**  
**CA3440**

August 1991

**Nanopower BiMOS Operational Amp**

**Features**

- Standby Power at  $V+ = 5V$  ..... 300nW (Typ)
- Supply Current, BW, Slew Rate Programmable Using External Resistor
- Input Current ..... 10pA (Typ)
- 5V to 15V Supply
- Output Drives Typical Bipolar-Type Loads
- Low Cost 8-Lead Mini-DIP, TO-5

**Description**

The CA3440A and CA3440\* are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440A and CA3440 BiMOS op amps feature gate-protected PMOS transistors in the input circuit to provide very high input impedance and very low input current (10pA). These devices operate at total supply voltage from 5V to 15V and can be operated over the temperature range from  $-55^{\circ}C$  to  $+125^{\circ}C$ . Their virtues are programmability and very low standby power consumption (300nW). These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.5V below the negative supply terminals, an important attribute for single supply applications. The output stage uses MOS complementary source follower form which permits moderate load driving capability (10K $\Omega$ ) at very low total standby currents (50nA).

The CA3440A and CA3440 have the same 8-lead terminal pin-out used for "741" and other industry standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

These devices are supplied in either the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix).

\*Formerly Dev. Type No. TA10580.

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**Pinouts**

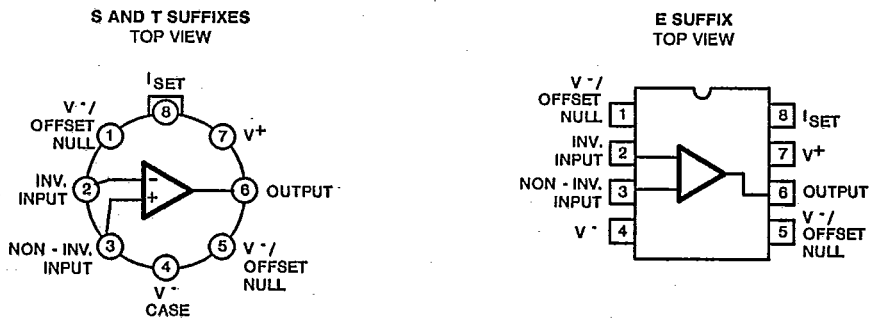


FIGURE 1.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
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**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY VOLTAGE  
 (BETWEEN  $V^+$  AND  $V^-$  TERMINALS) ..... 25 V  
 DIFFERENTIAL-MODE INPUT VOLTAGE .....  $\pm 9$  V  
 COMMON-MODE DC INPUT VOLTAGE ..... ( $V^+$  +8 V) to ( $V^-$  -0.5 V)  
 INPUT-TERMINAL CURRENT ..... 1 mA  
 DEVICE DISSIPATION:  
 WITHOUT HEAT SINK —  
 UP TO 55°C ..... 630 mW  
 ABOVE 55°C ..... Derate linearly 6.67 mW/°C  
 WITH HEAT SINK —  
 AT 125°C ..... 418 mW  
 BELOW 125°C ..... Derate linearly 16.7 mW/°C  
 TEMPERATURE RANGE:  
 OPERATING ..... -55 to +125°C  
 STORAGE ..... -65 to +150°C  
 OUTPUT SHORT-CIRCUIT DURATION ..... INDEFINITE  
 LEAD TEMPERATURE (DURING SOLDERING):  
 AT DISTANCE 1/16  $\pm$  1/32 IN. (1.59  $\pm$  0.79 MM) FROM CASE FOR 10 SECONDS MAX. .... +265°C

**TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE**

CHARACTERISTIC	TEST CONDITIONS $V^+=+5$ V; $V^-=-5$ V $R_{SET}=10$ M $\Omega$ ; $T_A=25^\circ$ C		CA3440A	CA3440	UNITS
Input Resistance, $R_i$			2	2	T $\Omega$
Input Capacitance, $C_T$			3.5	3.5	pF
Output Resistance, $R_o$			450	450	$\Omega$
Equivalent Input Noise Voltage, $e_n$	f = 1 kHz	$R_S=100$ $\Omega$	110	110	nV/ $\sqrt{Hz}$
	f = 10 kHz		110	110	
Short-Circuit Current Source IOM $^+$ To Opposite Supply Sink IOM $^-$			15	15	mA
			4.5	4.5	
Gain-Bandwidth Product, $f_T$			63	63	kHz
Slew Rate, SR			0.03	0.03	V/ $\mu$ s
Transient Response Rise Time, $t_r$ Overshoot	$R_L = 10$ k $\Omega$		5.6	5.6	$\mu$ s
	$C_L = 100$ pF		10	10	

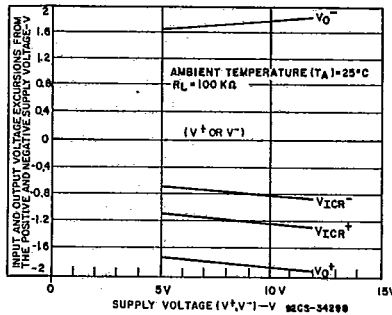


Fig. 1 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

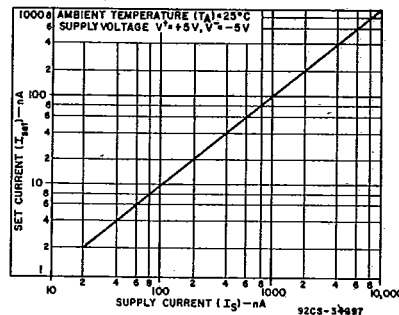


Fig. 2 - Set current versus supply current.

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ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V^+ = +5\text{ V}$ ,  $V^- = -5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  Unless Otherwise Specified,  $R_{SET} = 10\text{ M}\Omega$

CHARACTERISTIC	LIMITS						UNITS
	CA3440A			CA3440			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $ V_{IO} $	—	2	5	—	5	10	mV
Input Offset Current, $ I_{IO} $	—	2.5	20	—	2.5	30	pA
Input Current, $ I_{ij} $	—	10	40	—	10	50	pA
Large-Signal Voltage Gain, AOL ( $R_L = 10\text{ K}\Omega$ )	10K	100K	—	10K	100K	—	V/V
	80	100	—	80	100	—	dB
Common-Mode	—	100	320	—	100	320	$\mu\text{V/V}$
Rejection Ratio, CMRR	70	80	—	70	80	—	dB
Common-Mode Input $V_{ICR}^+$	+3.5	+3.7	—	+3.5	+3.7	—	V
Voltage Range, $V_{ICR}^-$	-5.0	-5.3	—	-5.0	-5.3	—	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V$	—	32	320	—	32	320	$\mu\text{V/V}$
	70	90	—	70	90	—	dB
Maximum Output Voltage, $V_{OM}^+$ $V_{OM}^-$	+3	+3.2	—	+3	+3.2	—	V
	-3	-3.2	—	-3	-3.2	—	
	—	—	—	—	—	—	
Supply Current, $I^+$	—	10	17	—	10	17	$\mu\text{A}$
Device Dissipation, $P_D$	—	100	170	—	100	170	$\mu\text{W}$
Input Offset Voltage Temperature Drift, $\Delta V_{IO}/\Delta T$	—	4	—	—	4	—	$\mu\text{V}/^\circ\text{C}$

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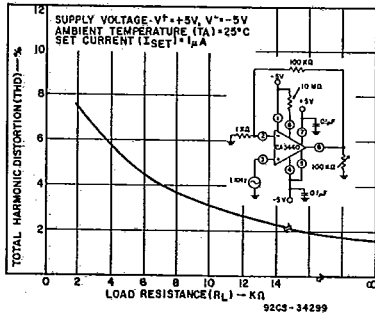


Fig. 3 - Total harmonic distortion percentage versus load resistance.

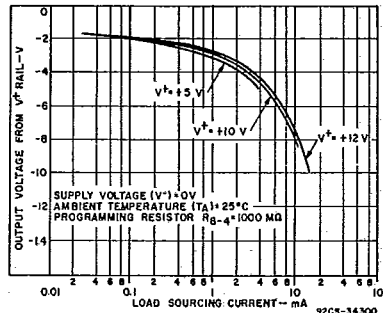


Fig. 4 - Output voltage versus sourcing load current.

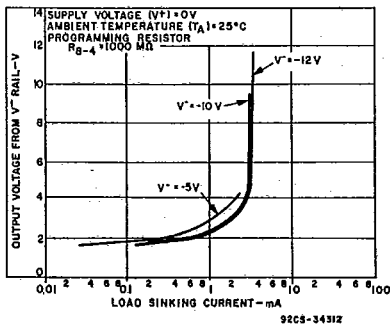


Fig. 5 - Output voltage versus sinking load current.

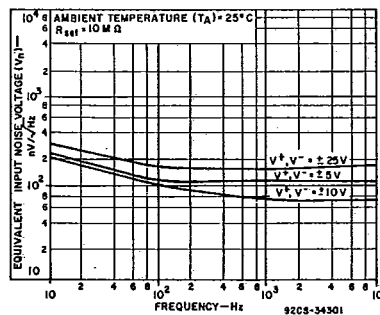


Fig. 6 - Input noise voltage versus frequency.

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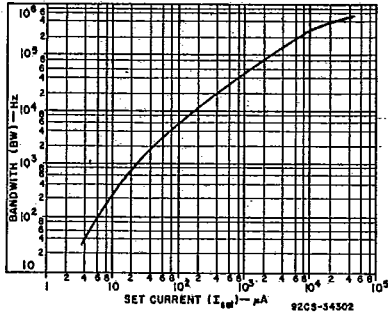


Fig. 7 - Bandwidth versus set current.

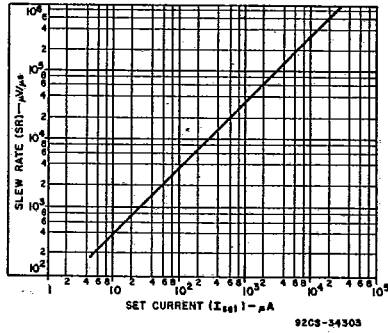
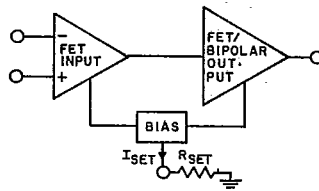


Fig. 8 - Slew rate versus set current.

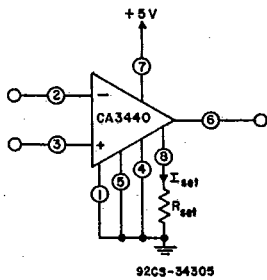


STAGE 1  
[HIGH GAIN  
100 db]

STAGE 2  
[BUFFER  
LOW Z  
OUTPUT]

92CS-34304

Fig. 9 - Nanopower op amp (supply current programmable using RSET) 1-pA typical input bias current, 4.0 to 15-volt supply.



92CS-34305

Fig. 10 - Nanopower op amp (usable standby power versus programming resistor RSET).

As RSET is increased, ISET and the standby power decrease while the BW/SR also decreases.

Operating at a +5 V single supply, the CA3440 exhibits the following characteristics:

RSET	Standby Power	BW	SR
1 MΩ	250 μW	164 kHz	0.17 V/μs
10 MΩ	25 μW	27 kHz	0.017 V/μs
100 MΩ	2.5 μW	2.6 kHz	.0017 V/μs
1000 MΩ	250 nW	78 Hz	0.00017 V/μs

The CA3440 is pin-compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the ISET terminal, must be returned to either ground or -V via RSET.

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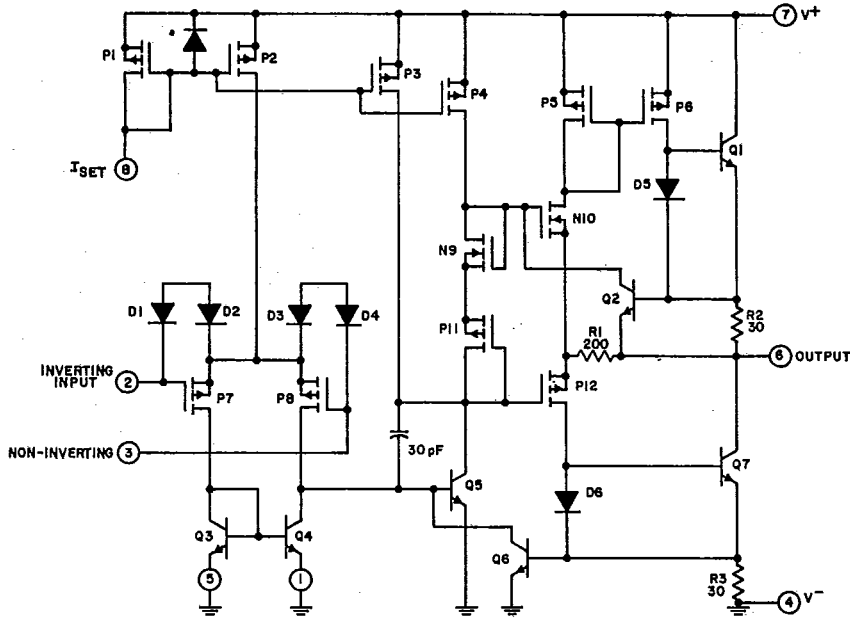
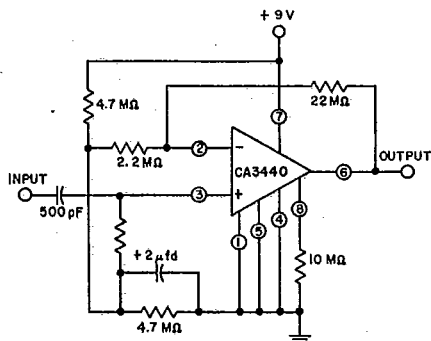


Fig. 11 - Schematic diagram for CA3440.

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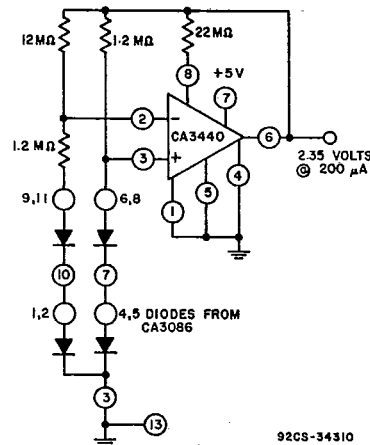
APPLICATIONS CIRCUITS



$R_{IN} > 20 \text{ M}\Omega$   
 STAND-BY POWER =  $90 \mu\text{W}$   
 GAIN = 20 dB  
 BW: 20-Hz TO 3-KHz  
 SR =  $0.016 \text{ V}/\mu\text{s}$

92CS-34309

Fig. 12 - High-input impedance amplifier.



92CS-34310

Fig. 13 - Micropower bandgap reference.