2.5A Output Current Opto-Compatible Single Channel Isolated IGBT Gate Driver with Active Protection Features

GENERAL DESCRIPTION

The SLMi333 isolated driver is an advanced opto-compatible single channel isolated IGTB gate driver with active protection features, such as desaturation detection, UVLO, isolated fault sensing and active miller clamp. The SLMi333 can provide 2.5A peak output current and it has auto-fault reset feature. The default desaturation threshold is 6.5V for devices without suffix H and 9V for devices with suffix H.

The input side supply operates from 3V to 18V and the output side supply allows for a range from 14V to 40V. All the supply voltage pins have under voltage lock-out (UVLO) protection.

An internal desaturation (DESAT) fault detection recognizes when the IGBT is in an overcurrent condition. When desaturation is active, a fault signal is sent across the isolation barrier, pulling the FAULT output at the input side low and blocking the isolator input. When the IGBT is turned off during normal operation with bipolar output supply, the output is clamp to VEE. If the output supply is unipolar, an active Miller clamp can be used, allowing Miller current to sink across a low impedance path, preventing IGBT to be dynamically turned on during high voltage transient conditions. The input side is isolated from output drivers by a 5kV$_{RMS}$ reinforced isolation barrier, with a minimum of 150kV/us common-mode transient immunity (CMTI).

FEATURES

- 2.5A source/sink output current
- Desaturation detection
- Miller clamping
- Soft turn-off during fault
- Fault automatic reset
- 80ns (Typ.) propagation delay
- 150kV/us (Min.) common mode transient immunity (CMTI)
- Input side supply range from 3V to 18V
- Output side supply range from 14 V to 40 V
- Pin to pin compatible to optocoupler isolated IGBT gate drivers
- SOP16W package with >8.0mm creepage and clearance
- Operating temperature: –40°C to +125°C
- Safety certifications:
  - 5kV$_{RMS}$ isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2011
  - DIN V VDE 0884-11 (Planned)

APPLICATION

- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial power supplies

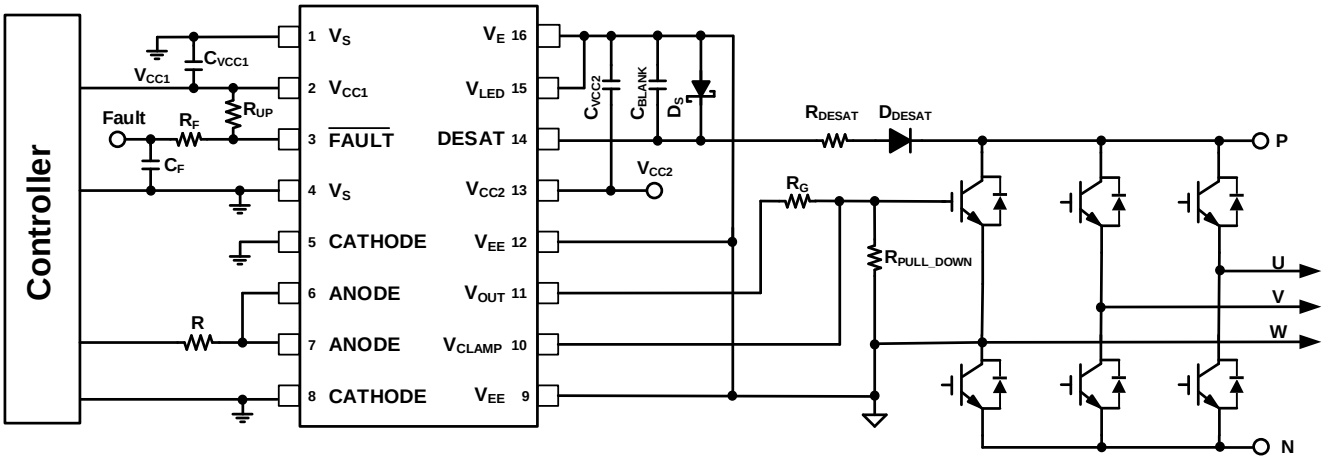

Figure 1. SLMi333 Application Circuit to Driver IGBT

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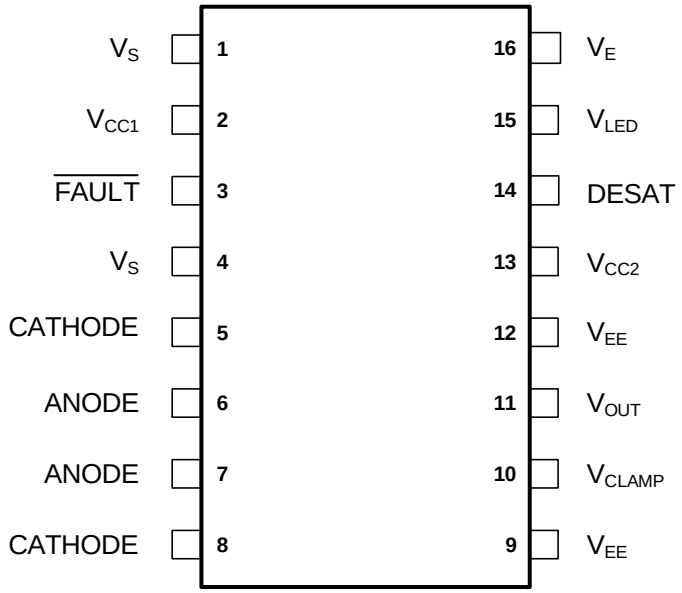
PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP16W	

PIN DESCRIPTION

No.	Pin	Description
1	V_S	Input ground
2	V_{CC1}	Positive Input supply voltage
3	$\overline{FAULT}$	Fault output. Open drain and active low.
4	V_S	Input ground
5	CATHODE	Cathode
6	ANODE	Anode
7	ANODE	Anode
8	CATHODE	Cathode
9	V_{EE}	Negative output supply voltage
10	V_{CLAMP}	Miller clamp
11	V_{OUT}	Gate drive voltage output
12	V_{EE}	Negative output supply voltage
13	V_{CC2}	Positive output supply voltage
14	DESAT	Desaturation voltage input. Connect to V_E if this pin is not in use.
15	V_{LED}	For internal test only. Suggest to connect it to V_{EE}
16	V_E	Common (IGBT emitter) output supply voltage

FUNCTIONAL BLOCK DIAGRAM

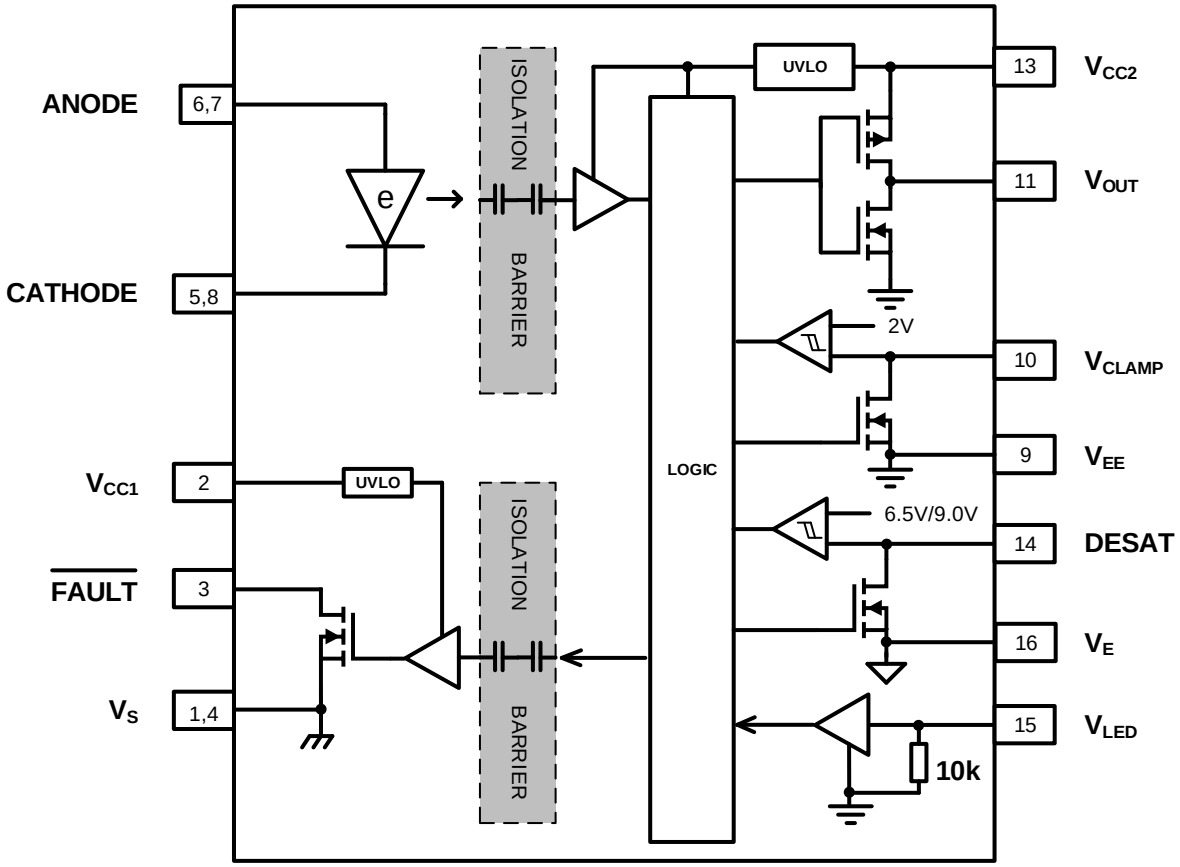


Figure 2. SLMi333 Block Diagram

ORDERING INFORMATION

Order Part No.	DESAT Threshold	Package	QTY
SLMi333CG-DG	6.5V	SOP16W, Pb-Free	1500/Reel
SLMi333HCG-DG	9.0V	SOP16W, Pb-Free	1500/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Units
$I_{F(AVG)}$	Average Input Current		25	mA
V_R	Reverse Input Voltage		30	V
V_{CC1} -V_S	Input Side Supply Voltage	-0.5	20	V
V_{CC2} -V_{EE}	Output Supply Voltage	-0.5	45	V
V_E -V_{EE}	Negative Output Supply Voltage	-0.5	20	V
V_{CC2} -V_E	Positive Output Supply Voltage	-0.5	45-(V_E -V_{EE})	V
V_{DESAT}	DESAT Voltage	V_E-0.5	Min(V_E+20, V_{CC2})	V
V_{CLAMP} - V_{EE}	Miller Clamping Voltage	-0.5	45	V
V_{FAULT} - V_S	Fault pin Voltage	-0.5	20	V
V_{OUT}	V_{OUT} pin Voltage	V_{EE}	V_{CC2}	V
T_J	Junction Temperature	-40	150	°C
T_S	Storage Temperature	-55	150	

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Max	Units
V_{CC1} -V_S	Input Side Supply Voltage	3	18	V
V_{CC2} -V_{EE}	Output Supply Voltage	14	40	V
V_E-V_{EE}	Negative Output Supply Voltage	0	15	V
V_{CC2} -V_E	Positive Output Supply Voltage	14	40-(V_E -V_{EE})	V
I_F(ON)	Input Diode Forward Current (Diode “ON”)	7	16	mA
V_F(OFF)	Anode Voltage - Cathode Voltage (Diode “OFF”)	-30	0.9	V
T_J	Junction Temperature	-40	150	°C
T_A	Ambient Temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±3000	V
	CDM	±1500	V

THERMAL INFORMATION[1]

Symbol	Definition	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	100	°C/W
$R_{\theta JC(TOP)}$	Junction to case (top) thermal resistance	40	°C/W

Note1: Standard JESD51-3 low effective thermal conductivity test board.

PACKAGE SPECIFICATIONS

Symbol	Definition	Min	Typ	Max	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		1.6		pF
C_{IN}	Input Capacitance		30		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value	Units
CLR	External clearance	Shortest terminal to terminal distance through air	8.0	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	8.0	mm
DTI	Distance through the insulation	Minimum internal gap	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	V
	Material Group		I	
	Overvoltage category	Rated mains voltages ≤600Vrms	I-IV	
		Rated mains voltages ≤1000Vrms	I-III	
DIN V VDE 0884-11(1)				
V_{IORM}	Maximum repetitive peak isolation voltage		1414	V_{PK}
V_{IOWM}	Maximum isolation working voltage		1000	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage	60s	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.6 x V_{IOSM}	6250	V_{PK}
q_{pd}	Apparent charge	Method b2: $V_{pd(m)}$=1.875 x V_{IORM}, tm=1 s	≤5	pC
	Climatic Category		40/125/21	
	Pollution Degree		2	
UL1577				
V_{ISO}	Withstand Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	5000	V_{RMS}

Note 1: Certification planned

SAFETY RELATED CERTIFICATIONS

VDE (planned)	**UL**	**CQC**
DIN V VDE 0884011-11: 2017-01	UL 1577 component recognition program	Certified according to GB4943.1-2011
Reinforced Insulation	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude≤ 5000m, Tropical climate, 400 V_{RMS} maximum working voltage
Certification Planned	File number: E521801	File number: CQC21001324484

SAFETY LIMITING VALUES

Symbol	**Parameter**	**Condition**	**Value**	**Unit**
I_S	Safety input, output, or supply current	$R_{\theta JA}$=100°C/W, V_{CC2}-V_{EE} = 15V, T_J =150°C, T_A =25°C	83.3	mA
		$R_{\theta JA}$=100°C/W, V_{CC2}-V_{EE} = 30V, T_J =150°C, T_A =25°C	41.6	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=100°C/W, T_J =150°C, T_A =25°C	1250	mW
T_S	Maximum safety temperature		150	°C

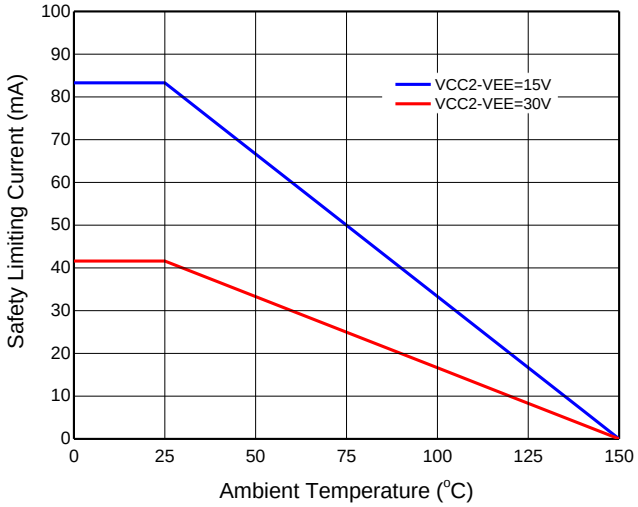


Figure 3. Thermal Derating Curve for Limiting Current per VDE

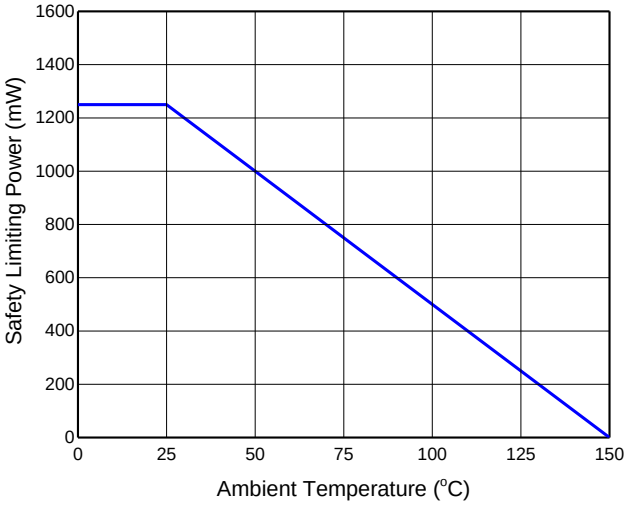


Figure 4. Thermal Derating Curve for Limiting Power per VDE

ELECTRICAL CHARACTERISTICS (DC)

All typical values at V_{CC2}-V_{EE} = 15V, V_{EE} -V_{EE} = 0V and T_A = 25°C unless otherwise specified. All min and max specifications are at recommended operating conditions and T_A = -40°C to 125°C.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
INPUT						
I_{FLH}	Input Forward Threshold Current Low to High			2.2		mA
V_F	Input Forward Voltage	I_F=10mA		2.2		V
$\Delta V_F/\Delta T$	Temp Coefficient of Input Forward Voltage	I_F=10mA		0.5		mV/°C
V_R	Input Reverse Breakdown Voltage	I_R=10uA	30			V
V_{CLAMP}	Clamp Pin Threshold Voltage			2.0		V
V_{DESAT}	DESAT Threshold	Without suffix H		6.5		V
		With suffix H		9		V
I_{CHG}	DESAT Blank Charging Current	V_{DESAT}=2V		0.22		mA
I_{DSCHG}	DESAT Blank Discharging Current	V_{DESAT}=7V		33		mA
V_{FT_LOW}	FAULT Output Low Voltage	I_{FAULT}=1mA, V_{CC1}=5V		0.1		V
I_{FT_LK}	FAULT Pin Leakage Current	V_{FAULT}=5V, V_{CC1}=5V		0.1		uA
OUTPUT						
I_{OH}	High Level Peak Output Current	I_F=10mA, C_{VCC2}=10uF, C_{LOAD}=220nF		2.5		A
I_{OL}	Low Level Peak Output Current	I_F=10mA, C_{VCC2}=10uF, C_{LOAD}=220nF		2.5		A
I_{CL}	Clamp Low Sink Current			1.67		A
I_{OLF}	Low Level Output Current During Fault Condition			0.19		A
V_{OH}	High Level Output Voltage	I_F=10mA, I_O=-20mA		60		mV
V_{OL}	Low Level Output Voltage	V_F=0V, I_O=20mA		30		mV
UNDER VOLTAGE LOCKOUT						
V_{UVLO1_R}	Under Voltage Lockout Rising on V_{CC1}			2.7		V
V_{UVLO1_F}	Under Voltage Lockout Falling on V_{CC1}			2.5		V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{UVLO1_HYS}	Under Voltage Lockout Hysteresis on V_{CC1}			0.2		V
V_{UVLO2_R}	Under Voltage Lockout Rising on V_{CC2}		10.5	11.6	12.5	V
V_{UVLO2_F}	Under Voltage Lockout Falling on V_{CC2}		9.2	10.3	11.1	V
V_{UVLO2_HYS}	Under Voltage Lockout Hysteresis on V_{CC2}			1.3		V

SWITCHING CHARACTERISTICS (AC)

All typical values at V_{CC2}-V_{EE} = 15V, V_{EE} -V_{EE} = 0V and T_A = 25°C unless otherwise specified. All min and max specifications are at recommended operating conditions and T_A = -40°C to 125°C.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation delay, Low to High	C_{LOAD}=1nF, f_{sw}=20kHz, (50% Duty Cycle), V_{CC2}=15V		80	120	ns
t_{PHL}	Propagation delay, High to Low			80	120	ns
t_r	Turn on rise time				28	ns
t_f	Turn off fall time				25	ns
t_{PWD}	Pulse Width Distortion				35	ns
t_{UVLO_REC}	UVLO Recovery Delay	V_{CC2} Rising from 0V to 15V			30	us
$t_{DESAT(90\%)}$	DESAT to 90% V_{OUT} Delay	C_{BLANK}=100pF, C_{LOAD}=10nF		0.15		us
$t_{DESAT(10\%)}$	DESAT to 10% V_{OUT} Delay			0.5		us
$t_{DESAT(MUTE)}$	DESAT Input Mute			23		us
$t_{DESAT(LOW)}$	DESAT to DESAT Low Propagation Delay			0.2		us
$t_{DESAT(FAULT)}$	DESAT to FAULT Low Delay			0.3		us
$t_{RESET(FAULT)}$	RESET to High Level FAULT Signal Delay			1		us
$CMTI_H$	Output High Level Common Mode Transient Immunity	I_F=10mA, V_{CM}=1000V, V_{CC2}=15V, T_A=25°C	150			kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_F=0V, V_{CM}=1000V, V_{CC2}= 15V, T_A=25°C	150			kV/us

PARAMETER MEASUREMENT INFORMATION

Propagation Delay, Rise Time and Fall Time

Figure 5 shows the circuit used to measure the rise (t_r)and fall(t_f) times, and the propagation delays t_{PDLH} and t_{PDHL}.

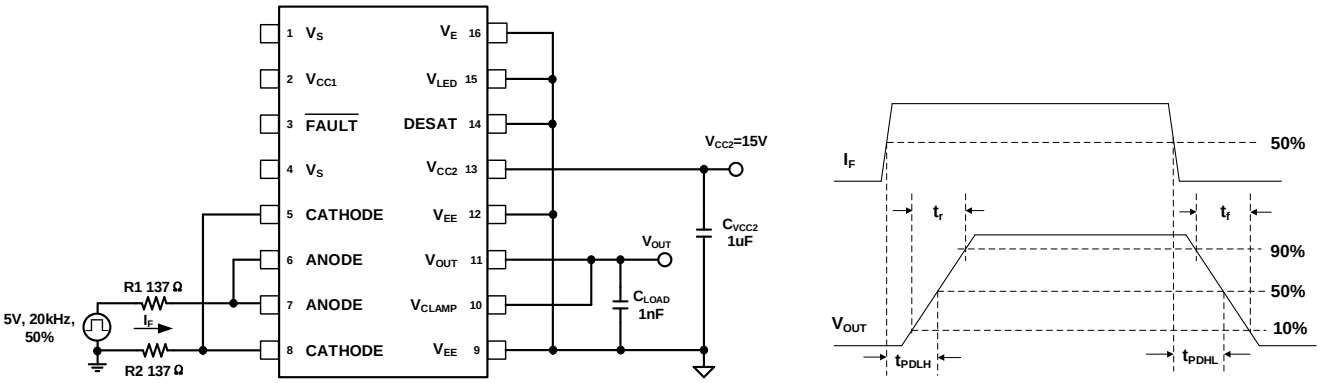


Figure 5. Propagation Delay, Rise Time and Fall Time

CMTI Testing

Figure 6 is the simplified diagram of the CMTI testing for V_{OUT}. Common mode voltage is set to 1000V. The test is performed with V_{OUT} is High and V_{OUT} is Low.

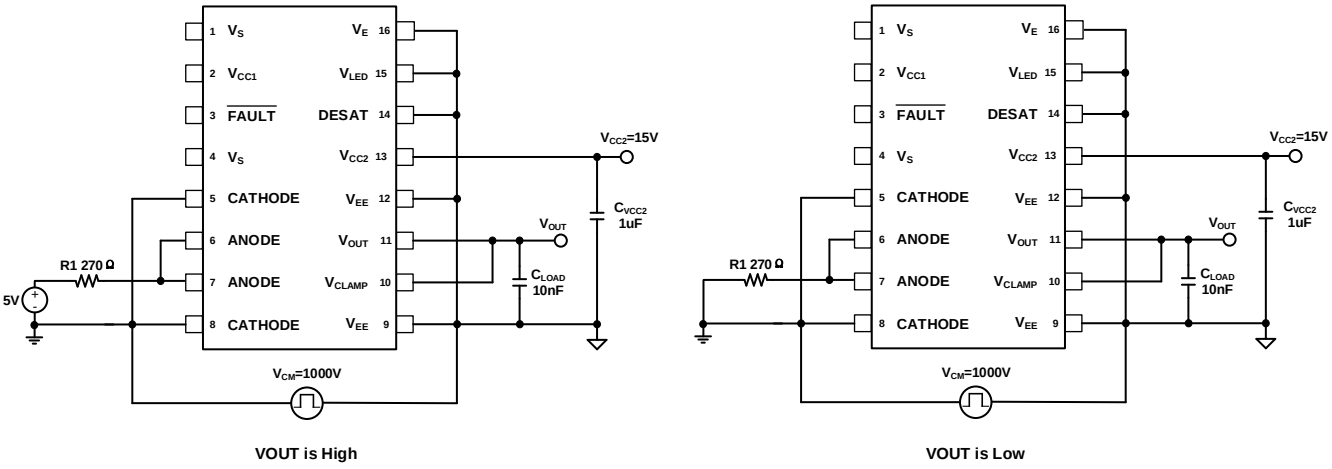


Figure 6. CMTI Test of V_{OUT}

Figure 7 is the simplified diagram of the CMTI testing for FAULT. Common mode voltage is set to 1000V. The test is performed with FAULT is High and FAULT is Low.

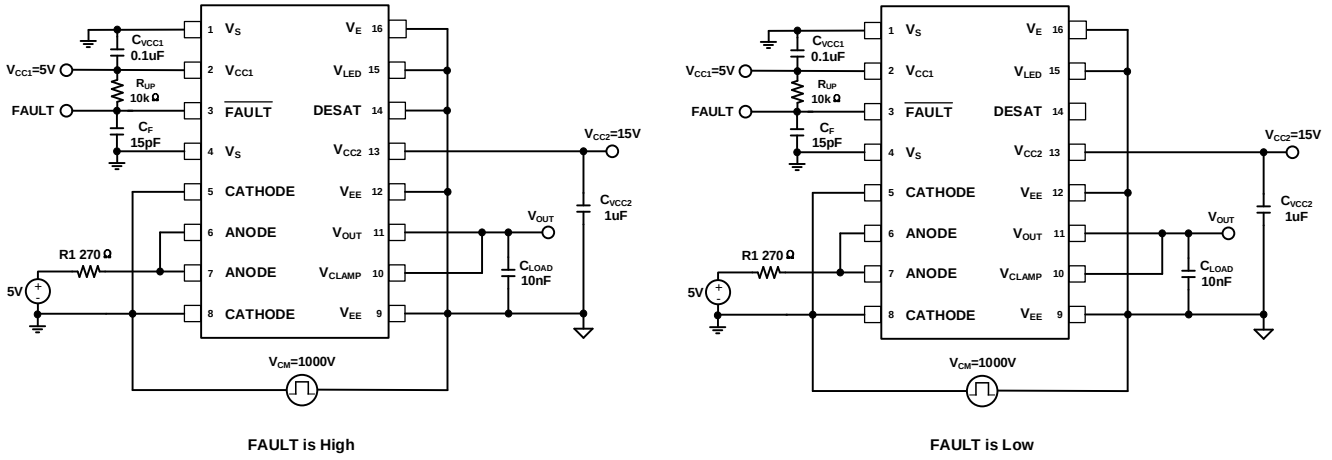


Figure 7. CMTI Test of FAULT

FEATURE DESCRIPTION

The SLMi333 is an advanced opto-compatible single channel isolated gate driver with rich protection features, such as desaturation detection, miller clamp, isolated fault sensing and under voltage lockout.

Desaturation Detection

The DESAT pin monitors the IGBT V_{CE} voltage. When the voltage on the DESAT pin exceeds DESAT threshold (6.5V for without suffix H and 9V for with suffix H) while the IGBT is on, a weak pull down circuit (I_{OLF})in the output driver stage will turn on to ramp down the V_{OUT} slowly and "softly" turn off the IGBT. This "softly" turn-off feature prevents large di/dt which induces high voltage spikes to damage the IGBT. The V_{CLAMP} pin should be connected to V_{OUT} pin in order to use the soft turn-off feature.

A blank time is needed in the DESAT detection circuit following the turn on of the IGTB to allow the collector voltage to fall below the DESAT threshold. The blank time is controlled by the internal DESAT blank charge current, the DESAT voltage threshold, and the external DESAT capacitor. Using the following equation to calculate the blank time.

$$t_{BLANK} = \frac{C_{BLANK} \times V_{DESAT}}{I_{CHG}}$$

Here:

t_{BLANK}: Blank time

C_{BLANK}: External DESAT capacitor

V_{DESAT}: DESAT voltage threshold

I_{CHG}: DESAT blank charging current

During the IGBT turn on, high negative spike voltage occurs on the collection of the IGBT due to parasitic parameters and this negative spike may damage the DESAT pin. In order to protect the DESAT pin in such case, a resistor, R_{DESAT}, is needed to in series with the DESAT diode. The value of the RDESAT depends on the different application, but generally a 100Ω resistor is recommended.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to VE potential at low-voltage levels.

Fault Sensing

The SLMi333 integrates isolated fault indication. When the DESAT has monitored a fault on the IGTB, it also activates an internal feedback channel which pull low the $\overline{\text{FAULT}}$ pin in the input side to inform the fault condition to a micro-controller. In the meanwhile, all input control signals will be ignored during the fixed mute time to allow the driver to completely soft shutdown the IGBT.

The SLMi333 will reset the $\overline{\text{FAULT}}$ pin automatically after the fixed mute time, $t_{DESAT(MUTE)}$. After the fixed mute time, the V_{OUT} is controlled by the input control signal.

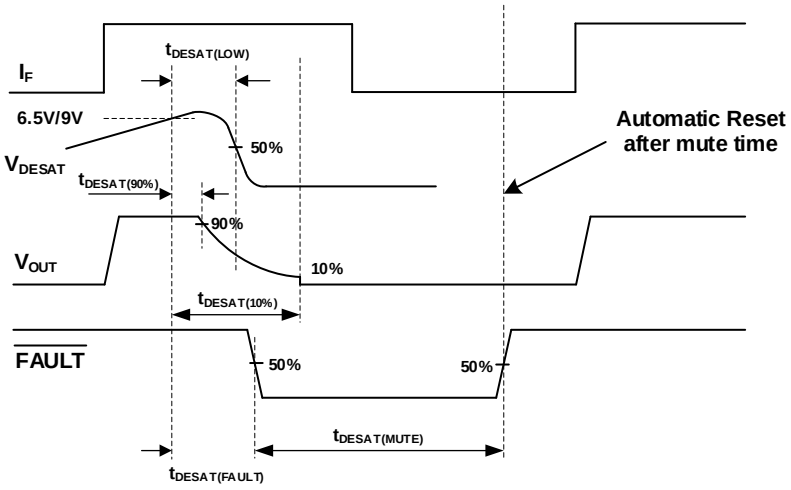


Figure 8. Fault Timing with Automatic Reset

Miller Clamp

A Miller clamp circuit integrates in the SLMi333 which allows the control of the Miller current during a high dV/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn off, the gate voltage is monitored through the V_{CLAMP} pin and the clamp circuit is activated when the voltage on the V_{CLAMP} pin goes below the clamp voltage threshold (2V typical, relative to V_{EE}). A clamp low sink current is generated when the clamp circuit is activated. The clamp circuit is disabled when the input on signal is triggered again.

Under Voltage Lockout

The under voltage lockout (UVLO) feature on the V_{CC2} is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the SLMi333 output low. When the voltage on the V_{CC2} is lower than the under voltage lockout falling threshold on V_{CC2}, the output is clamp to V_{EE}. When the voltage on the V_{CC2} is higher than the under voltage lockout rising threshold on V_{CC2}, the output is allowed to turn on according to the input signal if no other faults happens.

The under voltage lockout feature on the V_{CC1} only effects the $\overline{FAULT}$ pin function. If the voltage on the V_{CC1} is below the UVLO threshold, the $\overline{FAULT}$ can't be pulled low.

The Table 1 shows the relationship between I_F, UVLO, DESAT function, fault and V_{OUT}.

Table 1. Relationship between Input and Output

I_F	**UVLO on V_{CC2}**	**DESAT Function**	FAULT	**V_{OUT}**
ON	Active	Not active	High	Low
ON	Not active	Active with DESAT fault	Low	Low
ON	Not active	Active without DESAT fault	High	High
OFF	Active	Not active	High	Low
OFF	Not active	Not active	High	Low

Layout

In order to achieve optimum performance for the SLMi333, some suggestions on the PCB layout.

Component placement:

- Low ESR capacitors must be connected close to the device between the V_{CC2} and V_{EE} pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the V_{EE} pins connected to the switch node, the parasitic inductances between the source of the top transistor and the drain of the bottom transistor must be minimized.

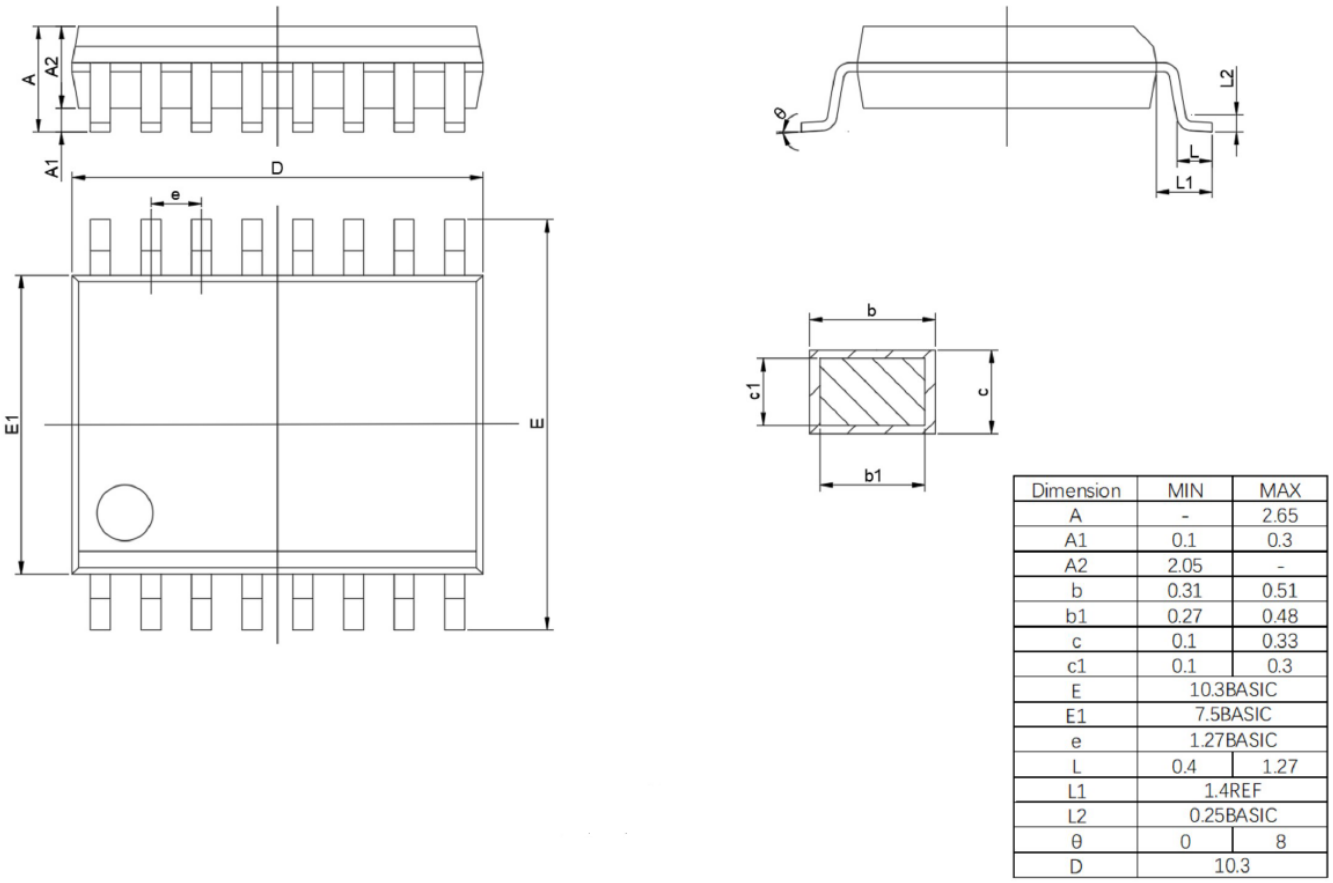
Grounding considerations:

- Limiting the high peak currents trace loop that charge and discharge the transistor gates to a minimal physical area is essential. Small trace loop decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

High voltage considerations:

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

PACKAGE CASE OUTLINES



Dimension	MIN	MAX
A	-	2.65
A1	0.1	0.3
A2	2.05	-
b	0.31	0.51
b1	0.27	0.48
c	0.1	0.33
c1	0.1	0.3
E	10.3BASIC	
E1	7.5BASIC	
e	1.27BASIC	
L	0.4	1.27
L1	1.4REF	
L2	0.25BASIC	
θ	0	8
D	10.3	

Figure 9. SOP16W Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: Mar/2022	
Whole document	Initial release
Rev 1.1 datasheet: Sep/2022	
Page 6	Add thermal information
Page 7	Add the test condition in the Insulation specifications
Page 8	Add safety related certifications and safety limiting values