Buck 2A, 2-Channel Power Management IC

General Description

The LP6312 is a 2A buck converter of 2-CH power management IC for applications powered by one Li-Ion battery or a DC 5V adapter. It integrates four synchronous buck converters and can provide high efficiency output at light load and heavy load operation. The internal compensation architecture simplifies the application circuit design. Besides, the independent enable control makes the designer have the greatest flexibility to optimize timing for power sequencing purposes.

The LP6312 is available in a 10 pin DFN-10 package.

Features

- 2.5V to 5.5V Input Voltage Range
- Two Buck Converters
- Output Voltage Range: 0.6V to Vin
- Continuous Loading: 2A (Buck1), 2A (Buck2)
- Fixed 1.5MHz Switching Frequency
- 100% Duty Cycle Low Dropout Operation
- <1uA Shutdown Current
- Independent Enable Control
- Internal Compensation
- Cycle-by-Cycle Current Limit
- Short Circuit Protection
- Auto Recovery OTP Protection
- Available in 10-pin DFN Package

Order Information

LP6312 □ □□ □

- □ (VOUT Type): A: Adjustable
- □□ (Package Type): QV: DFN-10
- □: F: Pb/Halogen-Free

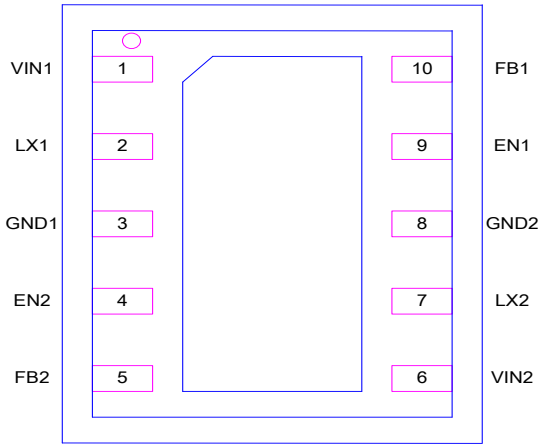
Marking Information

Device	Marking	Package	Shipping
LP6312AQVF	LPS LP6312 YWX	DFN3X3	5K/REEL
Marking indication: Y:Production year W:Production week X:Production batch			

Applications

- Smart Phone
- IP Camera
- OTT
- Digital Camera

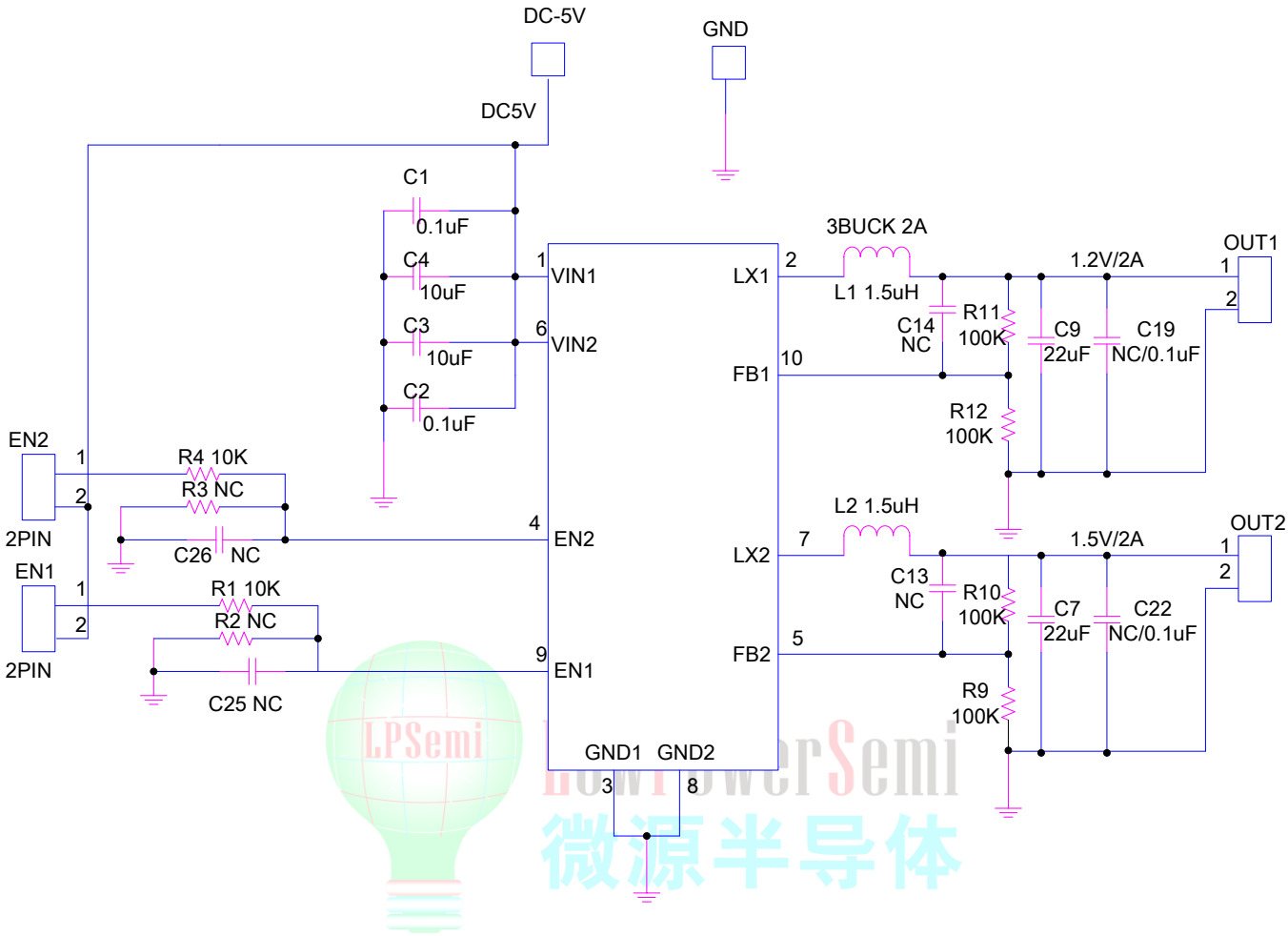
Functional Pin Description

Package Type	Pin Configurations
DFN-10	

Pin Description

Pin	Name	Description
1	VIN1	Supply Input Power.
2	LX1	Switch Mode Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
3	GND1	Common Ground.
4	EN2	Chip Enable.
5	FB2	Feedback Reference Voltage Pin.
6	VIN2	Supply Input Power.
7	LX2	Switch Mode Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
8	GND2	Common Ground.
9	EN1	Chip Enable.
10	FB1	Feedback Reference Voltage Pin.

Application Circuit



Absolute Maximum Ratings Note 1

- ✧ Input Voltage (VIN1, VIN2) ---------- -0.3V to +6.5V
- ✧ LX Pin Voltage (VLX1, VLX2) ---------- -0.3V to V_{INX}+0.3V
- ✧ All Other Pins Voltage ---------- -0.3V to V_{INX}+0.3V
- ✧ Ambient Temperature operating Range (T_A) ---------- -40°C to 85°C
- ✧ Maximum Junction Temperature (T_{J_MAX}) ---------- 150°C
- ✧ Lead Temperature (Soldering, 10 sec) ---------- 260°C
- ✧ Storage Temperature Range (T_S) ---------- -60°C to 125°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics

- ✧ DFN -10 Thermal Resistance (θ_{JC}) ---------- 7.5°C/W
- ✧ DFN -10 Thermal Resistance (θ_{JA}) ---------- 65°C/W
- ✧ DFN -10 Power Dissipation at T_A=25°C (P_{D_MAX}) ---------- 1.5W

Recommended Operating Conditions

- ✧ Input Voltage (VIN1, VIN2) ---------- 2.5V to +5.5V
- ✧ Junction Temperature Range (T_J) ---------- -40°C to +125°C

ESD Susceptibility

- ✧ HBM(Human Body Mode) ---------- 2KV
- ✧ MM(Machine Mode) ---------- 200V

Electrical Characteristics

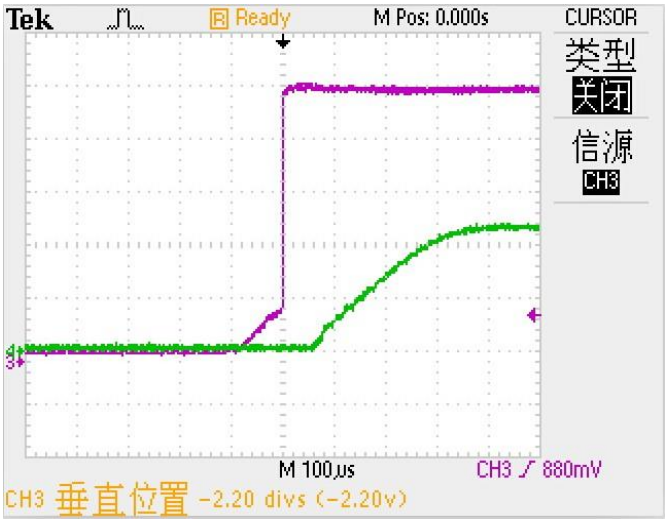
(V_{INX}=3.6V, V_{CC}=3.6V, T_A=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Supply Voltage						
Input Voltage	V_{INX}		2.5		5.5	V
Control Circuit Input Voltage	V_{CC}		2.5		5.5	V
Buck Converter 1, 2						
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		0.1	1	μA
Quiescent Current	I_Q	Non-switching, No Load		70		μA
UVLO Threshold	V_{UVLO}	V_{IN} Rising	1.8	2	2.2	V
UVLO Hysteresis	$V_{UV-HYST}$			0.2		V
Output Load Current	I_{LOAD}		2			A
Reference Voltage	V_{REF}		0.588	0.6	0.612	V
Switching Frequency	F_{SW}	I_{LOAD} = 100mA		1.5		MHz
PMOS Current Limit	I_{LIM-P}		3			A
PMOS On-Resistance	$R_{DS(ON)-P}$	I_{LOAD} = 100mA		100		mΩ
NMOS On-Resistance	$R_{DS(ON)-N}$	I_{LOAD} = 100mA		90		mΩ
Enable Pin Input Low Voltage	V_{EN-L}				0.4	V
Enable Pin Input High Voltage	V_{EN-H}		1.4			V
Maximum Duty Cycle	D_{MAX}		100			%
Thermal Shutdown						
Thermal Shutdown Threshold	T_{OTP}			150		℃
Thermal Shutdown Hysteresis	T_{HYST}			20		℃

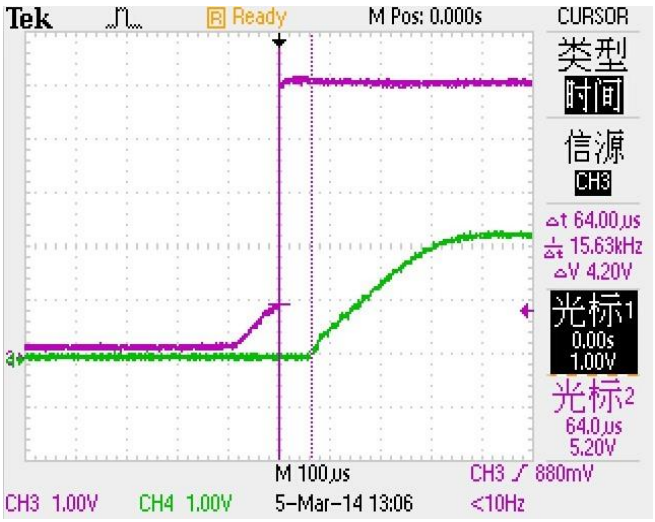
Note:

1. MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.
2. Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

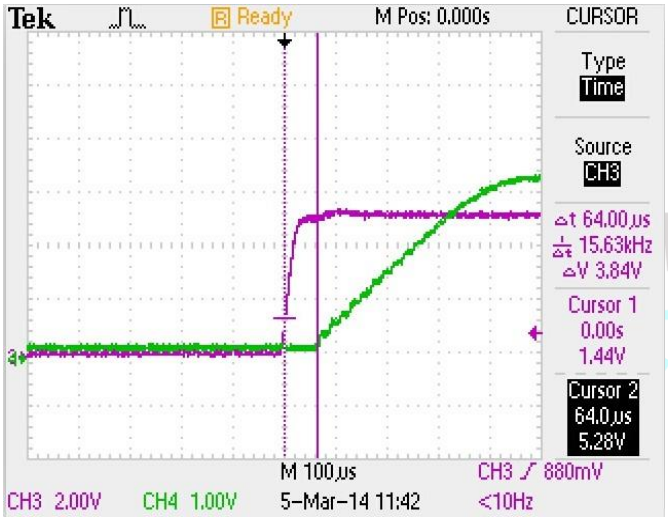
Typical Operating Characteristics



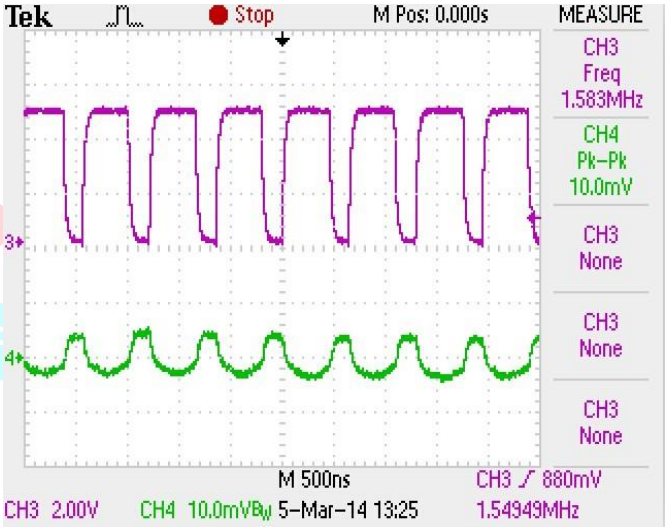
V_{IN}=5V V_{OUT}=3.3V



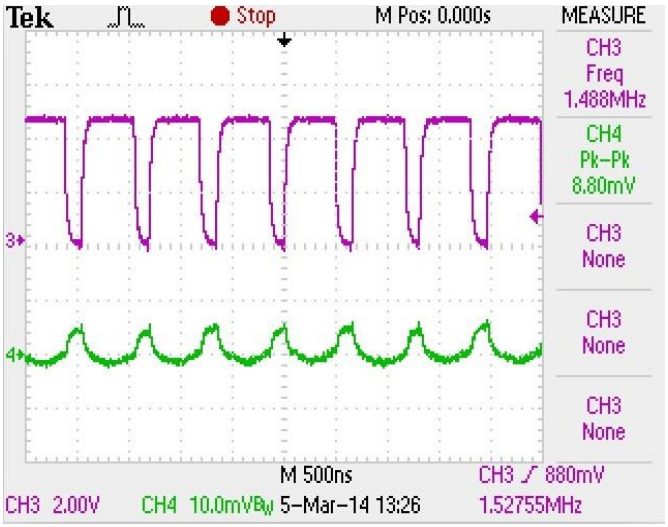
V_{IN}=5V V_{OUT}=3.3V



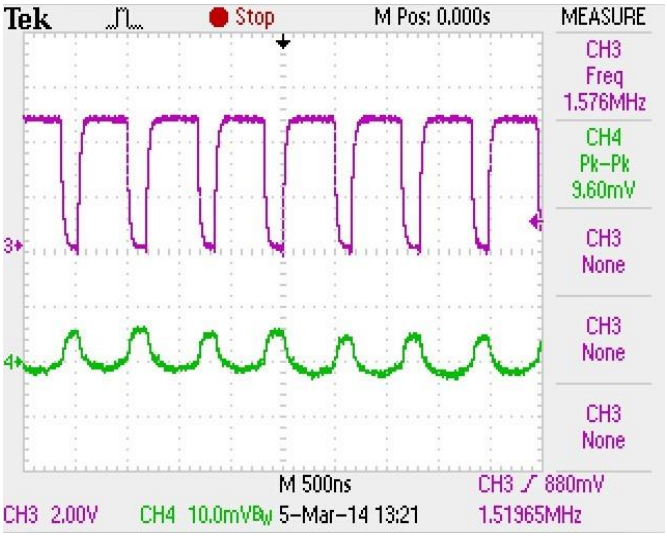
V_{IN}=5V V_{OUT}=3.3V



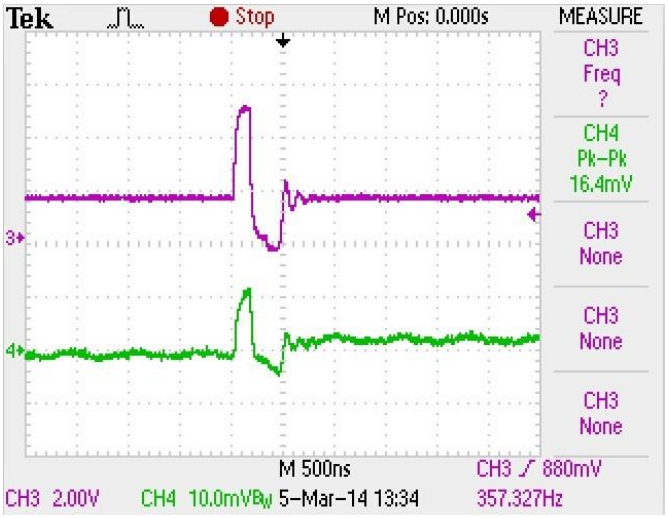
V_{IN}=5V V_{OUT}=3.3V/2A



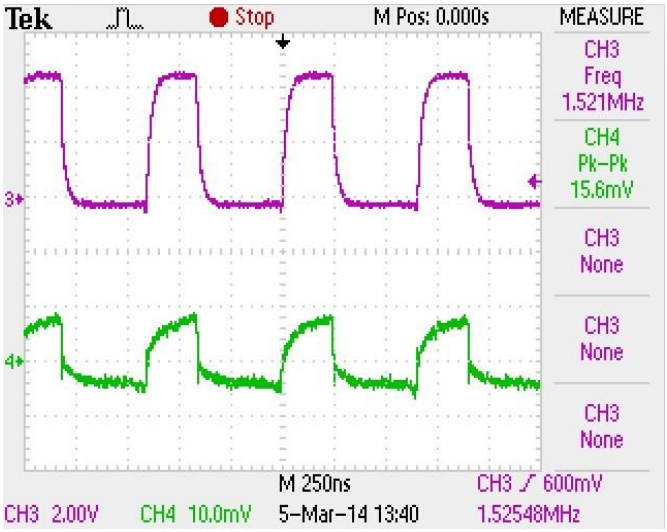
V_{IN}=5V V_{OUT}=3.3V/1A



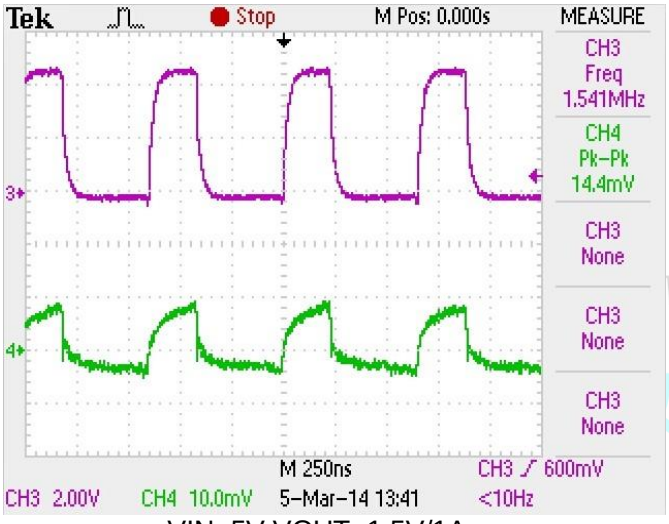
V_{IN}= 5V V_{OUT}=3.3V/1.5A



V_{IN}=5V V_{OUT}=1.5V



V_{IN}=5V V_{OUT}=1.5V/2A



VIN=5V VOUT=1.5V/1A

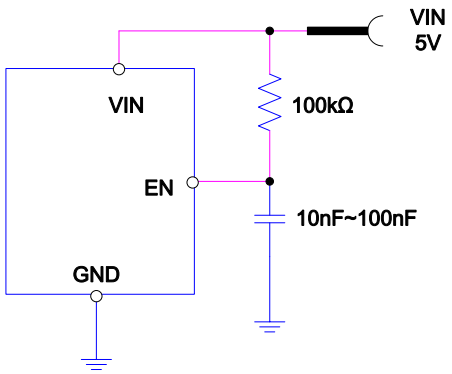
Functional Description

PFM/PWM Operation

Each of the buck regulators can be operated at PFM/PWM mode. If the output current is less than 150mA (typ.), the regulators automatically enters the PFM mode. The output voltages and output ripples at PFM mode are higher than the output voltages and output ripples at PWM mode. But at very light load, the PFM mode operation provides higher efficiency than PWM mode operation.

Enable Control

The LP6312 is a high efficiency Power Management IC which is designed for IPC and OTT applications. It incorporates four 2A synchronous buck regulators and can be controlled by individual EN pins. The start-up time for each channel can be programmed by using the circuit shown as below:



Over Current Protection

The LP6312 internal four regulators have their own cycle-by-cycle current limit circuits. When the inductor peak current exceeds the current limit threshold, the output voltage starts to drop until FB pin voltage is below the threshold, typically 30% below the reference.

Thermal Shutdown

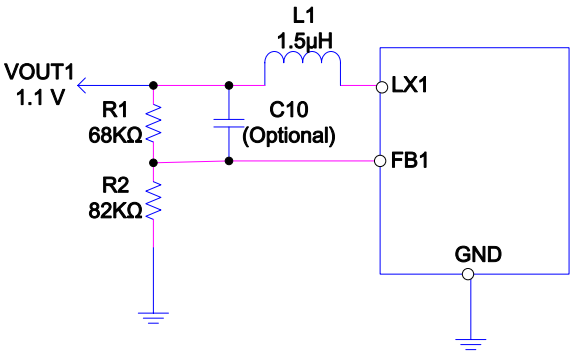
The LP6312 will automatically disable if the die temperature is higher than the thermal shutdown threshold point. To avoid unstable operation, the hysteresis of thermal shutdown is about 20°C.

Application Information

Output Voltage Setting

Each of the regulators output voltage can be set via a resistor divider (ex. R1, R2). The output voltage is calculated by following equation:

$$V_{OUT1} = 0.6 \times \frac{R1}{R2} + 0.6\ V$$



The following table lists common output voltage and the corresponding R1, R2 resistance value for reference.

V_{OUT}	R1	R2	Tolerance
3.3V	510KΩ	110KΩ	1%
1.8V	200KΩ	100KΩ	1%
1.5V	150KΩ	100KΩ	1%
1.1V	68KΩ	82KΩ	1%

Output Inductor Selection

The output inductor selection mainly depends on the amount of ripple current through the inductor ΔI_L. Large ΔI_L will cause larger output voltage ripple and loss, but the user can use a smaller inductor to save cost and space. On the contrary, the larger inductance can get smaller ΔI_L and thus the smaller output voltage ripple and loss. But it will increase the space and the cost. The inductor value can be calculated as:

$$L = \frac{V_{PWR} - V_{OUT}}{\Delta I_L \times F_{SW}} \times \frac{V_{OUT}}{V_{PWR}}$$

For most applications, 1.0uH to 4.7uH inductors are suitable for LP6312

Power Dissipation

The total output power dissipation of LP6312 should not to exceed the maximum 5W range. The total output power dissipation can be calculated as:

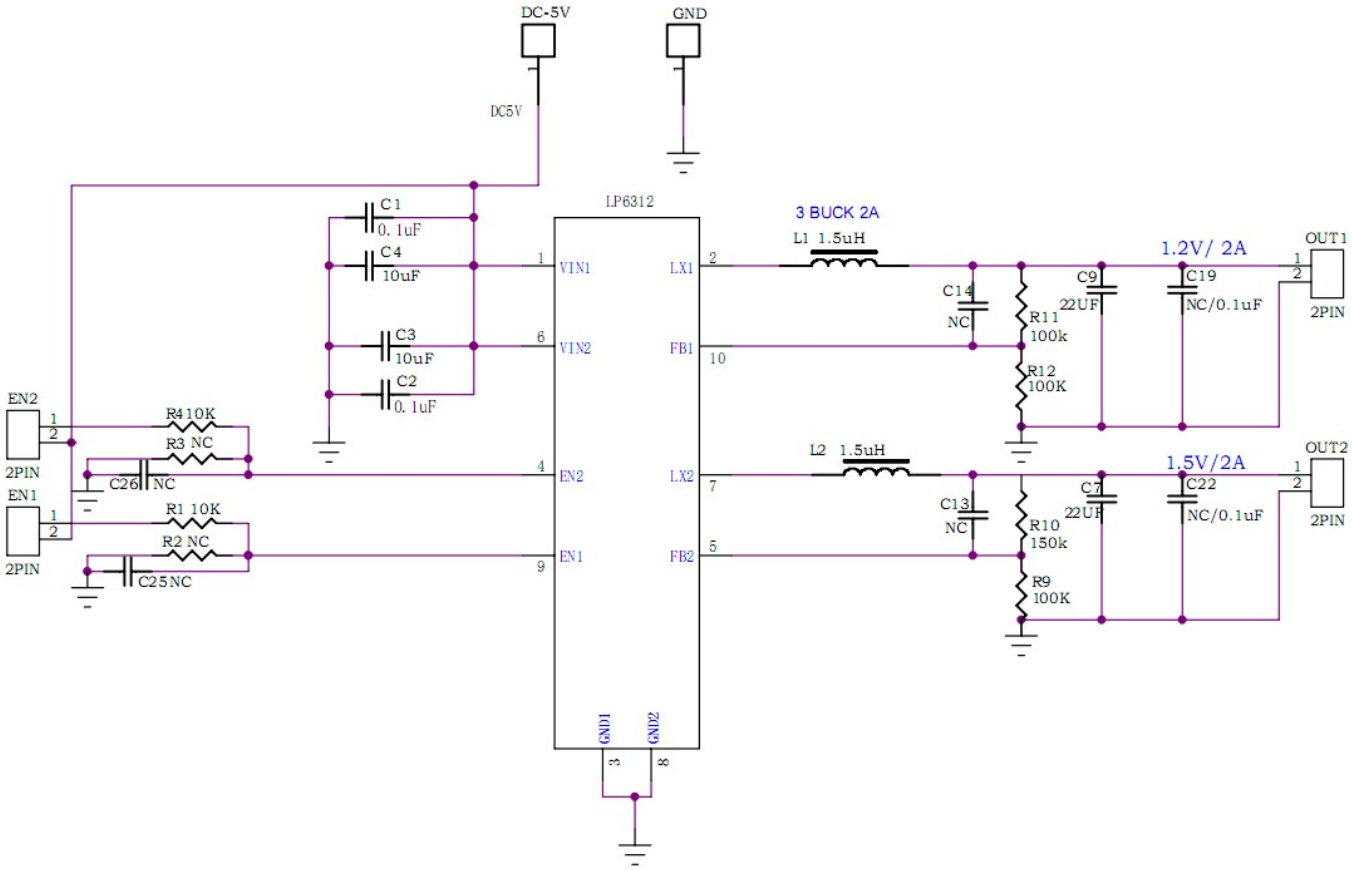
$$P_{D(TOTAL)} = V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2}$$

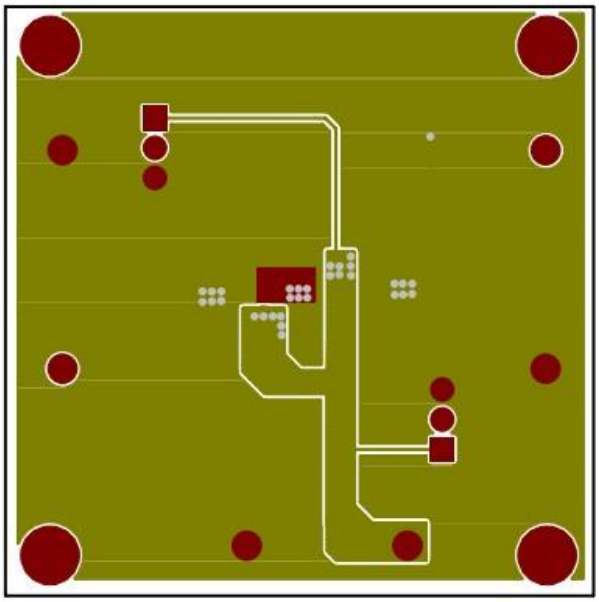
PCB Layout

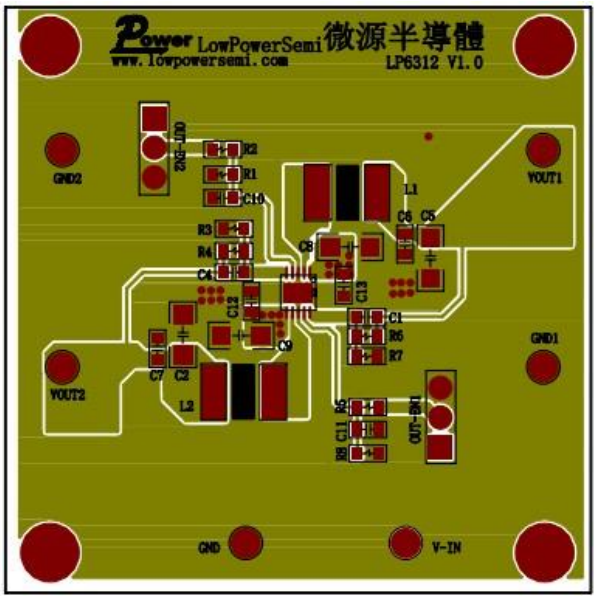
Layout is very critical for PMIC designs. For LP6312 PCB layout considerations, please refer to the following suggestions to get best performance.

- It is suggested to use 4-layer PCB layout and place LX plane and output plane on the top layer, place VIN plane in the inner layer.
- The top layer SMD input and output capacitors ground plane should be connected to the internal ground layer and bottom ground plane individually by using vias.
- The GND should be connected to inner ground layer directly by using via.
- High current path traces need to be widened.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.
- Keep the feedback path (from V_{OUTX} to FBx) away from the noise node (ex. LXx). LXx is a high current noise node. Complete the layout by using short and wide traces.
- The top layer exposed pad ground plane should be connected to the internal ground layer and bottom ground plane by using a number of vias to improve thermal performance.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.

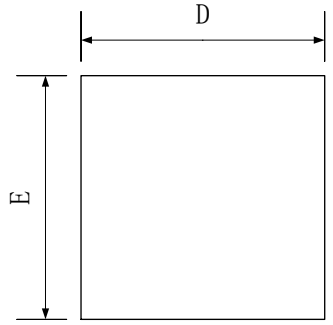
Demo Board


DC-5V
GND
DC5V
LP6312
C1
0. 1uF
C4
10uF
C3
10uF
C2
0. 1uF
3 BUCK 2A
L1 1.5uH
1.2V/ 2A
OUT1
2PIN
C14
NC
R11
100k
C9
22UF
C19
NC/0.1uF
R12
100K
EN2
R4 10K
R3 NC
C26 NC
EN1
R1 10K
R2 NC
C25 NC
L2 1.5uH
1.5V/2A
OUT2
C13
NC
R10
150k
C7
22UF
C22
NC/0.1uF
R9
100K
VIN1
VIN2
EN2
EN1
LX1
LX2
FB1
FB2
GND1
GND2

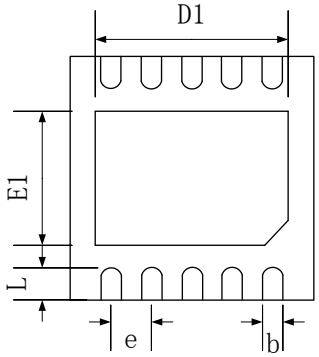



LowPowerSemi
www.lowpowersemi.com
LP6312 V1.0
GND2
VOUT1
VOUT2
GND1
GND
V-IN

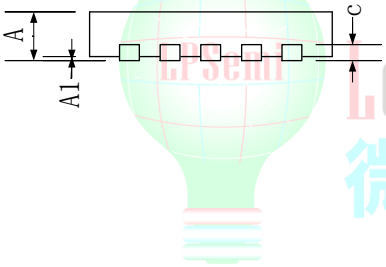
Packaging Information



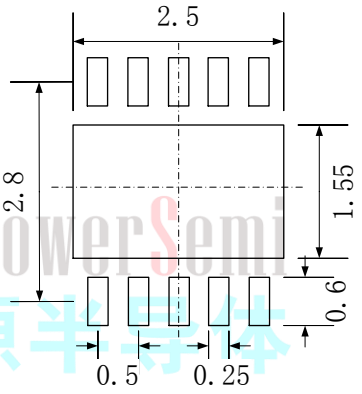
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C		0.20 REF	
D	2.90	3.00	3.10
D1	2.40	2.50	2.60
E	2.90	3.00	3.10
E1	1.45	1.55	1.65
e		0.50 BSC	
L	0.30	0.40	0.50