14CH Programmable Gamma and VCOM Buffers

General Description

The LP6298 providers a 14-channel programmable gamma buffer and 1-channel programmable VCOM buffer for applications in TFT-LCD Panel. Each of the 14-channel gamma buffers is generated using a 10-bit resolution digital-to-analog converter together with a buffer through IIC control.

The LP6298 also features a programmable operational amplifier that drives the LCD VCOM. This unity-gain buffer is capable of rail-to-rail output, fast slew rate, and ±140mA output short-circuits current. The VCOM buffer voltage is IIC programmed using 7-bit resolution.

The LP6298 includes EEPROM to store gamma codes and VCOM codes, and control it through IIC interface at the real time.

The LP6298 is available in a space saving QFN24 (0.5mm pitch) package.

Order Information

LP6298 □□□
- F: Pb-Free
- Package Type
  - QV: QFN-24

Features

- IIC Interface Control (0x74, 0x75)
- Integrated EEPROM
- Input Supply Voltage Range
  - 2.9V to 3.6V Logic Supply Range
  - 6.5V to 18V Analog Supply Range
- 14-Channel Programmable Gamma Buffers
  - 10-Bit, 1024-Step Resolution
  - ±70mA Output Short Current
  - ±20mA Operation Current
  - 8V/μs Slew Rate
- 1-Channel Programmable VCOM Buffer
  - 7-Bits, 128-Step Current Output
  - ±140mA Output Short Current
  - ±70mA Operation Current
  - 25V/μs Slew Rate
- Protection Function
  - Under Voltage Lockout
  - Short Circuit Protection
  - Over Temperature Protection
  - Check Sum Function
- Available in QFN-24 (4mm×4mm)
- RoHS Compliant and Halogen Free
- Pb-Free Package

Applications

- TFT LCD Panels

Marking Information

Device	Marking	Package	Shipping
LP6298QVF	LPS LP6298 YWXXX	QFN-24	3K/REEL
Y is year code. W is week code. XXX is series number.			

Typical Application Circuit

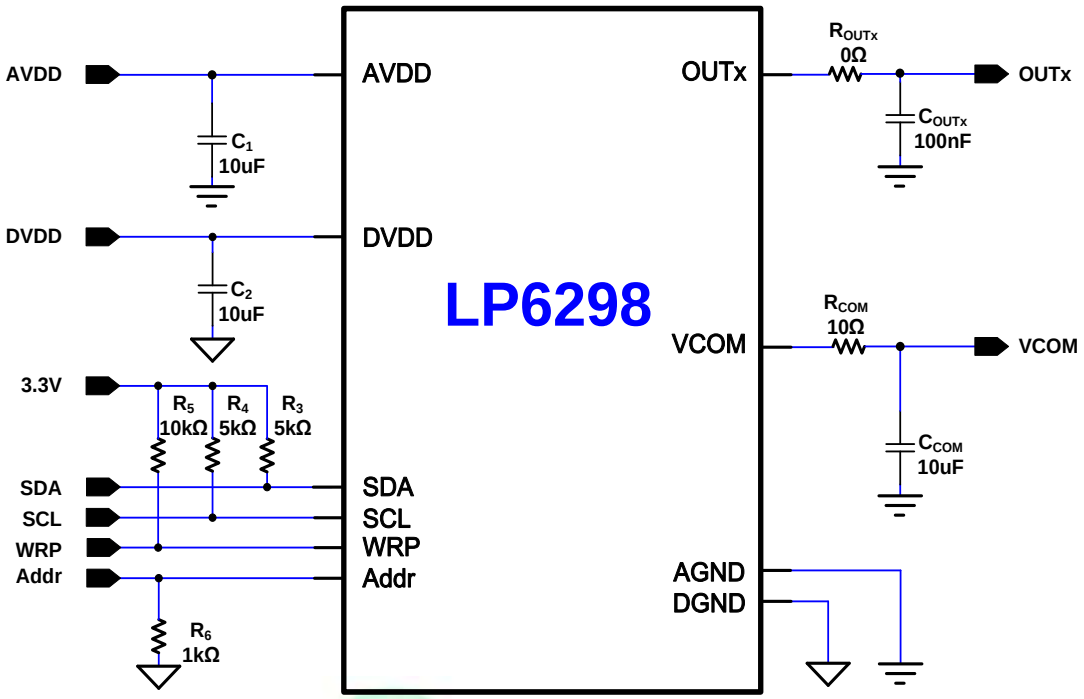


Figure 1. Typical Application Circuit of LP6298

Pin Configuration

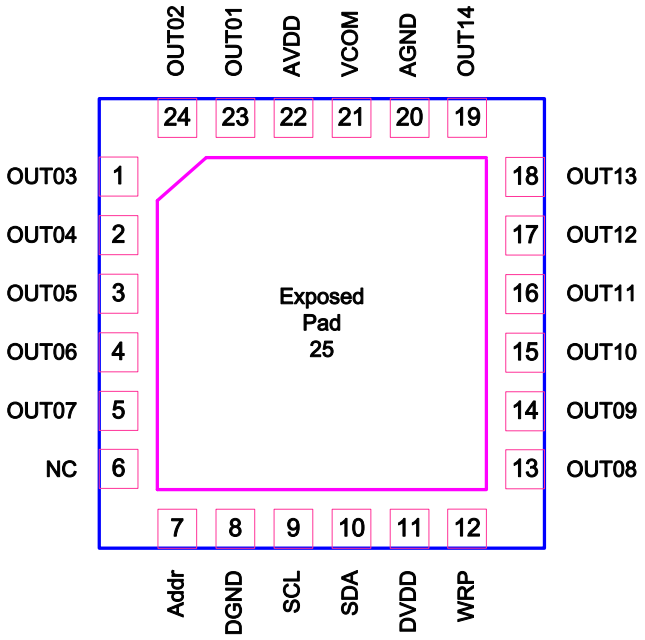


Figure 2. QFN-24 Package (4mm x 4mm) Top View

Function Block Diagram

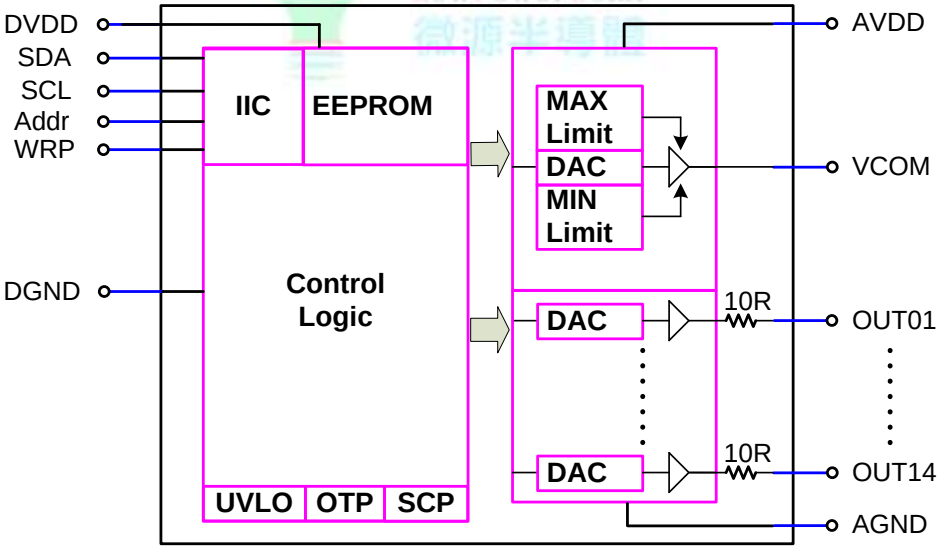


Figure 3. Function Block Diagram

Functional Pin Description

Pin NO.	Pin Name	Description
1	OUT03	Gamma Buffer Output.
2	OUT04	Gamma Buffer Output.
3	OUT05	Gamma Buffer Output.
4	OUT06	Gamma Buffer Output.
5	OUT07	Gamma Buffer Output.
6	NC	Not Connect.
7	Addr	IIC interface Device Address Bit0. Addr = L : IIC slave address is 0x74H. Addr = H : IIC slave address is 0x75H.
8	DGND	Digital Ground.
9	SCL	IIC interface clock signal.
10	SDA	IIC interface data signal.
11	DVDD	Digital Power Supply Input. Bypass DVDD to DGND with 10μF capacitor
12	WRP	EEPROM Write Protection. WRP = H: Write Enable. WRP = L : Write Disable
13	OUT08	Gamma Buffer Output.
14	OUT09	Gamma Buffer Output.
15	OUT10	Gamma Buffer Output.
16	OUT11	Gamma Buffer Output.
17	OUT12	Gamma Buffer Output.
18	OUT13	Gamma Buffer Output.
19	OUT14	Gamma Buffer Output.
20	AGND	Analog Ground.
21	VCOM	VCOM Amplifier Output
22	AVDD	Analog Power Supply Input. Bypass AVDD to AGND with 10μF capacitor
23	OUT01	Gamma Buffer Output
24	OUT02	Gamma Buffer Output
25		Exposed Pad. Connect this pin to AGND.

Absolute Maximum Ratings Note 1

- ✧ AVDD to AGND ---------- −0.3V to +20V
- ✧ DVDD to DGND ---------- −0.3V to +7V
- ✧ SDA, SCL, WRP, Addr to DGND ---------- −0.3V to DVDD+0.3V
- ✧ OUT01~OUT14, VCOM to AGND ---------- −0.3V to AVDD +0.3V
- ✧ AGND to DGND ---------- −0.3V to +0.3V
- ✧ Operating Junction Temperature Range (T_J) ---------- −40℃ to +150℃
- ✧ Operation Ambient Temperature Range (T_J) ---------- −40°C to +85°C
- ✧ Storage Temperature Range ---------- −65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- +150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

  QFN-24 (4mm x 4mm), θ_{JA} ---------- 50°C/W

  QFN-24 (4mm x 4mm), θ_{JC} ---------- 25°C/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) ---------- 4KV
- ✧ MM(Machine Mode) ---------- 400V

Recommended Operating Conditions

- ✧ VCOM Output Current, I_{COM} ---------- -70mA ~ +70mA
- ✧ Gamma Output Current, I_{GMA} ---------- -20mA ~ +20mA

Electrical Characteristics

(V_{DVDD}=3.3V, V_{AVDD}= 16.5V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
DVDD Input Supply Voltage	V_{DVDD}		2.9		3.6	V
DVDD UVLO Threshold	V_{UVLO}				2.7	V
DVDD Supply Current	I_{DQ}			0.75	1.5	mA
AVDD Input Supply Voltage	V_{AVDD}		6.5		18	V
AVDD Supply Current	I_{AQ}			10	15	mA
Thermal Shutdown Threshold	T_{SD}	Junction Temperature Rising		150		°C
Digital Input (WRP, Addr)						
Input Threshold Voltage	V_{IH}	Logic High.	0.8* DVDD			V
	V_{IL}	Logic Low			0.2* DVDD	
Input Current	I_{DIN}		-40		+40	nA
VGMA Reference DAC						
Reference DAC Voltage	V_{REF}	AVDD-0.2V > V_{REF}	6		17.8	V
Reference Voltage Resolution				8		Bits
Differential Nonlinearity	DNL_{REF}	V_{REF}=6V~17.8V, V_{REF}(DAC)=0~255	-0.5		0.5	LSB
Integral Nonlinearity	INL_{REF}	V_{REF}=6V~17.8V, V_{REF}(DAC)=0~255	-1		1	LSB
Gamma Buffers (OUT1~OUT14)						
OUTx Resolution				10		Bits
OUTx Differential Nonlinearity Error	DNL_{OUTx}		-1		+1	LSB
OUTx Integral Nonlinearity Error	INL_{OUTx}		-4		+4	LSB
OUTx Swing	V_{GOH}	V_{AVDD}=10V , V_{REF}=9.8V, OUTx(DAC)=1023	V_{REF} -0.15	V_{REF}		V
	V_{GOL}	V_{AVDD}=10V , V_{REF}=9.8V, OUTx(DAC)=0			GND +0.15	
OUTx Short Circuit Current	I_{Short_OUTx}			±70		mA
Load Regulation	LR_{OUTx}	OUTx(DAC)=512, I_{OUTx} =±25mA		±0.5	±1.5	V/A
Slew Rate	SR_{OUTx}		10			V/us
Settling Time	ts_{OUTx}			5		us
Electrically-Erasable Programmable ROM (EEPROM)						
Byte Write Time	t_{BYTE}				10	ms
Programmable Times				1000		Cycle

Electrical Characteristics (Continued)

(V_{DVDD}=3.3V, V_{AVDD}= 16.5V, V_{REF}=16V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCOM Reference MAX/MIN						
VCOM Resolution				7		Bits
Limit Ref. Voltage	V_{L_REF}		0.6*$V_{REF\_DAC\_MIN}$		0.6*$V_{REF\_DAC\_MAX}$	V
Differential Nonlinearity	DNL_{CDAC}	V_{AVDD}=18V, V_{REF}=16.5V, $V_{COM\_MAX/MIN}$(DAC)=0~127, (No Load)	-0.5		0.5	LSB
Integral Nonlinearity	INL_{CDAC}	V_{AVDD}=18V, V_{REF}=16.5V, $V_{COM\_MAX/MIN}$(DAC)=0~127, (No Load)	-1		1	LSB
VCOM Buffer (VCOM)						
VCOM Resolution				7		Bits
VCOM Differential Nonlinearity Error	DNL_{COM}	V_{AVDD}=18V, V_{REF}=16.5V, V_{COM}(DAC)=0~127, (No Load)	-1		+1	LSB
VCOM Integral Nonlinearity Error	INL_{COM}	V_{AVDD}=18V, V_{REF}=16.5V V_{COM}(DAC)=0~127, (No Load)	-4		+4	LSB
VCOM Output Swing	VOH	V_{AVDD}=10V , V_{L_REF}=9.8V, V_{COM_DAC}=127, (No Load)	V_{L_REF} -0.15	V_{L_REF}		V
	VOL	V_{AVDD}=10V , V_{L_REF}=9.8V, V_{COM_DAC}=0, (No Load)		GND	GND +0.15	V
Short Circuit Current	I_{Short_COM}			±140		mA
Load Regulation	LR_{VCOM}	AVDD=18V,V_{REF}=16.5V, $V_{COM\ Max\ /\ Min}$ =127 / 0, V_{COM} = V_{COM_DAC}/2 ; I_{SINK}=I_{SOURCE} = 70mA		±0.5	±1.0	V/A
Slew Rate	SR_{VCOM}	AVDD=18V,V_{REF}=16.5V, V_{L_ref} = 0.6*V_{REF}; $V_{COM\ Max\ /\ Min}$ =127 / 0, V_{COM_DAC}=0 to 127, (No Load)	20	25		V/us
Settling Time	ts_{VCOM}			5		us
Power Supply Rejection Ration	PSRR	6.5V<AVDD<18V		60		dB
Bandwidth	BW		13	20		MHz

Application Information

The LP6298 integrates 14 channels of programmable gamma buffers, and a programmable operational amplifier that drives the LCD VCOM. The device uses IIC interface for setting such as output voltages, programming gamma and VCOM codes into EEPROM.

Under Voltage Lockout (UVLO)

The LP6298 had an UVLO internal circuit that enables the device once the voltage on the DVDD voltage exceeds the UVLO threshold voltage.

DACs Output Setting

The V_{REF} control the full-scale output of the DACs. It can use the following equations to determine the output voltages.

The V_{REF} value can calculate using below equation.

$$V_{REF} = 6 + 11.8 \times \frac{V_{REF(CODE)}}{255}$$

The V_{OUTx} value can calculate using below equation.

$$V_{OUTx} = V_{REF} \times \frac{V_{GMAx(CODE)}}{1023}$$

The V_{COM_MAX} and V_{COM_MIN} value can calculate using below equation.

$$V_{COM\_MAX} = 0.6 \times V_{REF} \times \frac{V_{COM\_MAX(CODE)}}{127}$$

$$V_{COM\_MIN} = 0.6 \times V_{REF} \times \frac{V_{COM\_MIN(CODE)}}{127}$$

The V_{COM} value can calculate using below equation.

$$V_{COM} = V_{COM\_MIN} + (V_{COM\_MAX} - V_{COM\_MIN}) \times \frac{V_{COM(CODE)}}{127}$$

EEPROM Write Protection

The WRP pin control the register can write to EEPROM or not by IIC interface. The WRP pin pull high level defines can be write data into EEPROM from register by IIC interface. If WRP is low level and IIC could write command to save into control byte of the register, but not happen write EEPROM event.

Over Temperature Protection

The LP6298 device enters over temperature protection if its junction temperature exceeds 150°C (Typ.). During over temperature protection none of the device's functions are available.

DT V_{COM} Setting (0x4F)

LP6298 device has a special situation; it can quickly modify the value of V_{COM} through another slave address.

Slave Address							
D6	D5	D4	D3	D2	D1	D0	W/R
1	0	0	1	1	1	1	0/1

What's more, you can directly modify the EEROM and RAM of V_{COM} by using the control pin of DT-V_{COM}.

DT V_{COM} Value							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM Data[6:0]							0/1

DT-V_{COM} Control	
Register	Bit Description
0	Data written to EEPROM and RAM register
1	Data written to RAM register only

Application Information (Continued)

Layout Guideline

The proper PCB layout and component placement are critical for all circuit. Here are some suggestions to the layout of LP6298 design.

1. Connected all ground together with one uninterrupted ground plane, which include digital ground and analog ground.

2. The input capacitor should be located as closed as possible to the VIN and ground plane.

3. All output capacitor must be closed to ground plane. The ground terminal of C_{OUT} must be located as closed as possible to ground plane.

4. The exposed pad of the chip should be connected to ground plane for maximum thermal consideration.

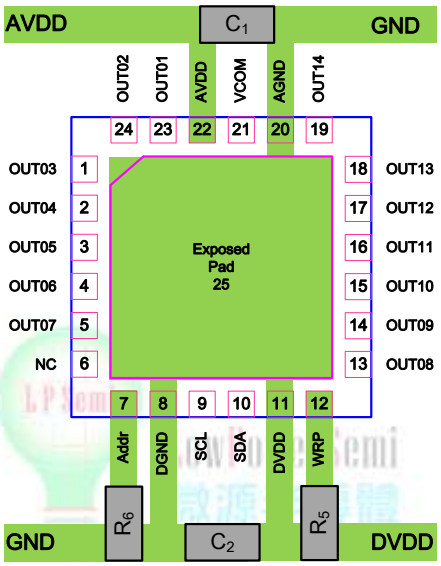


Figure 4. Recommended PCB Layout Diagram

Application Information (Continued)

1. IIC Interface Specification

The LP6298 can easily modify parameters by IIC bus, that slave address is show below:

Slave Address							
D6	D5	D4	D3	D2	D1	D0	W/R
1	1	1	0	1	0	**Addr**	**0/1**

IIC is a two wire serial interface developed, the bus consists of a clock line(SCL) and a data line(SDA) with pull-up structures. The LP6298 works as a slave mode, and address can set by Addr pin. The data transfer protocol is follow IIC-Bus Specification's standard mode(100kbps) and fast mode(400kbps).

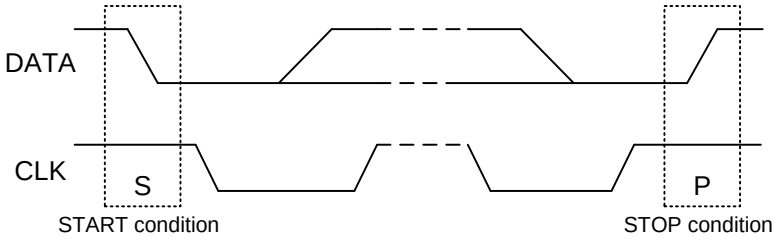


Figure 5. START and STOP Conditions

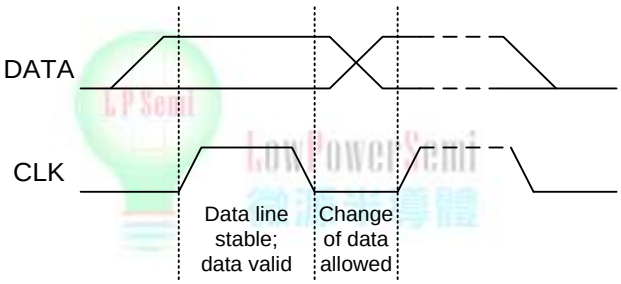


Figure 6. Bit Transfer on the Serial Interface

2. Write Data to Register

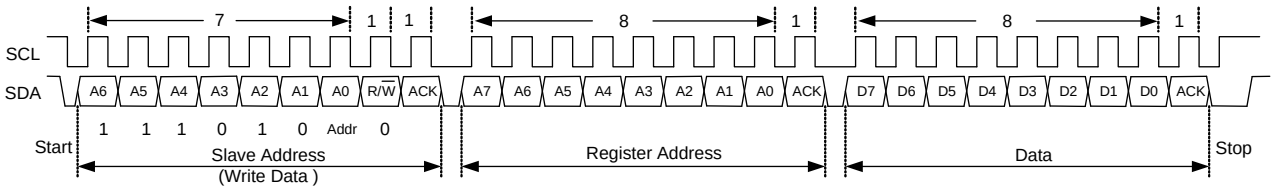


Figure 7. Write Single Byte Data to Register

3. Read Data to Register

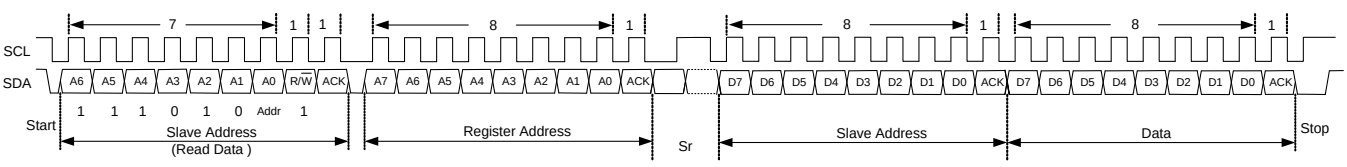


Figure 8. Read Single Byte Data from Register

Application Information (Continued)

4. IIC REGISTER MAP

The lowest bit number (0) represents the least bit, the highest bit number (7) represents the most bit, and R/W indicates whether the bit is read only (R), write only (W), or both read and write (R/W).

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Preset EEPROM	NOTE
0x00				Reset	W_ROM2	W_ROM1	OUT_EN		02h	**CONTROL**
0x01	VCOM [6:0]								80h	**DVR_VCOM**
0x02	VREF [7:0]								FFh	**VREF_DAC**
0x03		VCOM_MAX [6:0]							7Fh	**VCOM_MAX**
0x04		VCOM_MIN [6:0]							00h	**VCOM_MIN**
0x05			GMA1 [9:4]						20h	Gamma1 Gamma2
0x06	GMA1 [3:0]						GMA2 [9:8]		02h	
0x07	GMA2 [7:0]								00h	
0x08			GMA3 [9:4]						20h	Gamma3 Gamma4
0x09	GMA3 [3:0]						GMA4 [9:8]		02h	
0x0A	GMA4 [7:0]								00h	
0x0B			GMA5 [9:4]						20h	Gamma5 Gamma6
0x0C	GMA5 [3:0]						GMA6 [9:8]		02h	
0x0D	GMA6 [7:0]								00h	
0x0E			GMA7 [9:4]						20h	Gamma7 Gamma8
0x0F	GMA7 [3:0]						GMA8 [9:8]		02h	
0x10	GMA8 [7:0]								00h	
0x11			GMA9 [9:4]						20h	Gamma9 Gamma10
0x12	GMA9 [3:0]						GMA10 [9:8]		02h	
0x13	GMA10 [7:0]								00h	
0x14			GMA11 [9:4]						20h	Gamma11 Gamma12
0x15	GMA11 [3:0]						GMA12 [9:8]		02h	
0x16	GMA12 [7:0]								00h	
0x17			GMA13 [9:4]						20h	Gamma13 Gamma14
0x18	GMA13 [3:0]						GMA14 [9:8]		02h	
0x19	GMA14 [7:0]								00h	
0x1A	--	--	--	--	--	--	--	--		**Reserved**
.	.									**Reserved**
.	.									**Reserved**
.	.									**Reserved**
.	.									**Reserved**
.	.									**Reserved**
0x58	--	--	--	--	--	--	--	--		**Reserved**
0x59	Gheck-Sum1 [7:1]							--	80h	**VCOM**
0x5A	--	--	Gheck-Sum2 [13:8]						01h	**VREF/ VCOM_MAX/MIN**
0x5B	Gheck-Sum2 [7:0]								7Eh	
0x5C			Gheck-Sum3 [13:8]						00h	**All Gamma**
0x5D	Gheck-Sum3 [7:0]								EEh	
0x5E	--	--	--	--	--	--	--	--		**Reserved**

Application Information (Continued)

Set Control Signal (Register Address – 00H)

Control Signal							
Addr: 00H	**Default Value : Ctrl(Register)=0x02H**						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R
0	0	0	Reset[4]	W_ROM2[3]	W_ROM1[2]	OUT_EN[1]	0

Control Reset[4]		Control W_ROM2[3]	
Register	**Bit Description**	**Register**	**Bit Description**
0	W/O Action	0	W/O Action
1	Download data from EEPROM to Register	1	Write VCOM Register data into EEPROM

Control W_ROM1[2]		Control OUT_EN[1]	
Register	**Bit Description**	**Register**	**Bit Description**
0	W/O Action	0	Disable Output.
1	Write Other Register data into EEPROM	1	Enable Output.

Set VCOM Signal (Register Address – 01H)

VCOM Signal							
Addr: 01H	**Default Value : VCOM(Register)=0x80H**						
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
VCOM[6]	VCOM[5]	VCOM[4]	VCOM[3]	VCOM [2]	VCOM [1]	VCOM [0]	0

Set VREF Output Voltage (Register Address – 02H)

VREF Voltage							
Addr: 02H	**Default Value : VREF (Register)=0xFFH, VREF=17.8V**						
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VREF [7]	VREF [6]	VREF [5]	VREF [4]	VREF [3]	VREF [2]	VREF [1]	VREF [0]

Set VCOM Maximum Signal (Register Address – 03H)

VCOM Signal							
Addr: 03H	**Default Value : VCOM_MAX(Register)=0x7FH, VCOM_ MAX =10.68V**						
D7	D6	D5	D4	D3	D2	D1	D0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	VCOM_MAX[6]	VCOM_MAX[5]	VCOM_MAX[4]	VCOM_MAX[3]	VCOM_MAX[2]	VCOM_MAX[1]	VCOM_MAX[0]

Set VCOM Minimum Signal (Register Address – 04H)

VREF Signal							
Addr: 04H	**Default Value : VCOM_ MIN (Register)=0x00H, VCOM_ MIN =0V**						
D7	D6	D5	D4	D3	D2	D1	D0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	VCOM_MIN[6]	VCOM_MIN[5]	VCOM_MIN[4]	VCOM_MIN[3]	VCOM_MIN[2]	VCOM_MIN[1]	VCOM_MIN[0]

Application Information (Continued)

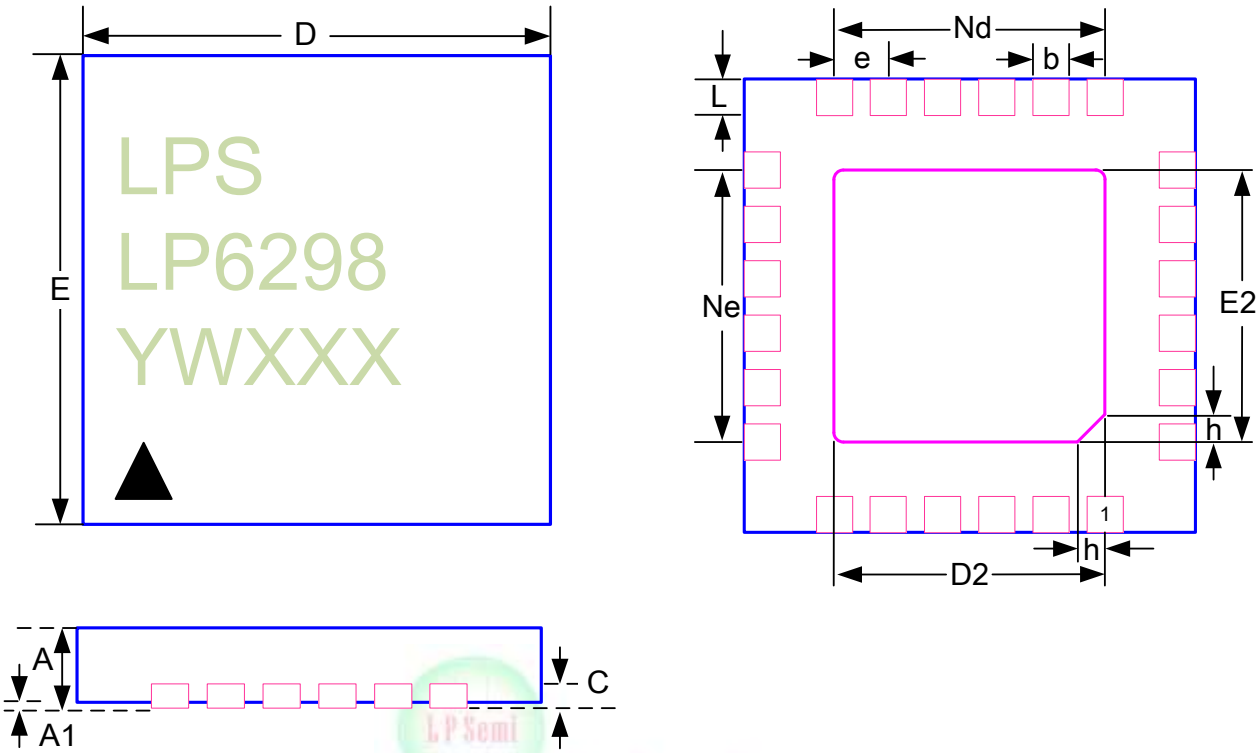
Set GMA1~GMA14 Output Voltage (Register Address – 05H to 19H)

GMAx Voltage									
Addr: 05H to 19H		Default Value : GMAx (Register)=0x200H, GMAx =8.9V, R[02]=0xFFH							
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
GMAx [9]	GMAx [8]	GMAx [7]	GMAx [6]	GMAx [5]	GMAx [4]	GMAx [3]	GMAx [2]	GMAx [1]	GMAx [0]

GMAx [9:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
0000000000	(VREF/1023)*0	0100000000	(VREF/1023)*256	1000000000	(VREF/1023)*512	1100000000	(VREF/1023)*768
0000000001	(VREF/1023)*1	0100000001	(VREF/1023)*257	1000000001	(VREF/1023)*513	1100000001	(VREF/1023)*769
0000000010	(VREF/1023)*2	0100000010	(VREF/1023)*258	1000000010	(VREF/1023)*514	1100000010	(VREF/1023)*770
0000000011	(VREF/1023)*3	0100000011	(VREF/1023)*259	1000000011	(VREF/1023)*515	1100000011	(VREF/1023)*771
0000000100	(VREF/1023)*4	0100000100	(VREF/1023)*260	1000000100	(VREF/1023)*516	1100000100	(VREF/1023)*772
0000000101	(VREF/1023)*5	0100000101	(VREF/1023)*261	1000000101	(VREF/1023)*517	1100000101	(VREF/1023)*773
0000000110	(VREF/1023)*6	0100000110	(VREF/1023)*262	1000000110	(VREF/1023)*518	1100000110	(VREF/1023)*774
0000000111	(VREF/1023)*7	0100000111	(VREF/1023)*263	1000000111	(VREF/1023)*519	1100000111	(VREF/1023)*775
0000001000	(VREF/1023)*8	0100001000	(VREF/1023)*264	1000001000	(VREF/1023)*520	1100001000	(VREF/1023)*776
0000001001	(VREF/1023)*9	0100001001	(VREF/1023)*265	1000001001	(VREF/1023)*521	1100001001	(VREF/1023)*777
0000001010	(VREF/1023)*10	0100001010	(VREF/1023)*266	1000001010	(VREF/1023)*522	1100001010	(VREF/1023)*778
0000001011	(VREF/1023)*11	0100001011	(VREF/1023)*267	1000001011	(VREF/1023)*523	1100001011	(VREF/1023)*779
0000001100	(VREF/1023)*12	0100001100	(VREF/1023)*268	1000001100	(VREF/1023)*524	1100001100	(VREF/1023)*780
0000001101	(VREF/1023)*13	0100001101	(VREF/1023)*269	1000001101	(VREF/1023)*525	1100001101	(VREF/1023)*781
0000001110	(VREF/1023)*14	0100001110	(VREF/1023)*270	1000001110	(VREF/1023)*526	1100001110	(VREF/1023)*782
0000001111	(VREF/1023)*15	0100001111	(VREF/1023)*271	1000001111	(VREF/1023)*527	1100001111	(VREF/1023)*783
			:				
0011110000	(VREF/1023)*240	0111110000	(VREF/1023)*496	1011110000	(VREF/1023)*752	1111110000	(VREF/1023)*1008
0011110001	(VREF/1023)*241	0111110001	(VREF/1023)*497	1011110001	(VREF/1023)*753	1111110001	(VREF/1023)*1009
0011110010	(VREF/1023)*242	0111110010	(VREF/1023)*498	1011110010	(VREF/1023)*754	1111110010	(VREF/1023)*1010
0011110011	(VREF/1023)*243	0111110011	(VREF/1023)*499	1011110011	(VREF/1023)*755	1111110011	(VREF/1023)*1011
0011110100	(VREF/1023)*244	0111110100	(VREF/1023)*500	1011110100	(VREF/1023)*756	1111110100	(VREF/1023)*1012
0011110101	(VREF/1023)*245	0111110101	(VREF/1023)*501	1011110101	(VREF/1023)*757	1111110101	(VREF/1023)*1013
0011110110	(VREF/1023)*246	0111110110	(VREF/1023)*502	1011110110	(VREF/1023)*758	1111110110	(VREF/1023)*1014
0011110111	(VREF/1023)*247	0111110111	(VREF/1023)*503	1011110111	(VREF/1023)*759	1111110111	(VREF/1023)*1015
0011111000	(VREF/1023)*248	0111111000	(VREF/1023)*504	1011111000	(VREF/1023)*760	1111111000	(VREF/1023)*1016
0011111001	(VREF/1023)*249	0111111001	(VREF/1023)*505	1011111001	(VREF/1023)*761	1111111001	(VREF/1023)*1017
0011111010	(VREF/1023)*250	0111111010	(VREF/1023)*506	1011111010	(VREF/1023)*762	1111111010	(VREF/1023)*1018
0011111011	(VREF/1023)*251	0111111011	(VREF/1023)*507	1011111011	(VREF/1023)*763	1111111011	(VREF/1023)*1019
0011111100	(VREF/1023)*252	0111111100	(VREF/1023)*508	1011111100	(VREF/1023)*764	1111111100	(VREF/1023)*1020
0011111101	(VREF/1023)*253	0111111101	(VREF/1023)*509	1011111101	(VREF/1023)*765	1111111101	(VREF/1023)*1021
0011111110	(VREF/1023)*254	0111111110	(VREF/1023)*510	1011111110	(VREF/1023)*766	1111111110	(VREF/1023)*1022
0011111111	(VREF/1023)*255	0111111111	(VREF/1023)*511	1011111111	(VREF/1023)*767	1111111111	(VREF/1023)*1023

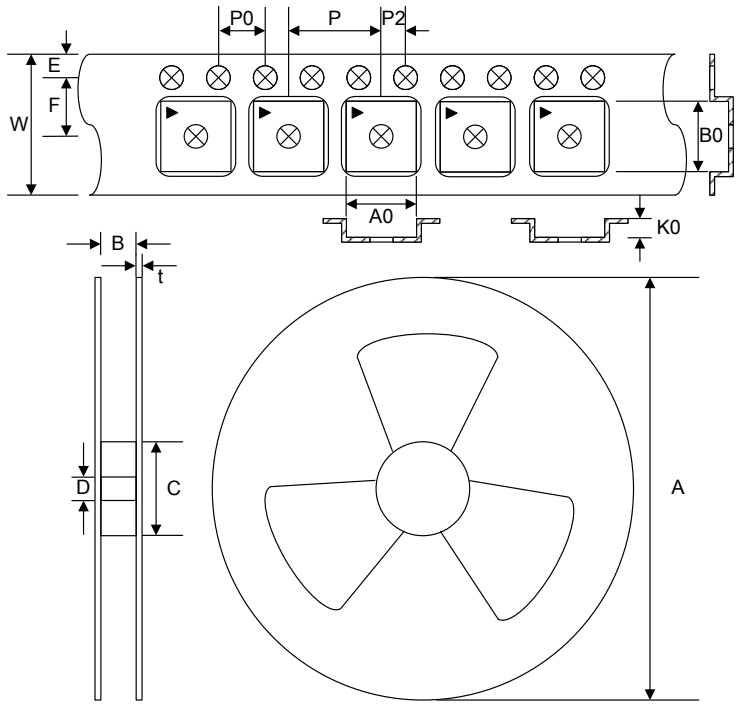
Outline Information

QFN-24 Package (4x4) pitch 0.5 (Unit: mm)



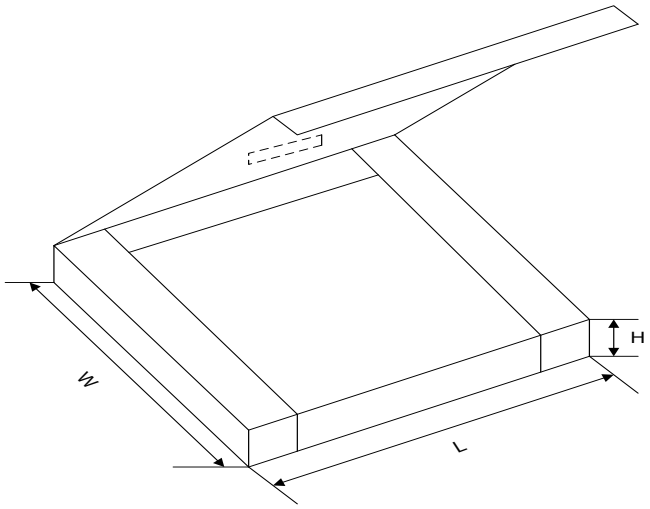
SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.180	0.250	0.300
C	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.400	2.500	2.600
E	3.900	4.000	4.100
E2	2.400	2.500	2.600
e	0.500 BSC		
Nd	2.500 BSC		
Ne	2.500 BSC		
L	0.350	0.400	0.450
h	0.300	0.350	0.400

Carrier Dimensions



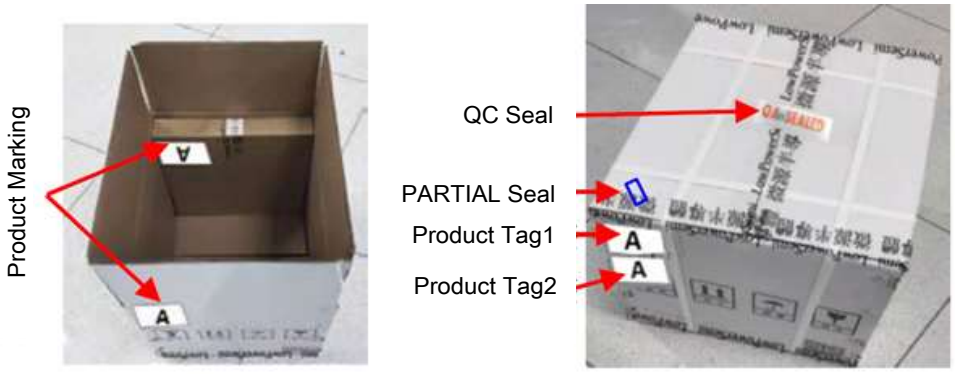
Device	Package Type		Pins	SPQ	A (mm)	B (mm)	C (mm)	D (mm)	t (mm)
LP6298	QFN		24	3000	ø329±1	16.8±1	ø100±1	ø13.3±0.3	2±0.3
	W (mm)	E (mm)	F (mm)	P (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P2 (mm)
	12±0.3	1.75±0.1	5.5±0.05	8±0.1	4.3±0.1	4.3±0.1	1.1±0.1	4±0.1	2±0.1

Carrier Box Dimensions



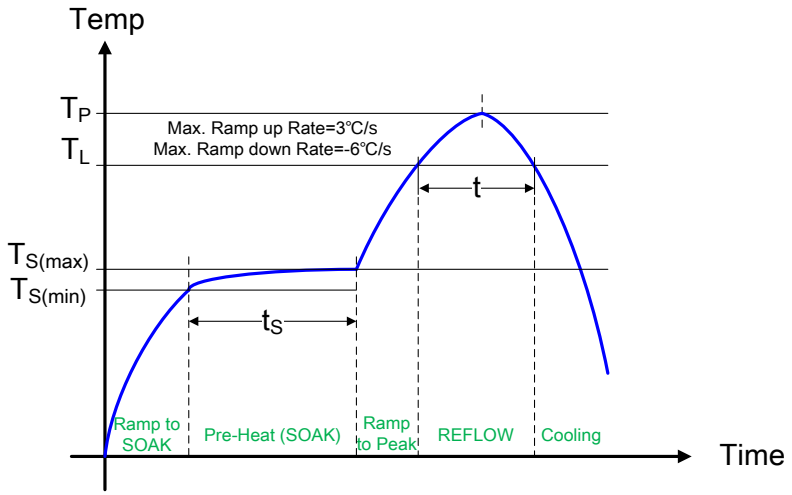
Device	Package Type	Pins	SPQ	L (mm)	W (mm)	H (mm)
LP6298	QFN	24	3000	336	336	48

Carton Dimensions



Device	PW (mg)	BOX/Carton	SPQ/Carton	L (mm)	W (mm)	H (mm)
LP6298	38	8	24000	420	355	365

Classification Profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature min ($T_{S(min)}$) Temperature max ($T_{S(max)}$) Time ($T_{S(min)}$ to $T_{S(max)}$) (t_S)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate ($T_{S(max)}$ to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (T_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temp. (T_P)	See Classification Temp in table 1	See Classification Temp in table 2
Time (T_P) within 5°C of the specified classification temperature	20 seconds	30 seconds
Average ramp-down rate (T_P to $T_{S(max)}$)	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

Table 1. SnPb Eutectic Process – Classification Temperatures

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	235 °C	220 °C
≥ 2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures

Package Thickness	Volume mm^3 < 350	Volume mm^3 <350 - 2000	Volume mm^3 ≥ 2000
< 1.6 mm	260 °C	260 °C	260 °C
1.6 mm ~ 2.5 mm	260 °C	250 °C	245 °C
≥ 2.5 mm	250 °C	245 °C	245 °C