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Product List

OB39R32T2W32VP,
OB39R32T2W28SP,
OB39R32T2W24SP,
OB39R32T2W24GP,
OB39R32T2W20SP,

Description

The OB39R32T2 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 32KB+8KB embedded Flash for program, and executes all ASM51 instructions fully compatible with MCS-51.

OB39R32T2 contains 1152B+256B on-chip RAM, various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.

The high performance of OB39R32T2 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

OB39R32T2ihhkL YWW
i: process identifier { W = 2.2V ~ 5.5V}
hh: pin count
k: package type postfix {as table below }
L:PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y: Year Code
WW: Week Code (01-52)

Postfix	Package
S	SOP (300 mil)
V	LQFP
G	SSOP (150 mil)

Features

- 32KB+8KB on-chip program memory.
- Working voltage 2.2V~5.5V.
- High speed architecture of 1 clock/machine cycle runs up to 22.1184MHz.
- 1~8T can be switched on the fly.
- 256 bytes RAM as standard 8052, plus 1152 bytes on-chip expandable RAM
- Port 0~3,Up to 30 GPIO
- Dual 16-bit Data Pointers (DPTR0 & DPTR1).
- Two serial peripheral interfaces in full duplex mode (UART0 & UART1)
- Up to 24 touch sense inputs, support multiplexing I/O function.
- Lower power touch-key wakeup function.
- Four 16-bit Timer/Counters. (Timer 0,1,2,3)
- Programmable watchdog reset and interrupt timer.
- Two IIC interface. (Master/Slave mode).
- 4-channel 16-bit compare / capture functions.
- 4-channel PWM.
- ISP/IAP/ICP functions.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- LVI/LVR (LVR deglitch 500ns).
  POR and Programmable LVR(2.7V / 1.55V) & LVI (4.0V / 3.3V / 2.8V / 1.8V)
- 10-channel 12-bit ADC.
- External interrupt 0, 1, 2, 3 with four priority levels.(INT x 4)
- Keyboard Interface (KBI x 8) on port 1 for eight more interrupts.
- LED driver: COM x7, Segment x 16.
- Software RTC
- Enhance user code protection.
- Power management unit for IDLE and power down modes.
- Clock Source:
  - 32.768KHz XTAL input to timer, allow running on power down mode with wakeup function .
  - HIRC: 22.1184MHz Internal RC-oscillator, with programmable clock divider. Factory trimmed to 2% at full temperature range
  - LIRC: 26KHz

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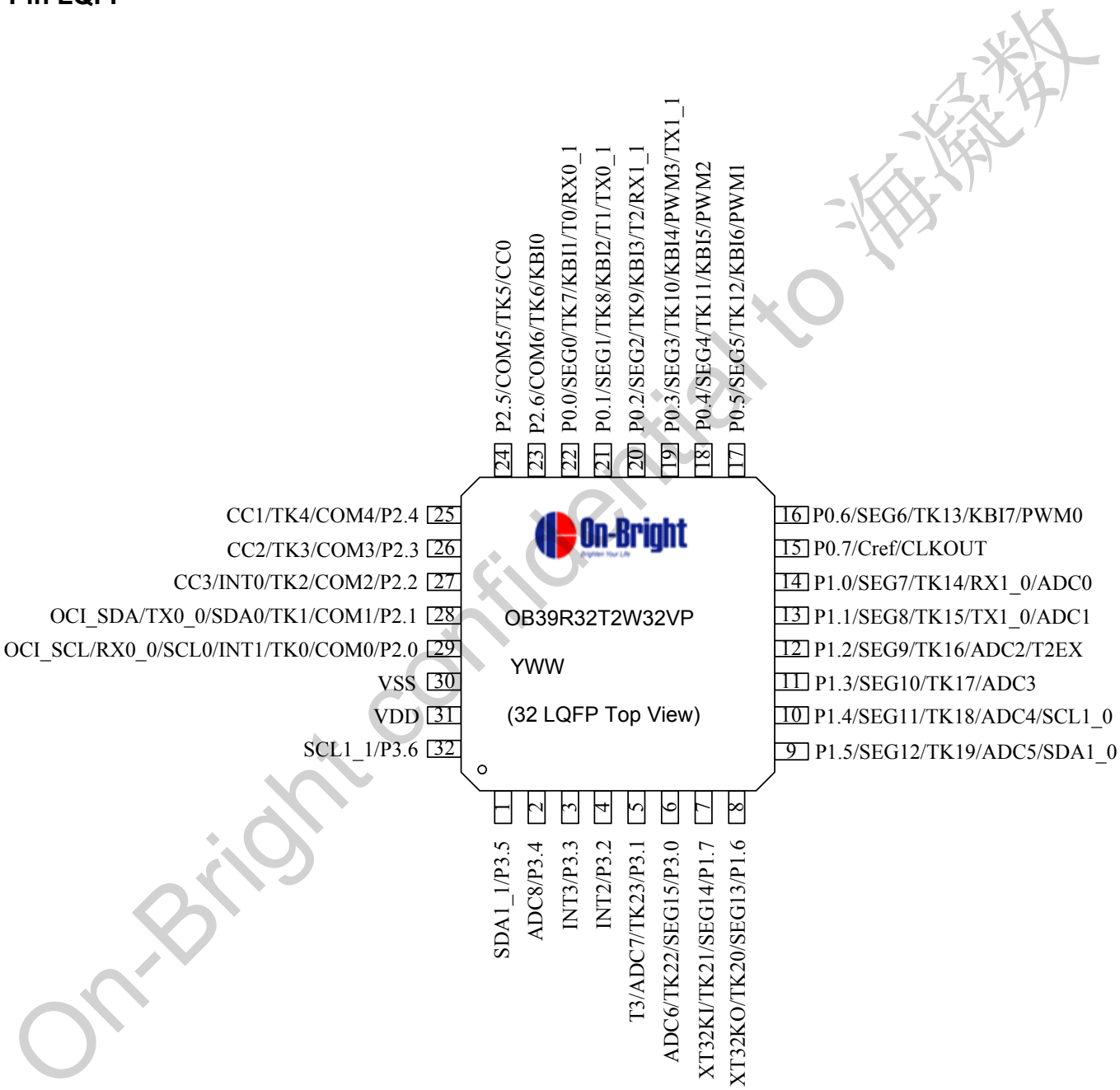
Pin Configuration

32 Pin LQFP



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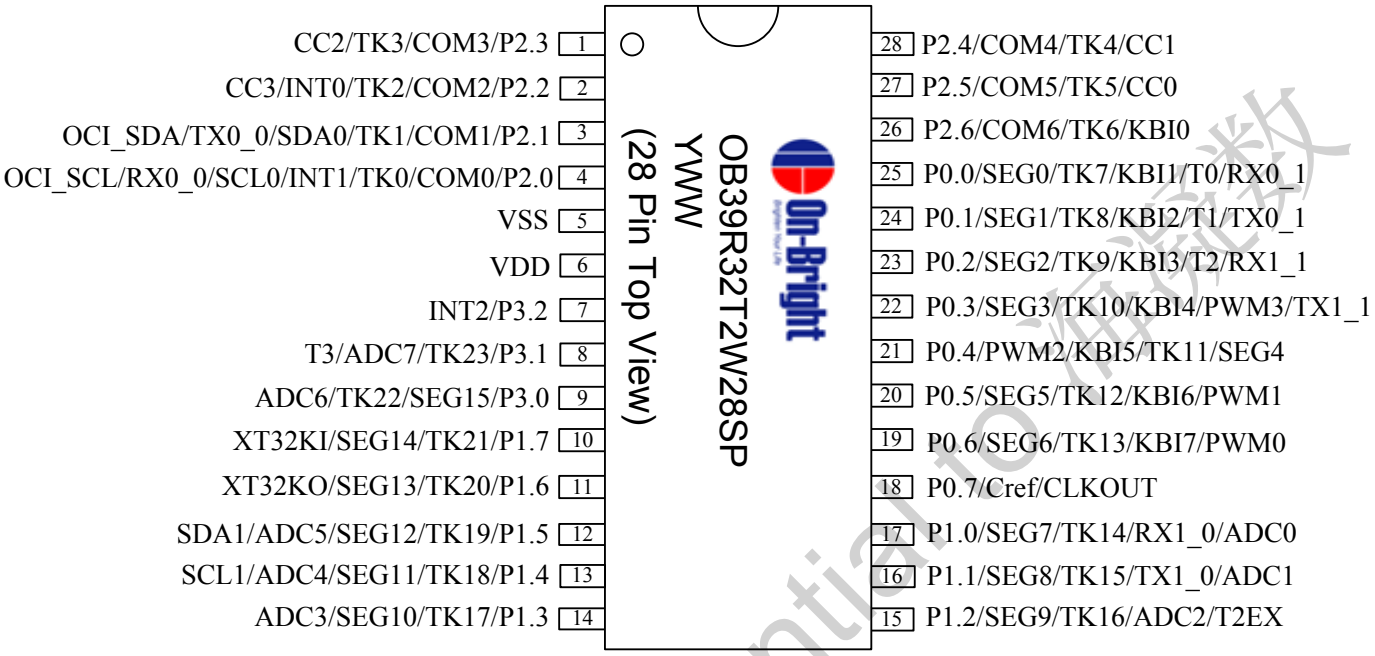
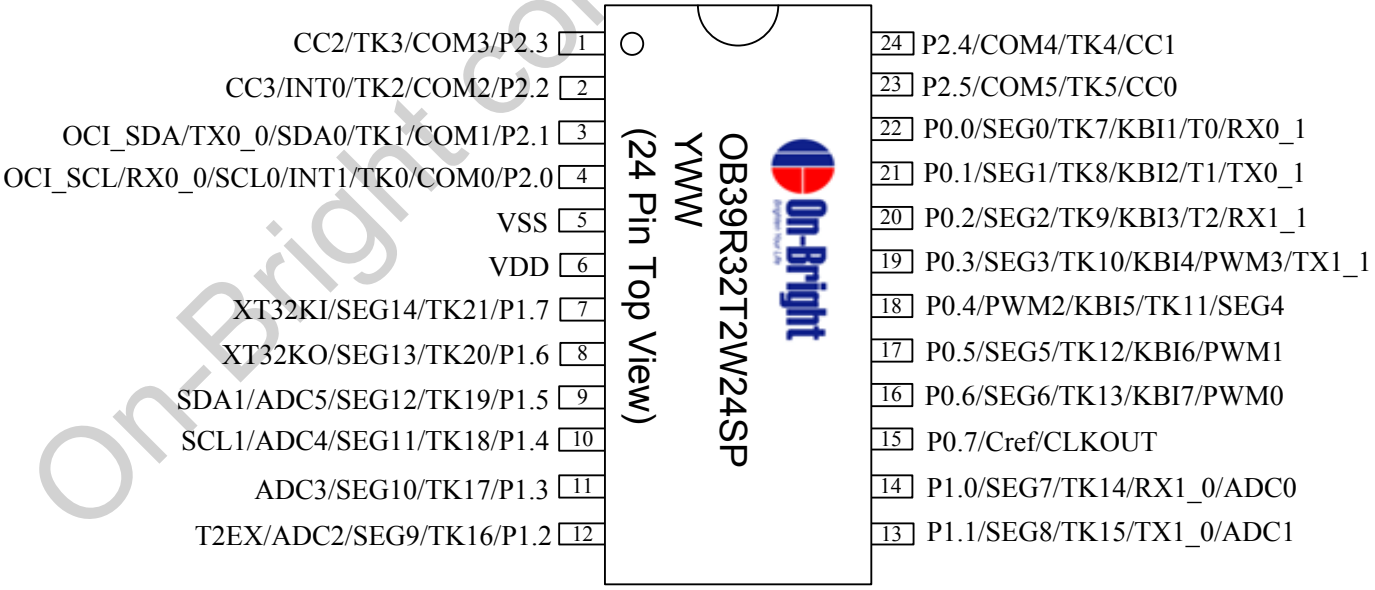
28 Pin SOP



24 Pin SOP/SSOP



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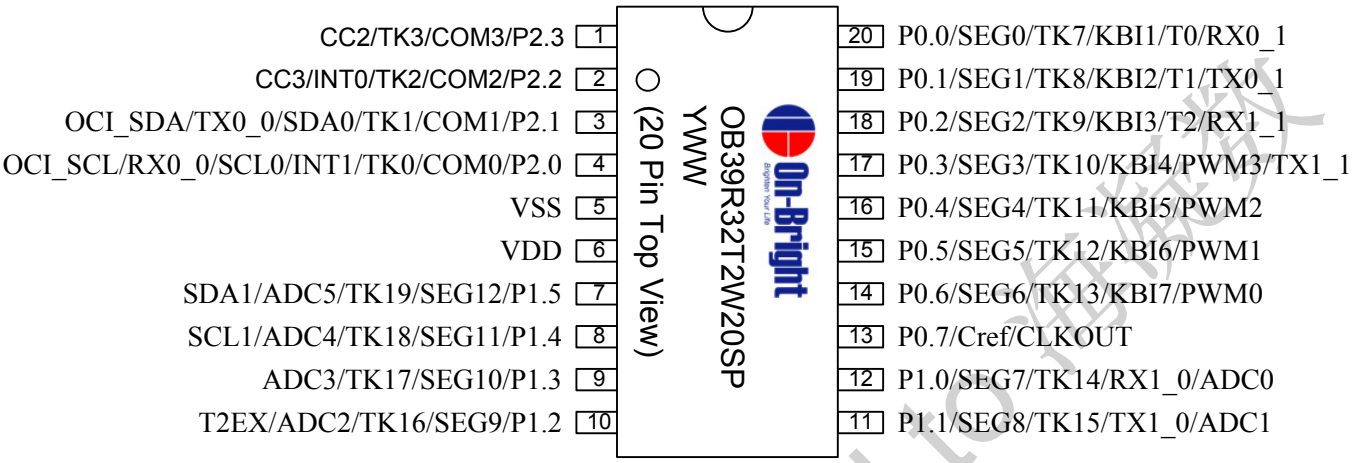
20 Pin SOP



Notes：

(1) To avoid accidentally entering ISP-Mode(refer to section 19.4), care must be taken not asserting pulse signal at RXD0 P2.0 & RXD1 P1.1 during power-up while P0.2, P0.3 or P0.4 are set to high.

(2) To apply ICP function, OCI_SDA/P2.1 and OCI_SCL/P2.0 are ICP pins during reset period. When reset finish, they are GPIO.

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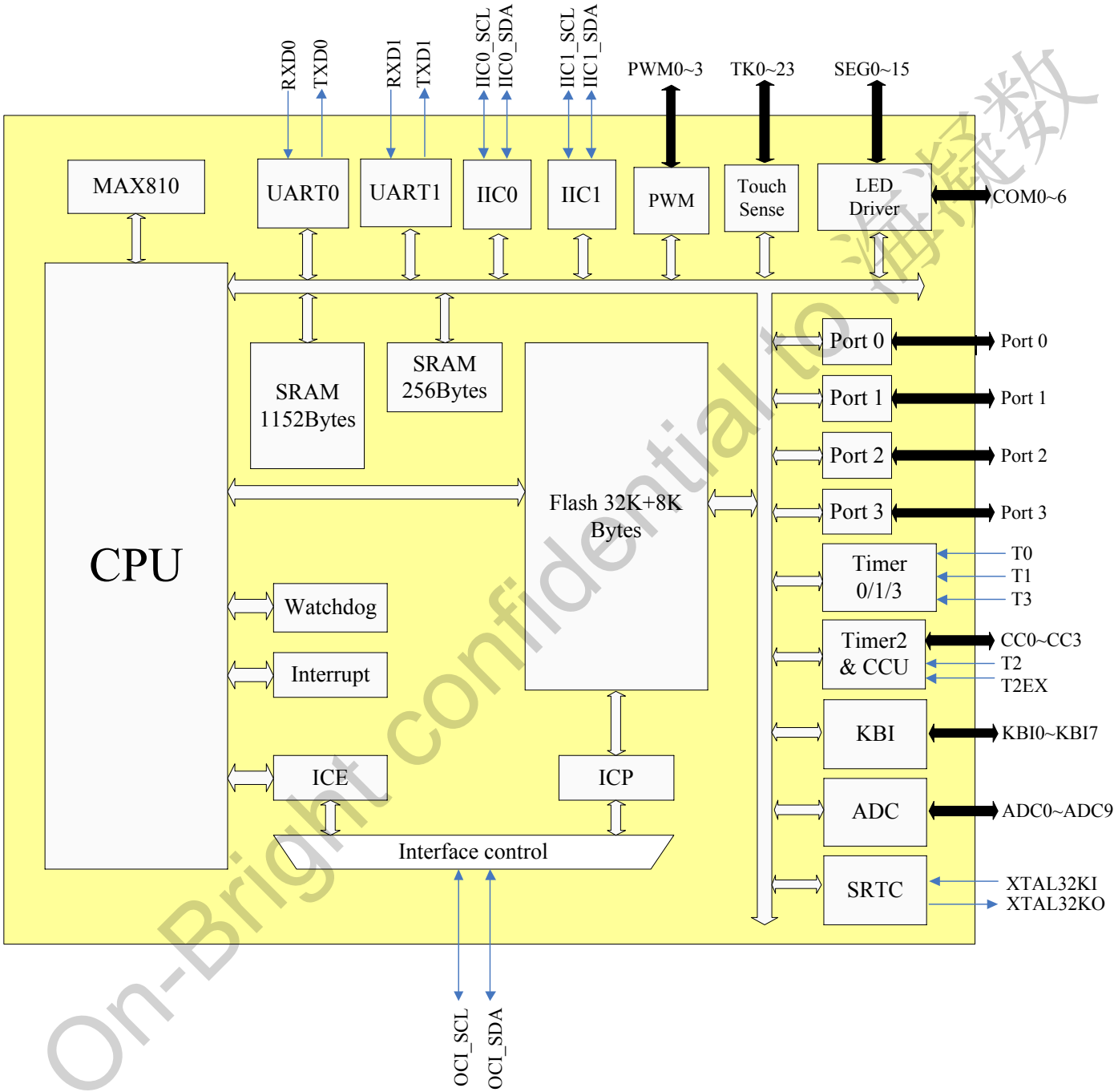
Block Diagram



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Pin Description

32L	28L	24L	20L	Symbol	I/O	Description
1				P3.5/SDA1_1	I/O	Bit 5 of port 3 & IIC1_1 SDA
2				P3.4/ADC8	I/O	Bit 4 of port 3 & ADC input channel 8
3				P3.3/INT3	I/O	Bit 3 of port 3 & External interrupt 3
4	7			P3.2/INT2	I/O	Bit 2 of port 3 & External interrupt 2
5	8			P3.1/TK23/ADC7/T3	I/O	Bit 1 of port 3 & Touch key 23 & ADC input channel 7 & Timer 3 external input
6	9			P3.0/SEG15/TK22/ADC6	I/O	Bit 0 of port 3 & LED driver segment 15 & Touch key 22 & ADC input channel 6
7	10	7		P1.7/SEG14/TK21/XT32KI	I/O	Bit 7 of port 1 & LED driver segment 14 & Touch key 21 & 32KHz Crystal input
8	11	8		P1.6/SEG13/TK20/XT32KO	I/O	Bit 6 of port 1 & LED driver segment 13 & Touch key 20 & 32KHz Crystal output
9	12	9	7	P1.5/SEG12/TK19/ADC5/SDA1_0	I/O	Bit 5 of port 1 & LED driver segment 12 & Touch key 19 & ADC input channel 5 & IIC1_0 SDA
10	13	10	8	P1.4/SEG11/TK18/ADC4/SCL1_0	I/O	Bit 4 of port 1 & LED driver segment 11 & Touch key 18 & ADC input channel 4 & IIC1_0 SCL
11	14	11	9	P1.3/SEG10/TK17/ADC3	I/O	Bit 3 of port 1 & LED driver segment 10 & Touch key 17 & ADC input channel 3
12	15	12	10	P1.2/SEG9/TK16/ADC2/T2EX	I/O	Bit 2 of port 1 & LED driver segment 9 & Touch key 16 & ADC input channel 2 & Timer 2 capture trigger
13	16	13	11	P1.1/SEG8/TK15/TX1_0/ADC1	I/O	Bit 1 of port 1 & LED driver segment 8 & Touch key 15 & Serial interface channel 1_0 transmit data & ADC input channel 1
14	17	14	12	P1.0/SEG7/TK14/RX1_0/ADC0	I/O	Bit 0 of port 1 & LED driver segment 7 & Touch key 14 & Serial interface channel 1_0 receive data & ADC input channel 0
15	18	15	13	P0.7/Cref/CLKOUT	I/O	Bit 7 of port 0 & Touch key external capacitor & Clock output
16	19	16	14	P0.6/SEG6/TK13/KBI7/PWM0	I/O	Bit 6 of port 0 & LED driver segment 6 & Touch key 13 & KBI interrupt 7 & PWM Channel 0
17	20	17	15	P0.5/SEG5/TK12/KBI6/PWM1	I/O	Bit 5 of port 0 & LED driver segment 5 & Touch key 12 & KBI interrupt 6 & PWM Channel 1
18	21	18	16	P0.4/SEG4/TK11/KBI5/PWM2	I/O	Bit 4 of port 0 & LED driver segment 4 & Touch key 11 & KBI interrupt 5 & PWM Channel 2
19	22	19	17	P0.3/SEG3/TK10/KBI4/PWM3/TX1_1	I/O	Bit 3 of port 0 & LED driver segment 3 & Touch key 10 & KBI interrupt 4 & PWM channel 3 & Serial interface channel 1_1 transmit data
20	23	20	18	P0.2/SEG2/TK9/KBI3/T2/RX1_1	I/O	Bit 2 of port 0 & LED driver segment 2 & Touch key 9 & KBI interrupt 3 & Timer 2 external input & Serial interface channel 1_1 receive data
21	24	21	19	P0.1/SEG1/TK8/KBI2/T1/TX0_1	I/O	Bit 1 of port 0 & LED driver segment 1 & Touch key 8 & KBI interrupt 2 & Timer 1 external input & Serial interface channel 0_1 transmit data

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22	25	22	20	P0.0/SEG0/TK7/KBI1/T0/RX0_1	I/O	Bit 0 of port 0 & LED driver segment 0 & Touch key 7 & KBI interrupt 1 & Timer 0 external input & Serial interface channel 0_1 receive data
23	26			P2.6/COM6/TK6/KBI0	I/O	Bit 6 of port 2 & LED driver common 6 & Touch key 6 & KBI interrupt 0
24	27	23		P2.5/COM5/TK5/CC0	I/O	Bit 5 of port 2 & LED driver common 5 & Touch key 5 & Timer 2 compare/capture Channel 0
25	28	24		P2.4/COM4/TK4/CC1	I/O	Bit 4 of port 2 & LED drIver common 4 & Touch key 4 & Timer 2 compare/capture Channel 1
26	1	1	1	P2.3/COM3/TK3/CC2	I/O	Bit 3 of port 2 & LED driver common 3 & Touch key 3 & Timer 2 compare/capture Channel 2
27	2	2	2	P2.2/COM2/TK2/INT0/CC3	I/O	Bit 2 of port 2 & LED driver common 2 & Touch key 2 & External interrupt 0 & Timer 2 compare/ capture Channel 3
28	3	3	3	P2.1/COM1/TK1/SDA0/TX0_0/OCI_SDA	I/O	Bit 1 of port 2 & LED driver common 1 & Touch key 1 & IIC0 SDA & Serial interface channel 0_0 transmit data & On-Chip Instrumentation Data I/O pin of ICE and ICP Functions
29	4	4	4	P2.0/COM0/TK0/INT1/SCL0/RX0_0/OCI_SCL	I/O	Bit 0 of port 2 & LED driver common 0 & Touch key 0 & External interrupt 1 & & IIC0 SCL & Serial interface channel 0_0 receive data & On-Chip Instrumentation Clock I/O pin of ICE and ICP Functions
30	5	5	5	VSS	I	Ground
31	6	6	6	VDD	I	Power supply
32				P3.6/SCL1_1	I/O	Bit 6 of port 3 & & IIC1_1 SCL

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Special Function Register (SFR)

A map of the Special Function Registers is shown as below:

In-direct access Mode

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8	IIC0S	IIC0CTL	IIC0A1	IIC0A2	IIC0RWD	IIC0EBT	TKSTATUS0	WDTIC	FF
F0	B	KBLS	KBE	KBF	KBD	SRTCCON		TAKEY	F7
E8	IIC1S	IIC1CTL	IIC1A1	IIC1A2	IIC1RWD	IIC1EBT	INTDEG	ADCSH	EF
E0	ACC	ISPFAH	ISPFAL	ISPFD	ISPFC	ENHIT	LVC	SWRES	E7
D8	TCON1	PFCON	P3M0	P3M1	S1CON	S1BUF	S1RELL	S1RELH	DF
D0	PSW	CCEN2	P0M0	P0M1	P1M0	P1M1	P2M0	P2M1	D7
C8	T2CON	CCCON	CRCL	CRCH	TL2	TH2	PWMMDL	PWMMDH	CF
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3	C7
B8	IEN1	IP1	S0RELH	TKSTATUS1	PWMD0L	PWMD0H	PWMD1L	PWMD1H	BF
B0	P3	PWMD2L	PWMD2H	PWMD3L	PWMD3H	PWMC	WDTRC	WDTK	B7
A8	IEN0	IP0	S0RELL	ADCC1	ADCC2	ADCDH	ADCDL	ADCCS	AF
A0	P2	RSTS							A7
98	S0CON	S0BUF	IEN2	TKCON	TKSW	TKCHN	TKCDL	TKCDH	9F
90	P1	AUX	T3MOD	TKSTATUS2	TL3	TH3		IRCON2	97
88	TCON0	TMOD	TL0	TL1	TH0	TH1	CKCON	IFCON	8F
80	P0	SP	DPL	DPH	DPL1	DPH1	RCON	PCON	87
Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex

Register map of xdata (External data memory):

Indirect Access Mode

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
FFF8								ADCCAL	FFFF
FFF0		TKEN2	TKEN1	TKEN0	TKRUNTIME	TKPSSR	TKWKTRICNT	TKDEB	FFF7
:									:
:									:
FF28									FF2F
FF20	LEDCLK								FF17
FF18	COM5_C [15:8]	COM5_C [7:0]	COM6_C [15:8]	COM6_C [7:0]	COMEN	SEGEN0	SEGEN1	LEDCON	FF1F
FF10	COM1_C [15:8]	COM1_C [7:0]	COM2_C [15:8]	COM2_C [7:0]	COM3_C [15:8]	COM3_C [7:0]	COM4_C [15:8]	COM4_C [7:0]	FF07
FF08	COM4_A [15:8]	COM4_A [7:0]	COM5_A [15:8]	COM5_A [7:0]	COM6_A [15:8]	COM6_A [7:0]	COM0_C [15:8]	COM0_C [7:0]	FF0F
FF00	COM0_A [15:8]	COM0_A [7:0]	COM1_A [15:8]	COM1_A [7:0]	COM2_A [15:8]	COM2_A [7:0]	COM3_A [15:8]	COM3_A [7:0]	FF07
Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex

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Note: Special Function Registers reset values and description for OB39R32T2.

Register	Location: 80h ~ 8Fh	Reset value	Description
SYSTEM			
SP	81h	07h	Stack Pointer
ACC	E0h	00h	Accumulator
PSW	D0h	00h	Program Status Word
B	F0h	00h	B Register
DPL	82h	00h	Data Pointer 0 Low Byte
DPH	83h	00h	Data Pointer 0 High Byte
DPL1	84h	00h	Data Pointer 1 Low Byte
DPH1	85h	00h	Data Pointer 1 High Byte
AUX	91h	00h	Auxiliary Register
PCON	87h	00h	Power Control
RCON	86h	00h	Internal RAM Control Register
CKCON	8Eh	10h	Clock Control Register
INTERRUPT & PRIORITY			
IRCON	C0h	00h	Interrupt Request Control Register
IRCON2	97h	00h	Interrupt Request Control Register 2
IEN0	A8h	00h	Interrupt Enable Register 0
IEN1	B8h	00h	Interrupt Enable Register 1
IEN2	9Ah	00h	Interrupt Enable Register 2
IP0	A9h	00h	Interrupt Priority Register 0
IP1	B9h	00h	Interrupt Priority Register 1
ENHIT	E5h	00h	Enhance Interrupt Type Register
INTDEG	EEh	00h	External Interrupt Deglitch Register
UART 0			
PCON	87h	00h	Power Control
S0CON	98h	00h	Serial Port 0, Control Register
S0BUF	99h	00h	Serial Port 0, Data Buffer
S0RELL	AAh	00h	Serial Port 0, Reload Register, Low Byte
S0RELH	BAh	00h	Serial Port 0, Reload Register, High Byte
AUX	91h	00h	Auxiliary register
UART 1			
S1CON	DCh	00h	Serial port 1, Control Register
S1BUF	DDh	00h	Serial port 1, Data Buffer
S1RELL	DEh	00h	Serial port 1, Reload Register, Low Byte
S1RELH	DFh	00h	Serial port 1, Reload Register, High Byte
ADC			

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Register	Location: 80h ~ 8Fh	Reset value	Description
ADCC1	ABH	00H	ADC Control 1 Register
ADCC2	ACH	00H	ADC Control 2 Register
ADCDH	ADH	00H	ADC Data Register,High Byte
ADCDL	AEH	00H	ADC Data Register,Low Byte
ADCCS	AFH	00H	ADC Clock Select Register
ADCSH	EFh	00h	ADC Sample and Hold Time
WDT			
RSTS	A1h	00h	Reset Status Register
WDTRC	B6h	04h	Watchdog Timer Reset Control Register
WDTIC	FFh	00h	Watchdog Timer Interrupt Control Register
WDTK	B7h	00h	Watchdog Timer Refresh Key.
TAKEY	F7h	00h	Time Access Key Register
SRTC			
SRTCCON	F5h	00h	Software RTC Control Register
PWM			
PWMC	B5H	00H	PWM Control Register
PWMD0H	BDH	00H	PWM 0 Data High Register
PWMD0L	BCH	00H	PWM 0 Data Low Register
PWMD1H	BFH	00H	PWM 1 Data High Register
PWMD1L	BEH	00H	PWM 1 Data Low Register
PWMD2H	B2H	00H	PWM 2 Data High Register
PWMD2L	B1H	00H	PWM 2 Data Low Register
PWMD3H	B4H	00H	PWM 3 Data High Register
PWMD3L	B3H	00H	PWM 3 Data Low Register
PWMMDH	CFH	00H	PWM Max Data High Register
PWMMDL	CEH	FFH	PWM Max Data Low Register
TIMER0/TIMER1/ TIMER3			
TL0	8Ah	00h	Timer 0 , Low Byte Register
TH0	8Ch	00h	Timer 0 , High Byte Register
TL1	8Bh	00h	Timer 1 , Low Byte Register
TH1	8Dh	00h	Timer 1 , High Byte Register
TL3	94h	00h	Timer 3 , Low Byte Register
TH3	95h	00h	Timer 3 , High Byte Register
TMOD	89h	00h	Timer 0,1 Mode Control Register
T3MOD	92h	00h	Timer 3 Mode Control Register
TCON1	D8h	00h	Timer/Counter Control 1 Register
TCON0	88h	00h	Timer/Counter Control 0 Register
ENHIT	E5h	00h	ENHance Interrupt Type Register
PFCON	D9h	00h	Peripheral Frequency Control Register
PCA(TIMER2)			

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Register	Location: 80h ~ 8Fh	Reset value	Description
CCEN	C1h	00h	Compare/Capture Enable Register
CCL1	C2h	00h	Compare/Capture Register 1, Low Byte
CCH1	C3h	00h	Compare/Capture Register 1, High Byte
CCL2	C4h	00h	Compare/Capture Register 2, Low Byte
CCH2	C5h	00h	Compare/Capture Register 2, High Byte
CCL3	C6h	00h	Compare/Capture Register 3, Low Byte
CCH3	C7h	00h	Compare/Capture Register 3, High Byte
T2CON	C8h	00h	Timer 2 Control Register
CCCON	C9h	00h	Compare/Capture Control Register
CRCL	CAh	00h	Compare/Reload/Capture Register, Low Byte
CRCH	CBh	00h	Compare/Reload/Capture Register, High Byte
TL2	CCh	00h	Timer 2, Low Byte Register
TH2	CDh	00h	Timer 2, High Byte Register
CCEN2	D1h	00h	Compare/Capture Enable 2 register
GPIO			
P0	80h	User define	Port 0
P1	90h	User define	Port 1
P2	A0h	User define	Port 2
P3	B0h	User define	Port 3
P0M0	D2h	00h	Port 0 output mode 0
P0M1	D3h	00h	Port 0 output mode 1
P1M0	D4h	00h	Port 1 output mode 0
P1M1	D5h	00h	Port 1 output mode 1
P2M0	D6h	00h	Port 2 output mode 0
P2M1	D7h	00h	Port 2 output mode 1
P3M0	DAh	00h	Port 3 output mode 0
P3M1	DBh	00h	Port 3 output mode 1
TOUCH KEY			
TKCON	9Bh	00h	Touch Key Control Register.
TKCHN	9Dh	00h	Touch Key Channel Number Register.
TKCDL	9Eh	00h	Touch Key Capture Data Low-Byte Register.
TKCDH	9Fh	00h	Touch Key Capture Data Hi-Byte Register.
TKSW	9Ch	00h	Touch Key Switch Register.
TKSTATUS0	FEh	00h	Touch Key Status 0 Register.
TKSTATUS1	BBh	00h	Touch Key Status 0 Register.
TKSTATUS2	93h	00h	Touch Key Status 0 Register.
ISP/IAP/EEPROM			
IFCON	8Fh	00h	Interface Control Register

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Register	Location: 80h ~ 8Fh	Reset value	Description
ISPFAH	E1h	FFh	ISP Flash Address-High Register
ISPFAL	E2h	FFh	ISP Flash Address-Low Register
ISPFD	E3h	FFh	ISP Flash Data Register
ISPFC	E4h	00h	ISP Flash control register
TAKEY	F7h	00h	Time Access Key Register
LVI/LVR/SOFTRESET			
RSTS	A1h	00h	Reset StatusRegister
LVC	E6h	60h	Low Voltage Control Register
SWRES	E7h	00h	Software Reset Register
TAKEY	F7h	00h	Time Access Key Register
KBI			
KBLS	F1h	00h	KBI Llevel Selection Register.
KBE	F2h	00h	KBI Input Enable Register.
KBF	F3h	00h	KBI Flag Register.
KBD	F4h	00h	KBI De-bounce Control Register.
IIC 0			
IIC0S	F8h	00h	IIC0 Status Register
IIC0CTL	F9h	04h	IIC0 Control Register
IIC0A1	FAh	A0h	IIC0 Channel Address 1 Register
IIC0A2	FBh	60h	IIC0 Channel Address 2 Register
IIC0RWD	FCh	00h	IIC0 Channel Read / Write Data Buffer
IIC0EBT	FDh	00h	IIC0 Enable Bus Transaction Register
IIC 1			
IIC1S	E8h	00h	IIC1 Status Register
IIC1CTL	E9h	04h	IIC1 Control Register
IIC1A1	EAh	A0h	IIC1 Channel Address 1 Register
IIC1A2	EBh	60h	IIC1 Channel Address 2 Register
IIC1RWD	ECh	00h	IIC1 Channel Read / Write Data Buffer
IIC1EBT	EDh	00h	IIC1 Enable Bus Transaction Register

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Register	Location: FF00h ~ FFFFh	Reset value	Description
LED			
COM0_AH	0xFF00	00h	Common Anode 0 High Byte Register.
COM0_AL	0xFF01	00h	Common Anode 0 Low Byte Register.
COM1_AH	0xFF02	00h	Common Anode 1 High Byte Register.
COM1_AL	0xFF03	00h	Common Anode 1 Low Byte Register.
COM2_AH	0xFF04	00h	Common Anode 2 High Byte Register.
COM2_AL	0xFF05	00h	Common Anode 2 Low Byte Register.
COM3_AH	0xFF06	00h	Common Anode 3 High Byte Register.
COM3_AL	0xFF07	00h	Common Anode 3 Low Byte Register.
COM4_AH	0xFF08	00h	Common Anode 4 High Byte Register.
COM4_AL	0xFF09	00h	Common Anode 4 Low Byte Register.
COM5_AH	0xFF0A	00h	Common Anode 5 High Byte Register.
COM5_AL	0xFF0B	00h	Common Anode 5 Low Byte Register.
COM6_AH	0xFF0C	00h	Common Anode 6 High Byte Register.
COM6_AL	0xFF0D	00h	Common Anode 6 Low Byte Register.
COM0_CH	0xFF0E	00h	Common Cathode 0 High Byte Register.
COM0_CL	0xFF0F	00h	Common Cathode 0 Low Byte Register.
COM1_CH	0xFF10	00h	Common Cathode 1 High Byte Register.
COM1_CL	0xFF11	00h	Common Cathode 1 Low Byte Register.
COM2_CH	0xFF12	00h	Common Cathode 2 High Byte Register.
COM2_CL	0xFF13	00h	Common Cathode 2 Low Byte Register.
COM3_CH	0xFF14	00h	Common Cathode 3 High Byte Register.
COM3_CL	0xFF15	00h	Common Cathode 3 Low Byte Register.
COM4_CH	0xFF16	00h	Common Cathode 4 High Byte Register.
COM4_CL	0xFF17	00h	Common Cathode 4 Low Byte Register.
COM5_CH	0xFF18	00h	Common Cathode 5 High Byte Register.
COM5_CL	0xFF19	00h	Common Cathode 5 Low Byte Register.
COM6_CH	0xFF1A	00h	Common Cathode 6 High Byte Register.
COM6_CL	0xFF1B	00h	Common Cathode 6 Low Byte Register.
COMEN	0xFF1C	00h	LED COM Enable Register.
SEGEN0	0xFF1D	00h	LED SEG Enable 0 Register.
SEGEN1	0xFF1E	00h	LED SEG Enable 1 Register.
LEDCON	0xFF1F	00h	LED Control Register.
LEDCLK	0xFF20	00h	LED Clock Register.
ADC Caliration			
ADCCAL	FFFFH	02h	ADC Calibration Register.

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Register	Location: FF00h ~ FFFFh	Reset value	Description
Touch			
TKWKTRICNT	FFF6H	00h	Touch Key Trigger Counter Register.
TKPSSR	FFF5H	00h	Touch Key Samping Rate Register.(for Power Saving Mode)
TKRUNTIME	FFF4H	00h	Touch Key Running Time Register.
TKEN0	FFF3H	00h	Touch Key Enable 0 Register.
TKEN1	FFF2H	00h	Touch Key Enable 1 Register.
TKEN2	FFF1H	00h	Touch Key Enable 2 Register.

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Function Description

1. General Features

OB39R32T2 is an 8-bit micro-controller. All of its functions and the detailed meanings of SFR will be given in the following sections.

1.1 Embedded Flash

The program can be loaded into the embedded 32KB+8KB Flash memory via its writer or In-System Programming (ISP). The high-quality Flash suitable for re-programming and data recording as EEPROM.

1.2 IO Pads

The OB39R32T2 has Four I/O ports: Port 0, Port 1, Port 2 and Port 3. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. As description in section 5.

All the pads for P0, P1, P2 and P3 are with slew rate to reduce EMI. The IO pads can withstand 4KV ESD in human body mode guaranteeing the OB39R32T2's quality in high electro-static environments.

1.3 Instruction timing Selection

The conventional 52-series MCUs are 12T, i.e., 12 oscillator clocks per machine cycle. OB39R32T2 is a 1T to 8T MCU, i.e., its machine cycle is one-clock to eight-clock. In the other words, it can execute one instruction within one clock to only eight clocks.

Mnemonic: CKCON **Address: 8Eh**

7	6	5	4	3	2	1	0	Reset
-	ITS[2:0]			-	-	CLKOUT[1:0]		10H

ITS: Instruction timing select.

ITS [2:0]	Instruction timing
000	1T mode
001	2T mode (default)
010	3T mode
011	4T mode
100	5T mode
101	6T mode
110	7T mode
111	8T mode

The default is in 2T mode, and it can be changed to another Instruction timing mode if CKCON [6:4] (at address 8Eh) is change any time. Not every instruction can be executed with one machine cycle. The exact machine cycle number for all the instructions are given in the next section.

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1.4 Clock Out Selection

The OB39R32T2 can generate a clock out signal at P3.4. The CKCON [1:0] (at address 8Eh) can change any time.

CLKOUT: Clock output select.

CKCON [1:0]	Mode.
00	GPIO(default)
01	Fosc
10	Fosc/2
11	Fosc/4

1.5 RESET

1.5.1 Hardware RESET function

OB39R32T2 provides Internal reset circuit inside, the Internal reset time can set by writer or ISP.

Internal Reset time
200ms
100ms
50ms
25ms
16ms
8ms(default)
4ms

1.5.2 Software RESET function

OB39R32T2 provides one software reset mechanism to reset whole chip. To perform a software reset, the firmware must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the Software Reset register (SWRES) write attribute. After SWRES register obtain the write authority, the firmware can write FFh to the SWRES register. The hardware will decode a reset signal that “OR” with the other hardware reset. The SWRES register is self-reset at the end of the software reset procedure.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Software Reset function											
RSTS	Reset status register	A1h	-	-	-	-	WDTRF	SWRF	LVRF	PORF	00H
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
SWRES	Software Reset register	E7h	SWRES [7:0]								00H

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1.5.3 Reset status

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	WDTRF	SWRF	LVRF	PORF	00H

WDTRF: Watchdog timer reset flag.

When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software.

SWRF: Software reset flag.

When MCU is reset by software, SWRF flag will be set to one by hardware. This flag clear by software.

LVRF: Low voltage reset flag.

When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.

PORF: Power on reset flag.

When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

1.5.4 Time Access Key register (TAKEY)

Mnemonic: TAKEY **Address:F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Software reset register (SWRES) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the SWRES register write attribute.

That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

1.5.5 Software Reset register (SWRES)

Mnemonic: SWRES **Address:E7H**

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Reset**
SWRES [7:0]								00H

SWRES [7:0]: Software reset register bit. These 8-bit is self-reset at the end of the reset procedure.

SWRES [7:0] = FFh, software reset.

SWRES [7:0] = 00h ~ FEh, MCU no action.

1.5.6 Example of software reset

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah     ; enable SWRES write attribute
MOV SWRES, #0FFh ; software reset MCU
```

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1.6 Clocks

The default clock is the 22.1184MHz Internal OSC. This clock is used during the initialization stage. The major work of the initialization stage is to determine the clock source used in normal operation.

The internal clock sources are from the internal OSC with difference frequency division As shown in Table 1-1, the clock source can set by writer.

Table 1-1: Selection of clock source

Clock source
22.1184MHz from internal OSC
11.0592MHz from internal OSC
5.5296MHz from internal OSC
2.7648MHz from internal OSC
1.3824MHz from internal OSC

There may be having a little variance in the frequency from the internal OSC. The max variance as giving in Table 1-2.

Table 1-2: Temperature with variance

Temperature	Max Variance
25℃	±2%

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2. Instruction Set

All OB39R32T2 instructions are binary code compatible and perform the same functions as they do with the industry standard 8051. The following tables give a summary of the instruction set cycles of the OB39R32T2 Microcontroller core.

Table 2-1: Arithmetic operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	28-2F	1	1
ADD A,direct	Add direct byte to accumulator	25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	26-27	1	2
ADD A,#data	Add immediate data to accumulator	24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	38-3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	36-37	1	2
ADDC A,#data	Add immediate data to A with carry flag	34	2	2
SUBB A,Rn	Subtract register from A with borrow	98-9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	96-97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	94	2	2
INC A	Increment accumulator	04	1	1
INC Rn	Increment register	08-0F	1	2
INC direct	Increment direct byte	05	2	3
INC @Ri	Increment indirect RAM	06-07	1	3
INC DPTR	Increment data pointer	A3	1	1
DEC A	Decrement accumulator	14	1	1
DEC Rn	Decrement register	18-1F	1	2
DEC direct	Decrement direct byte	15	2	3
DEC @Ri	Decrement indirect RAM	16-17	1	3
MUL AB	Multiply A and B	A4	1	5
DIV	Divide A by B	84	1	5
DA A	Decimal adjust accumulator	D4	1	1

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Table 2-2: Logic operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	58-5F	1	1
ANL A,direct	AND direct byte to accumulator	55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	56-57	1	2
ANL A,#data	AND immediate data to accumulator	54	2	2
ANL direct,A	AND accumulator to direct byte	52	2	3
ANL direct,#data	AND immediate data to direct byte	53	3	4
ORL A,Rn	OR register to accumulator	48-4F	1	1
ORL A,direct	OR direct byte to accumulator	45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	46-47	1	2
ORL A,#data	OR immediate data to accumulator	44	2	2
ORL direct,A	OR accumulator to direct byte	42	2	3
ORL direct,#data	OR immediate data to direct byte	43	3	4
XRL A,Rn	Exclusive OR register to accumulator	68-6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	66-67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	63	3	4
CLR A	Clear accumulator	E4	1	1
CPL A	Complement accumulator	F4	1	1
RL A	Rotate accumulator left	23	1	1
RLC A	Rotate accumulator left through carry	33	1	1
RR A	Rotate accumulator right	03	1	1
RRC A	Rotate accumulator right through carry	13	1	1
SWAP A	Swap nibbles within the accumulator	C4	1	1

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Table 2-3: Data transfer

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	E8-EF	1	1
MOV A,direct	Move direct byte to accumulator	E5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	E6-E7	1	2
MOV A,#data	Move immediate data to accumulator	74	2	2
MOV Rn,A	Move accumulator to register	F8-FF	1	2
MOV Rn,direct	Move direct byte to register	A8-AF	2	4
MOV Rn,#data	Move immediate data to register	78-7F	2	2
MOV direct,A	Move accumulator to direct byte	F5	2	3
MOV direct,Rn	Move register to direct byte	88-8F	2	3
MOV direct1,direct2	Move direct byte to direct byte	85	3	4
MOV direct,@Ri	Move indirect RAM to direct byte	86-87	2	4
MOV direct,#data	Move immediate data to direct byte	75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	F6-F7	1	3
MOV @Ri,direct	Move direct byte to indirect RAM	A6-A7	2	5
MOV @Ri,#data	Move immediate data to indirect RAM	76-77	2	3
MOV DPTR,#data16	Load data pointer with a 16-bit constant	90	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	93	1	3
MOVC A,@A+PC	Move code byte relative to PC to accumulator	83	1	3
MOVX A,@Ri	Move external RAM (8-bit addr) to A	E2-E3	1	3
MOVX A,@DPTR	Move external RAM (16-bit addr) to A	E0	1	3
MOVX @Ri,A	Move A to external RAM (8-bit addr)	F2-F3	1	4
MOVX @DPTR,A	Move A to external RAM (16-bit addr)	F0	1	4
PUSH direct	Push direct byte onto stack	C0	2	4
POP direct	Pop direct byte from stack	D0	2	3
XCH A,Rn	Exchange register with accumulator	C8-CF	1	2
XCH A,direct	Exchange direct byte with accumulator	C5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator	C6-C7	1	3
XCHD A,@Ri	Exchange low-order nibble indir. RAM with A	D6-D7	1	3

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Table 2-4: Program branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	xxx11	2	6
LCALL addr16	Long subroutine call	12	3	6
RET	from subroutine	22	1	4
RETI	from interrupt	32	1	4
AJMP addr11	Absolute jump	xxx01	2	3
LJMP addr16	Long iump	02	3	4
SJMP rel	Short jump (relative addr.)	80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	73	1	2
JZ rel	Jump if accumulator is zero	60	2	3
JNZ rel	Jump if accumulator is not zero	70	2	3
JC rel	Jump if carry flag is set	40	2	3
JNC	Jump if carry flag is not set	50	2	3
JB bit,rel	Jump if direct bit is set	20	3	4
JNB bit,rel	Jump if direct bit is not set	30	3	4
JBC bit,direct rel	Jump if direct bit is set and clear bit	10	3	4
CJNE A,direct rel	Compare direct byte to A and jump if not equal	B5	3	4
CJNE A,#data rel	Compare immediate to A and jump if not equal	B4	3	4
CJNE Rn,#data rel	Compare immed. to reg. and jump if not equal	B8-BF	3	4
CJNE @Ri,#data rel	Compare immed. to ind. and jump if not equal	B6-B7	3	4
DJNZ Rn,rel	Decrement register and jump if not zero	D8-DF	2	3
DJNZ direct,rel	Decrement direct byte and jump if not zero	D5	3	4
NOP	No operation	00	1	1

Table 2-5: Boolean manipulation

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	C3	1	1
CLR bit	Clear direct bit	C2	2	3
SETB C	Set carry flag	D3	1	1
SETB bit	Set direct bit	D2	2	3
CPL C	Complement carry flag	B3	1	1
CPL bit	Complement direct bit	B2	2	3
ANL C,bit	AND direct bit to carry flag	82	2	2
ANL C,/bit	AND complement of direct bit to carry	B0	2	2
ORL C,bit	OR direct bit to carry flag	72	2	2
ORL C,/bit	OR complement of direct bit to carry	A0	2	2
MOV C,bit	Move direct bit to carry flag	A2	2	2
MOV bit,C	Move carry flag to direct bit	92	2	3

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3. Memory Structure

The OB39R32T2 memory structure follows general 8052 structure. It is 32KB+8KB program memory.

3.1 Program Memory

The OB39R32T2 has 32KB+8KB on-chip flash memory which can be used as general program memory or EEPROM, on which include up to 8K byte specific ISP service program memory space. The address range for the 32K byte is $0000 to $7FFF. The address range for the ISP service program is $D800 to $F7FF. The ISP service program size can be partitioned as N blocks of 1KB (N=0 to 8). When N=0 means no ISP service program space available, total 8K byte memory used as program memory. When N=1 means address $F400 to $F7FF reserved for ISP service program. When N=2 means memory address $F000 to $F7FF reserved for ISP service program…etc. Value N can be set and programmed into OB39R32T2 information block by writer. As shown in Fig. 3-1

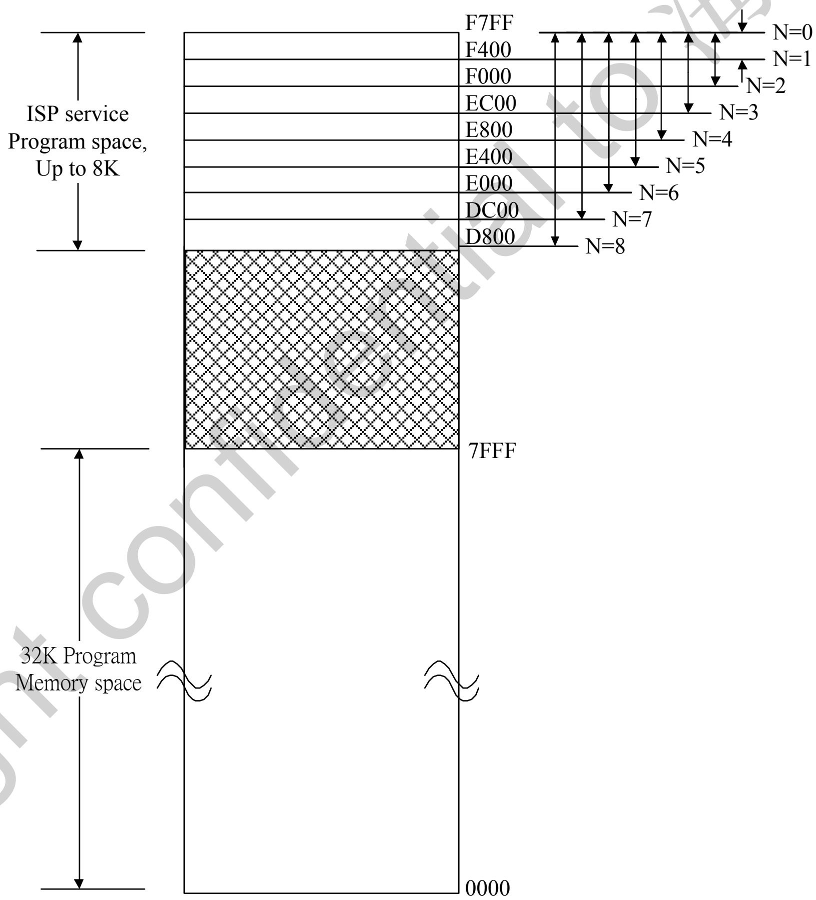

Fig. 3-1: OB39R32T2 programmable Flash

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3.2 Data Memory

The OB39R32T2 has 1152 + 256B on-chip RAM, 256B of it are the same as general 8052 internal memory structure while the expanded 1152 Bytes on-chip SRAM can be accessed by external memory addressing method (by instruction MOVX.). As shown in Fig. 3-2

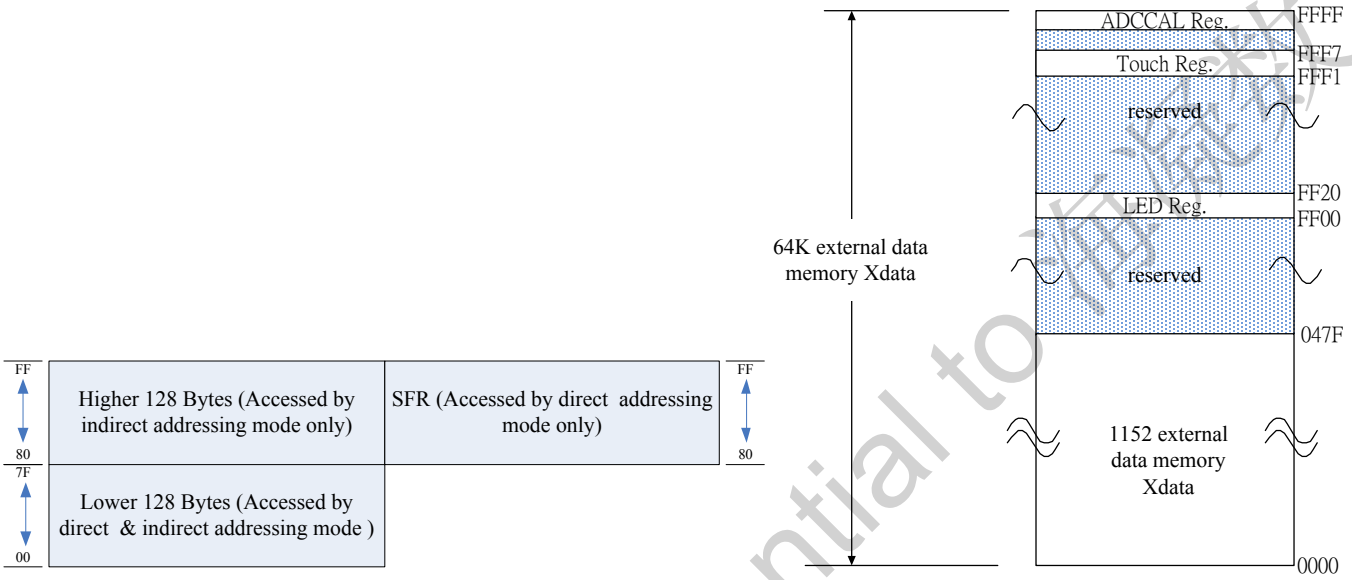

Fig. 3-2: RAM architecture

3.3 Data memory - lower 128 byte (00h to 7Fh)

Data memory 00h to FFh is the same as 8052.
The address 00h to 7Fh can be accessed by direct and indirect addressing modes.
Address 00h to 1Fh is register area.
Address 20h to 2Fh is memory bit area.
Address 30h to 7Fh is for general memory area.

3.4 Data memory - higher 128 byte (80h to FFh)

The address 80h to FFh can be accessed by indirect addressing mode.
Address 80h to FFh is data area.

3.5 Data memory - Expanded 1152 bytes ($0000 to $047F)

From external address 0000h to 047Fh is the on-chip expanded SRAM area, total 1152 Bytes. This area can be accessed by external direct addressing mode (by instruction MOVX).

The address space of instruction MOVX @Ri, i=0, 1 is determined by RCON [3:0] of special function register 86h RCON (internal RAM control register). The default setting of RCON [3:0] is 00h (page0). One page of data RAM is 256 bytes.

MOVX @Ri, A MOVX A,@Ri	0 ≦ RCON[7:0] ≦ 2

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4. CPU Engine

The OB39R32T2 engine is composed of four components:

(1) Control unit
(2) Arithmetic – logic unit
(3) Memory control unit
(4) RAM and SFR control unit

The OB39R32T2 engine allows to fetch instruction from program memory and to execute using RAM or SFR. The following chapter describes the main engine register.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
8051 Core											
ACC	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00H
B	B register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00H
PSW	Program status word	D0h	CY	AC	F0	RS[1:0]		OV	PSW.1	P	00H
SP	Stack Pointer	81h	SP[7:0]								07H
DPL	Data pointer low 0	82h	DPL[7:0]								00H
DPH	Data pointer high 0	83h	DPH[7:0]								00H
DPL1	Data pointer low 1	84h	DPL1[7:0]								00H
DPH1	Data pointer high 1	85h	DPH1[7:0]								00H
AUX	Auxiliary register	91h	BRGS	-	-	-	IIC1S	UR1S	UR0S	DPS	00H
CKCON	Clock control register	8Eh	-	ITS[2:0]			-	-	CLKOUT[1:0]		10H
IFCON	Interface control register	8Fh	-	CDPR	-	-	-	-	-	ISPE	00H

4.1 Accumulator

ACC is the Accumulator register. Most instructions use the accumulator to store the operand.

Mnemonic: ACC **Address: E0h**

7	6	5	4	3	2	1	0	Reset
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h

ACC[7:0]: The A (or ACC) register is the standard 8052 accumulator。

4.2 B Register

The B register is used during multiply and divide instructions. It can also be used as a scratch pad register to store temporary data.

Mnemonic: B **Address: F0h**

7	6	5	4	3	2	1	0	Reset
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h

B[7:0]: The B register is the standard 8052 register that serves as a second accumulator.

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4.3 Program Status Word

Mnemonic: PSW **Address: D0h**

7	6	5	4	3	2	1	0	Reset
CY	AC	F0	RS [1:0]		OV	F1	P	00h

CY: Carry flag.

AC: Auxiliary Carry flag for BCD operations.

F0: General purpose Flag 0 available for user.

RS[1:0]: Register bank select, used to select working register bank.

RS[1:0]	Bank Selected	Location
00	Bank 0	00h – 07h
01	Bank 1	08h – 0Fh
10	Bank 2	10h – 17h
11	Bank 3	18h – 1Fh

OV: Overflow flag.

F1: General purpose Flag 1 available for user.

P: Parity flag, affected by hardware to indicate odd/even number of “one” bits in the Accumulator, i.e. even parity.

4.4 Stack Pointer

The stack pointer is a 1-byte register initialized to 07h after reset. This register is incremented before PUSH and CALL instructions, causing the stack to start from location 08h.

Mnemonic: SP **Address: 81h**

7	6	5	4	3	2	1	0	Reset
SP [7:0]								07h

SP[7:0]: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

4.5 Data Pointer

The data pointer (DPTR) is 2-bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (e.g. MOV DPTR, #data16) or as two separate registers (e.g. MOV DPL,#data8). It is generally used to access the external code or data space (e.g. MOVC A, @A+DPTR, @DPTR respectively).

Mnemonic: DPL **Address: 82h**

7	6	5	4	3	2	1	0	Reset
DPL [7:0]								00h

DPL[7:0]: Data pointer Low 0

Mnemonic: DPH **Address: 83h**

7	6	5	4	3	2	1	0	Reset
DPH [7:0]								00h

DPH [7:0]: Data pointer High 0

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4.6 Data Pointer 1

The Dual Data Pointer accelerates the moves of data block. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the OB39R32T2 core the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located in LSB of AUX register (DPS).

The user switches between pointers by toggling the LSB of AUX register. All DPTR-related instructions use the currently selected DPTR for any activity.

Mnemonic: DPL1 **Address: 84h**

7	6	5	4	3	2	1	0	Reset
DPL1 [7:0]								00h

DPL1[7:0]: Data pointer Low 1

Mnemonic: DPH1 **Address: 85h**

7	6	5	4	3	2	1	0	Reset
DPH1 [7:0]								00h

DPH1[7:0]: Data pointer High 1

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	-	IIC1S	UR1S	UR0S	DPS	00H

DPS: Data Pointer selected register.

DPS = 1 – Selected DPTR1.

4.7 Clock control register

Mnemonic: CKCON **Address: 8Eh**

7	6	5	4	3	2	1	0	Reset
-	ITS[2:0]			-	-	CLKOUT[1:0]		10H

ITS[2:0]: Instruction timing select.

ITS [2:0]	Mode
000	1T mode
001	2T mode (default)
010	3T mode
011	4T mode
100	5T mode
101	6T mode
110	7T mode
111	8T mode

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CLKOUT: Clock output select.

CKCON [1:0]	Mode.
00	GPIO(default)
01	Fosc
10	Fosc/2
11	Fosc/4

4.8 Interface control register

Mnemonic: IFCON **Address: 8Fh**

7	6	5	4	3	2	1	0	Reset
-	CDPR	-	-	-	-	-	ISPE	00H

CDPR: Code protect (Read Only)

ISPE: ISP function enable bit.

ISPE = 1, enable ISP function

ISPE = 0, disable ISP function

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5. GPIO

The OB39R32T2 has four I/O ports: Port 0, Port 1, Port 2, Port 3. Ports 0, 1, 2 are 8-bit ports ,Ports 2 are 7-bit ports , and Ports 3 are 6-bit ports. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin. All I/O port pins on the OB39R32T2 may be configured by software to one fo four types on a pin-by-pin basis, shown as below:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
I/O port function register											
P0M0	Port 0 output mode 0	D2h	P0M0 [7:0]								~OP40
P0M1	Port 0 output mode 1	D3h	P0M1[7:0]								~OP48
P1M0	Port 1 output mode 0	D4h	P1M0[7:0]								~OP41
P1M1	Port 1 output mode 1	D5h	P1M1[7:0]								~OP49
P2M0	Port 2 output mode 0	D6h	-	P2M0[6:0]							~OP42
P2M1	Port 2 output mode 1	D7h	-	P2M1[6:0]							~OP4A
P3M0	Port 3 output mode 0	DAh	-	P3M0[6:0]							~OP43
P3M1	Port 3 output mode 1	DBh	-	P3M1[6:0]							~OP4B

*OP40~OP43, OP48~OP4B by writer programming set.

PxM1.y	PxM0.y	Port output mode
0	0	Quasi-bidirectional (standard 8051 port outputs) (pull-up)
0	1	Push-pull
1	0	Input only (high-impedance)
1	1	Open drain

For general-purpose applications, every pin can be assigned to either high or low independently. As shown below:

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Ports											
Port 3	Port 3	B0h	-	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	OP53
Port 2	Port 2	A0h	-	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	OP52
Port 1	Port 1	90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	OP51
Port 0	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	OP50

OP50~OP53 by writer programming set.

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Mnemonic: P0 **Address: 80h**

7	6	5	4	3	2	1	0	Reset
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	OP50

P0.7~ 0: Port0 [7] ~ Port0[0]

Mnemonic: P1 **Address: 90h**

7	6	5	4	3	2	1	0	Reset
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	OP51

P1.7~ 0: Port1 [7] ~ Port1 [0]

Mnemonic: P2 **Address: A0h**

7	6	5	4	3	2	1	0	Reset
-	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	OP52

P2.6~ 0: Port2 [6] ~ Port2 [0]

Mnemonic: P3 **Address: B0h**

7	6	5	4	3	2	1	0	Reset
-	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	OP53

P3.6~ 0: Port3 [6] ~ Port3 [0]

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6. Timer 0, Timer 1 and Timer 3

The OB39R32T2 has four 16-bit timer/counter registers: Timer 0, Timer 1, Timer 2 and Timer 3. All can be configured for counter or timer operations.

In timer mode, the Timer 0 register, Timer 1 register or Timer 3 register is incremented every 1/12/96 machine cycles, which means that it counts up after every 1/12/96 periods of the clk signal. It's dependent on SFR(PFCON).

In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Timer 0, Timer 1 and Timer 3											
TL0	Timer 0 , low byte	8Ah	TL0[7:0]								00H
TH0	Timer 0 , high byte	8Ch	TH0[7:0]								00H
TL1	Timer 1 , low byte	8Bh	TL1[7:0]								00H
TH1	Timer 1 , high byte	8Dh	TH1[7:0]								00H
TL3	Timer 3 , low byte	94h	TL3[7:0]								00H
TH3	Timer 3 , high byte	95h	TH3[7:0]								00H
TMOD	Timer Mode Control	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
T3MOD	Timer 3 Mode Control	92h	-	T3CS	T1CS	T0CS	GATE	C/T	M1	M0	00H
TCON1	Timer/Counter Control 1	D8h	-	-	TF3	TR3	IE3	IT3	IE2	IT2	00H
TCON0	Timer/Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
ENHIT	ENHance Interrupt Type Register	E5h	ENHIT3[1:0]		ENHIT2[1:0]		ENHIT1[1:0]		ENHIT0[1:0]		00H
INTDEG	External Interrupt Deglitch register	EEh	INT3DEG[1:0]		INT2DEG[1:0]		INT1DEG[1:0]		INT0DEG[1:0]		00H
PFCON	Peripheral Frequency control register	D9h	-	-	T3PS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

6.1 Timer/Counter mode control register (TMOD)

Mnemonic: TMOD **Address: 89h**

7	6	5	4	3	2	1	0	Reset
GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
Timer 1				Timer 0				

GATE: If set, enables external gate control (pin INT0 or INT1 for Counter 0 or 1, respectively). When INT0 or INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on T0 or T1 input pin.

C/T: Selects Timer or Counter operation. When set to 1, a counter operation is performed, when cleared to 0, the corresponding register will function as a timer.

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M1	M0	Mode	Function
0	0	Mode0	13-bit counter/timer, with 5 lower bits in TL0 or TL1 register and 8 bits in TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are hold at zero.
0	1	Mode1	16-bit counter/timer.
1	0	Mode2	8-bit auto-reload counter/timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.
1	1	Mode3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8 bit timers / counters.

6.2 Timer/counter 3 mode control register (T3MOD)

Mnemonic: T3MOD **Address: 92h**

7	6	5	4	3	2	1	0	Reset
-	T3CS	T1CS	T0CS	GATE	C/T	M1	M0	00h
				Timer 3				

T3CS: Timer3 Counter input select:
0: External T3 pin
1: XTAL 32K/8
T1CS: Timer1 Counter input select:
0: External T1 pin
1: XTAL 32K/8
T0CS: Timer0 Counter input select:
0: External T0 pin
1: XTAL 32K/8

GATE: If set, enables external gate control (pin INT3 for Counter 3). When INT3 is high, and TR3 bit is set (see TCON1 register), a counter is incremented every falling edge on T3 input pin

C/T: Selects Timer or Counter operation. When set to 1, a counter operation is performed, when cleared to 0, the corresponding register will function as a timer.

M1	M0	Mode	Function
0	0	Mode0	13-bit counter/timer, with 5 lower bits in TL3 register and 8 bits in TH3 register. The 3 high order bits of TL3 and TL3 are hold at zero.
0	1	Mode1	16-bit counter/timer.
1	0	Mode2	8 -bit auto-reload counter/timer. The reload value is kept in TH3, while TL3 is incremented every machine cycle. When TL3 overflows, a value from TH3 is copied to TL3.
1	1	-	Reserved

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6.3 Timer/counter control register 0(TCON0)

Mnemonic: TCON0 **Address: 88h**

7	6	5	4	3	2	1	0	Reset
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

TF1: Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR1: Timer 1 Run control bit. If cleared, Timer 1 stops.

TF0: Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR0: Timer 0 Run control bit. If cleared, Timer 0 stops.

IE1: Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.

IT1: IT1=0: INT1 select level trigger.(high or low dependent on ENHIT1)
IT1=1: INT1 select edge trigger.(falling or rising or both edge dependent on ENHIT1).

IE0: Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT0 is observed. Cleared when interrupt is processed.

IT0: IT0=0: INT0 select level trigger.(high or low dependent on ENHIT0)
IT0=1: INT0 select edge trigger.(falling or rising or both edge dependent on ENHIT0)

6.4 Timer/counter control register (TCON1)

Mnemonic: TCON1 **Address: D8h**

7	6	5	4	3	2	1	0	Reset
-	-	TF3	TR3	IE3	IT3	IE2	IT2	00h

TF3: Timer 3 overflow flag set by hardware when Timer 3 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR3: Timer 3 Run control bit. If cleared, Timer 3 stops.

IE3: Interrupt 3 flag. Set by hardware, when falling edge on external pin INT3 is observed. Cleared when interrupt is processed.

IT3: IT3=0: INT3 select level trigger.(high or low dependent on ENHIT3)
IT3=1: INT3 select edge trigger.(falling or rising or both edge dependent on ENHIT3)

IE2: Interrupt 2 flag. Set by hardware, when falling edge on external pin INT2 is

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observed. Cleared when interrupt is processed.

IT2: IT2=0: INT2 select level trigger.(high or low dependent on ENHIT2)

IT2=1: INT2 select edge trigger.(falling or rising or both edge dependent on ENHIT2)

6.5 ENHance Interrupt Type Register (ENHIT)

Mnemonic: ENHIT **Address: E5h**

7	6	5	4	3	2	1	0	Reset
ENHIT3[1:0]		ENHIT2[1:0]		ENHIT1[1:0]		ENHIT0[1:0]		00h

	ENHIT0[1:0]=00	ENHIT0[1:0]=01	ENHIT0[1:0]=10	ENHIT0[1:0]=11
IT0=0	INT0 Low level trigger	INT0 High level trigger	--	--
IT0=1	INT0 Falling edge	INT0 Rising trigger	INT0 Both falling and rising	--

	ENHIT1[1:0]=00	ENHIT1[1:0]=01	ENHIT1[1:0]=10	ENHIT1[1:0]=11
IT1=0	INT1 Low level trigger	INT1 High level trigger	--	--
IT1=1	INT1 Falling edge	INT1 Rising trigger	INT1 Both falling and rising	--

	ENHIT2[1:0]=00	ENHIT2[1:0]=01	ENHIT2[1:0]=10	ENHIT2[1:0]=11
IT2=0	INT2 Low level trigger	INT2 High level trigger	--	--
IT2=1	INT2 Falling edge	INT2 Rising trigger	INT2 Both falling and rising	--

	ENHIT3[1:0]=00	ENHIT3[1:0]=01	ENHIT3[1:0]=10	ENHIT3[1:0]=11
IT3=0	INT3 Low level trigger	INT3 High level trigger	--	--
IT3=1	INT3 Falling edge	INT3 Rising trigger	INT3 Both falling and rising	--

6.6 External Interrupt Deglitch Register (INTDEG)

Mnemonic: INTDEG **Address: EEh**

7	6	5	4	3	2	1	0	Reset
INT3DEG[1:0]		INT2DEG[1:0]		INT1DEG[1:0]		INT0DEG[1:0]		00H

INT3DEG[1:0] Select INT3 deglitch time.

00: no deglitch.

01: 5us

10: 10us

11: 15us

INT2DEG[1:0] Select INT2 deglitch time.

00: no deglitch.

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01: 5us

10: 10us

11: 15us

INT1DEG[1:0] Select INT1 deglitch time.

00: no deglitch.

01: 5us

10: 10us

11: 15us

INT0DEG[1:0] Select INT0 deglitch time.

00: no deglitch.

01: 5us

10: 10us

11: 15us

6.7 Peripheral Frequency control register

Mnemonic: PFCON **Address: D9h**

7	6	5	4	3	2	1	0	Reset
-	-	T3PS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

T3PS[1:0]: Timer3 Prescaler select

T3PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

T1PS[1:0]: Timer1 Prescaler select

T1PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

T0PS[1:0]: Timer0 Prescaler select

T0PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

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6.8 Mode 0 (13-bit Counter/Timer)

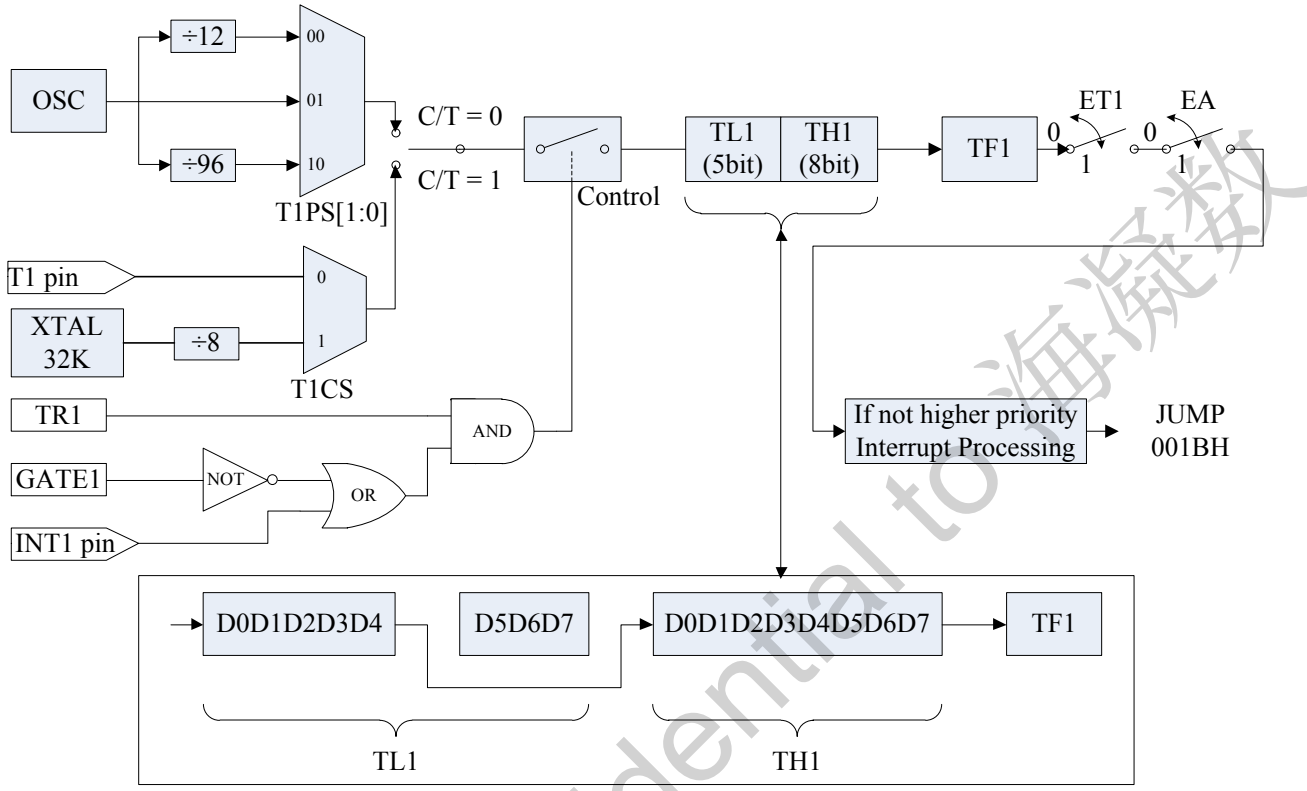

Fig. 6-1: Mode 0 -13 bit Timer / Counter operation

6.9 Mode 1 (16-bit Counter/Timer)

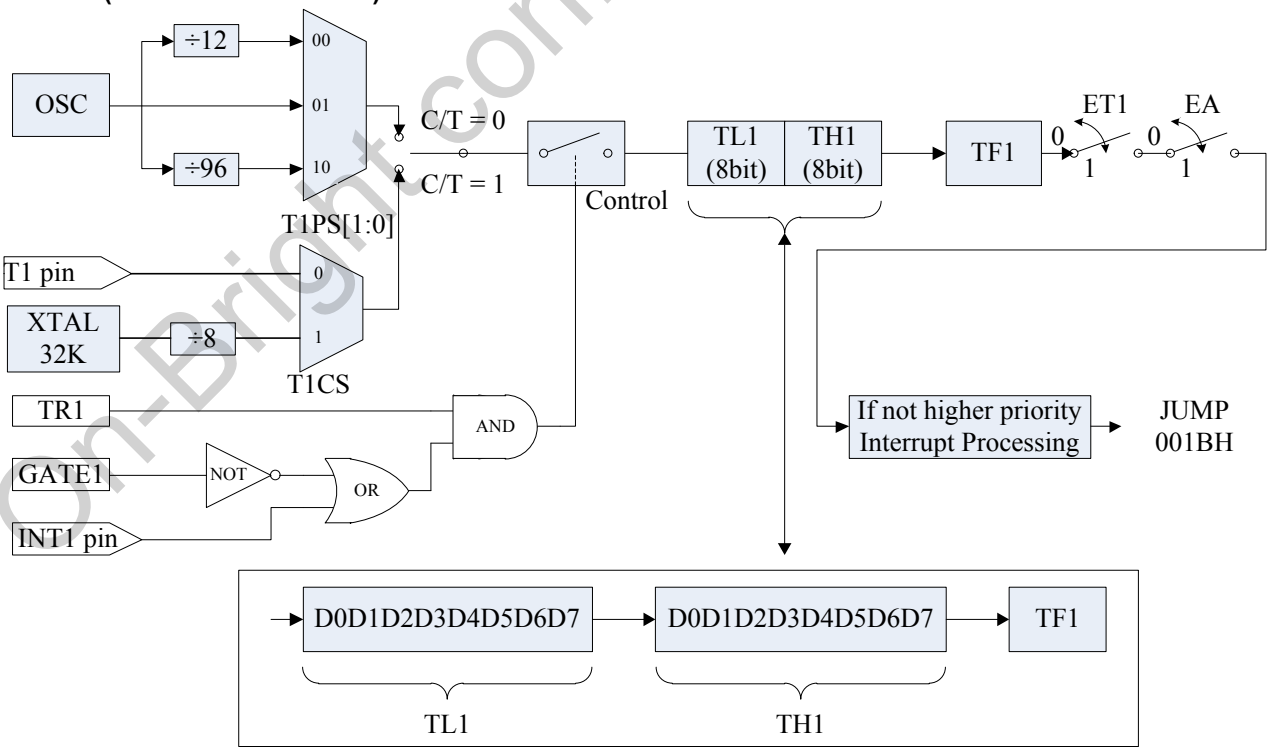

Fig. 6-2: Mode 1 16 bit Counter/Timer operation

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6.10 Mode 2 (8-bit auto-reload Counter/Timer)

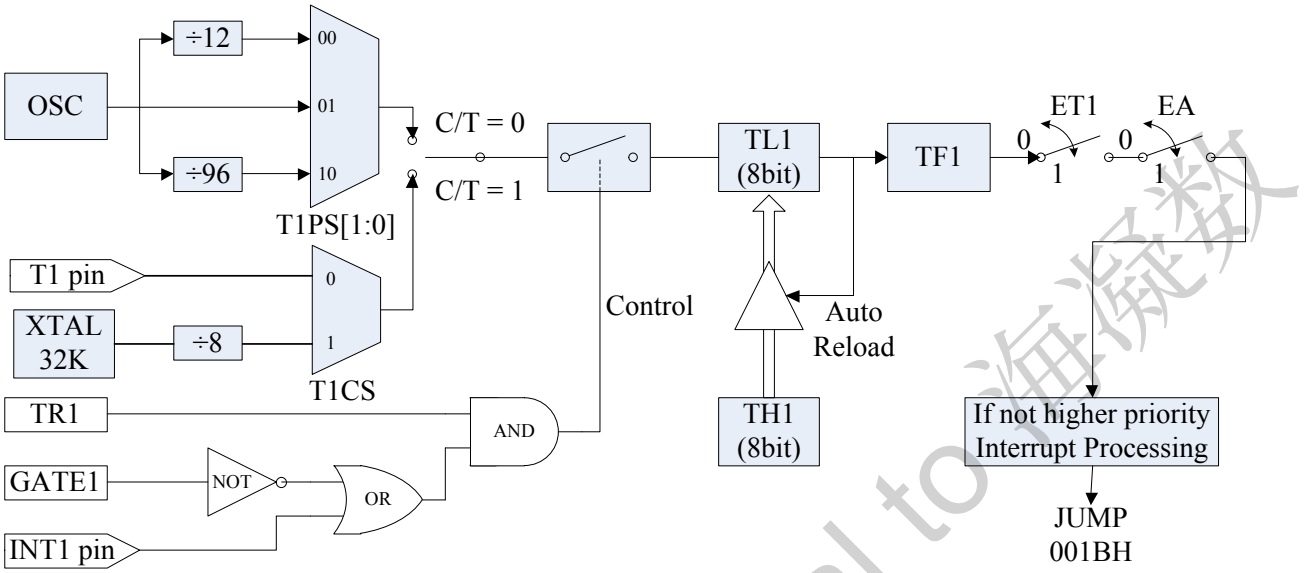

Fig. 6-3: Mode 2 8-bit auto-reload Counter/Timer operation.

6.11 Mode 3 (Timer 0 acts as two independent 8 bit Timers / Counters)

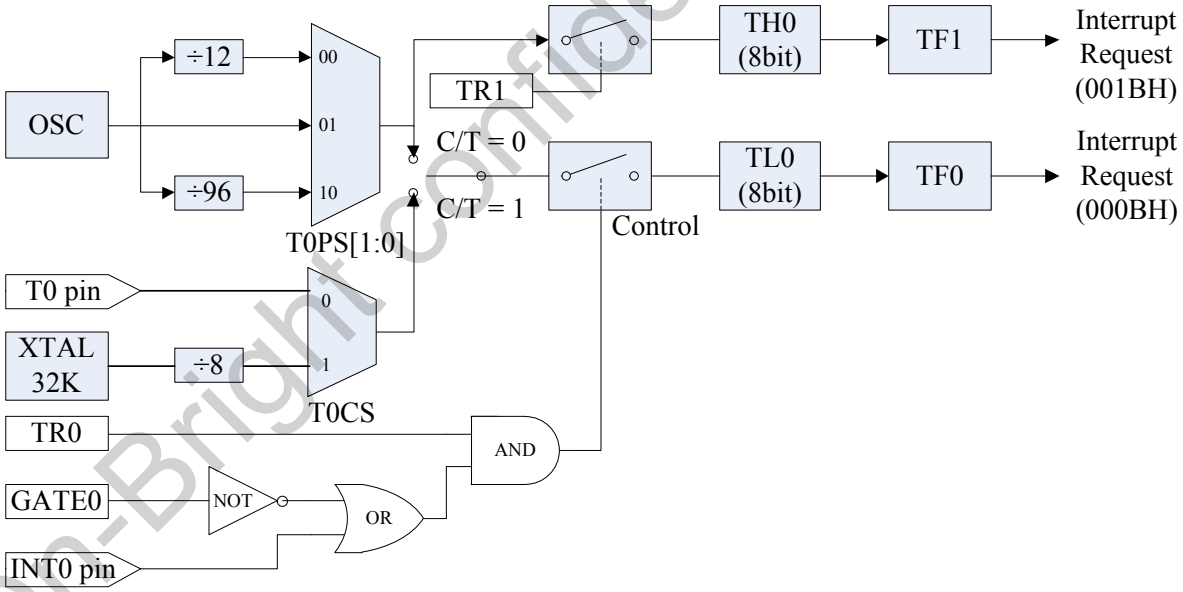

Fig. 6-4: Mode 3 Timer 0 acts as two independent 8 bit Timers / Counters operatin

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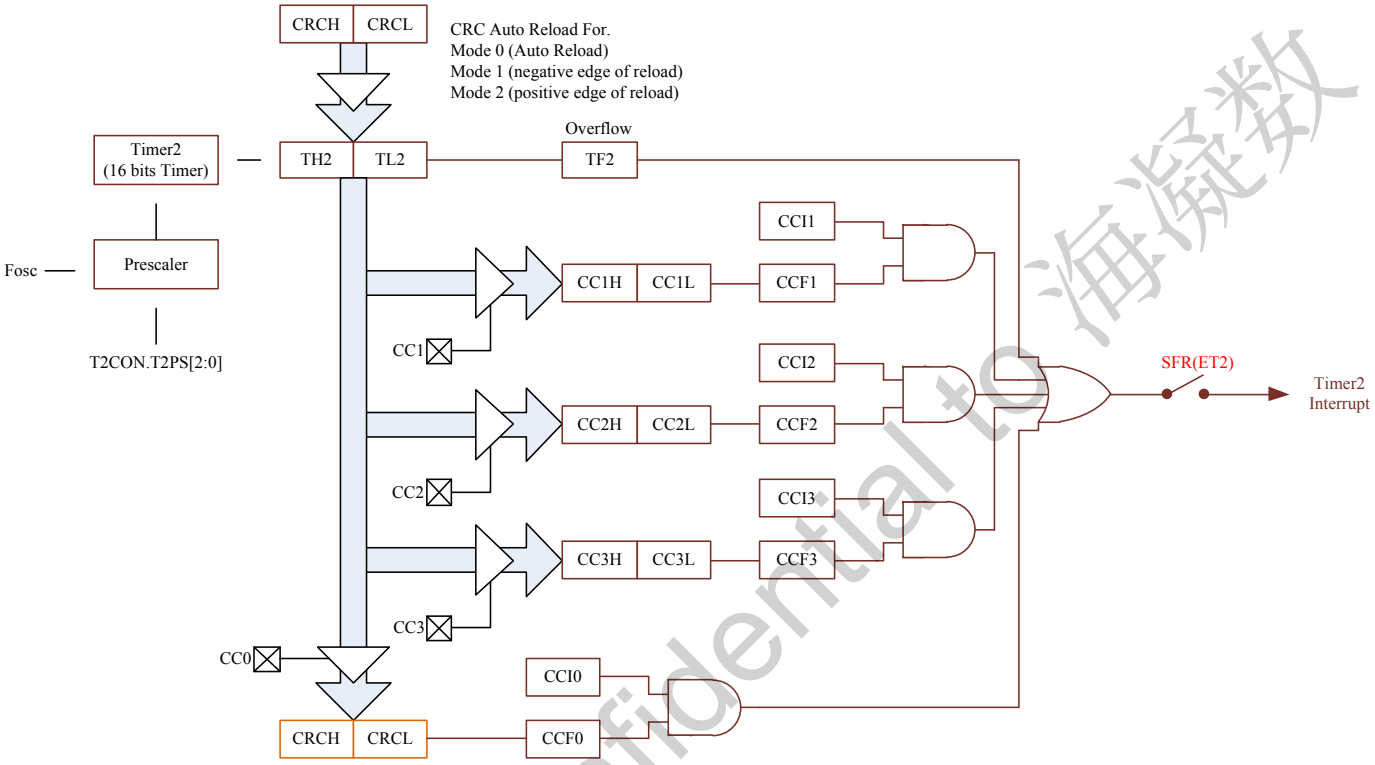
7. Timer 2 and Capture Compare Unit

Timer 2 is not only a 16-bit timer, also a 4-channel unit with compare, capture and reload functions. It is very similar to the programmable counter array (PCA) in some other MCUs except pulse width modulation (PWM).



Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Timer 2 and Capture Compare Unit											
T2CON	Timer 2 control	C8h	T2PS[2:0]			T2R[1:0]		T2CS	T2I[1:0]		00H
CCCON	Compare/Capture Control	C9h	CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H
CCEN	Compare/Capture Enable register	C1h	-	COCAM1[2:0]			-	COCAM0[2:0]			00H
CCEN2	Compare/Capture Enable 2 register	D1h	-	COCAM3[2:0]			-	COCAM2[2:0]			00H
TL2	Timer 2, low byte	CCh	TL2[7:0]								00H
TH2	Timer 2, high byte	CDh	TH2[7:0]								00H
CRCL	Compare/Reload/ Capture register, low byte	CAh	CRCL[7:0]								00H
CRCH	Compare/Reload/ Capture register, high byte	CBh	CRCH[7:0]								00H
CCL1	Compare/Capture register 1, low byte	C2h	CCL1[7:0]								00H
CCH1	Compare/Capture register 1, high byte	C3h	CCH1[7:0]								00H
CCL2	Compare/Capture register 2, low byte	C4h	CCL2[7:0]								00H

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CCH2	Compare/Capture register 2, high byte	C5h	CCH2[7:0]	00H
CCL3	Compare/Capture register 3, low byte	C6h	CCL3[7:0]	00H
CCH3	Compare/Capture register 3, high byte	C7h	CCH3[7:0]	00H

Mnemonic: T2CON **Address: C8h**

7	6	5	4	3	2	1	0	Reset
T2PS[2:0]			T2R[1:0]		T2CS	T2I[1:0]		00H

T2PS[2:0]: Prescaler select bit:

T2PS = 000 – timer 2 is clocked with the oscillator frequency.

T2PS = 001 – timer 2 is clocked with 1/2 of the oscillator frequency.

T2PS = 010 – timer 2 is clocked with 1/4 of the oscillator frequency.

T2PS = 011 – timer 2 is clocked with 1/6 of the oscillator frequency.

T2PS = 100 – timer 2 is clocked with 1/8 of the oscillator frequency.

T2PS = 101 – timer 2 is clocked with 1/12 of the oscillator frequency.

T2PS = 110 – timer 2 is clocked with 1/24 of the oscillator frequency.

T2R[1:0]: Timer 2 reload mode selection

T2R[1:0] = 00 – Reload disabled.

T2R[1:0] = 01 – Mode 2:T2EX Rising Edge Reload.

T2R[1:0] = 10 – Mode 0: Auto Reload.

T2R[1:0] = 11 – Mode 1: T2EX Falling Edge Reload.

T2CS: Timer 2 Counter input select

T2CS = 0 – External T2 pin.

T2CS = 1 – XTAL 32K/8 Hz.

T2I[1:0]: Timer 2 input selection

T2I[1:0] = 00 – Timer 2 stop.

T2I[1:0] = 01 – Input frequency from prescaler (T2PS[2:0]).

T2I[1:0] = 10:

T2CS = 0 – Timer 2 is incremented by external signal at pin T2.

T2CS = 1 – Timer 2 is incremented by XTAL 32K/8 Hz.

T2I[1:0] = 11 – internal clock input is gated to the Timer 2.

Mnemonic: CCCON **Address: C9h**

7	6	5	4	3	2	1	0	Reset
CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H

CCI3: Compare/Capture 3 interrupt control bit.

CCI3 = 1 is enable.

CCI2: Compare/Capture 2 interrupt control bit.

CCI3 = 1 is enable.

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CCI1: Compare/Capture 1 interrupt control bit.

CCI3 = 1 is enable.

CCI0: Compare/Capture 0 interrupt control bit.

CCI3 = 1 is enable.

CCF3: Compare/Capture 3 flag set by hardware. This flag can be cleared by software.

CCF2: Compare/Capture 2 flag set by hardware. This flag can be cleared by software.

CCF1: Compare/Capture 1 flag set by hardware. This flag can be cleared by software.

CCF0: Compare/Capture 0 flag set by hardware. This flag can be cleared by software.

Compare/Capture interrupt share T2 interrupt vector.

Mnemonic: CCEN **Address: C1h**

7	6 5 4	3	2 1 0	Reset
-	COCAM1[2:0]	-	COCAM0[2:0]	00H

COCAM1[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC1.

101 - Capture on falling edge at pin CC1.

110 - Capture on both rising and falling edge at pin CC1.

111 - Capture on write operation into register CC1.

COCAM0[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC0.

101 - Capture on falling edge at pin CC0.

110 - Capture on both rising and falling edge at pin CC0.

111 - Capture on write operation into register CC0.

Mnemonic: CCEN2 **Address: D1h**

7	6 5 4	3	2 1 0	Reset
-	COCAM3[2:0]	-	COCAM2[2:0]	00H

COCAM3[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC3.

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101 - Capture on falling edge at pin CC3.

110 - Capture on both rising and falling edge at pin CC3.

111 - Capture on write operation into register CC3.

COCAM2[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC2.

101 - Capture on falling edge at pin CC2.

110 - Capture on both rising and falling edge at pin CC2.

111 - Capture on write operation into register CC2.

7.1 Timer 2 function

Timer 2 can operate as timer, event counter, or gated timer as explained later.

7.1.1 Timer mode

In this mode Timer 2 can by incremented in various frequency that depending on the prescaler. The prescaler is selected by bit T2PS[2:0] in register T2CON. As shown in Fig. 7-1

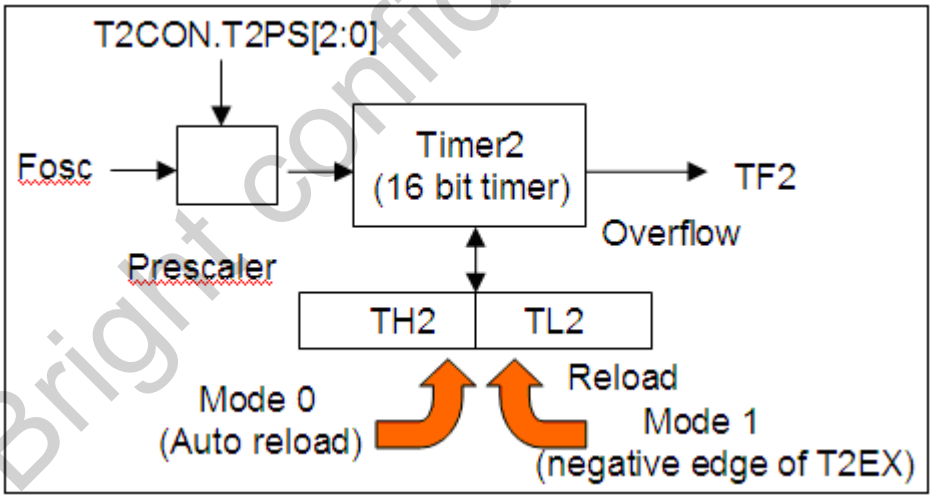

Fig. 7-1: Timer mode and Reload mode function

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7.1.2 Event counter mode

In this mode, the timer is incremented when external signal T2 change value from 1 to 0. The T2 input is sampled in every cycle. Timer 2 is incremented in the cycle following the one in which the transition was detected. As shown in Fig. 7-2.

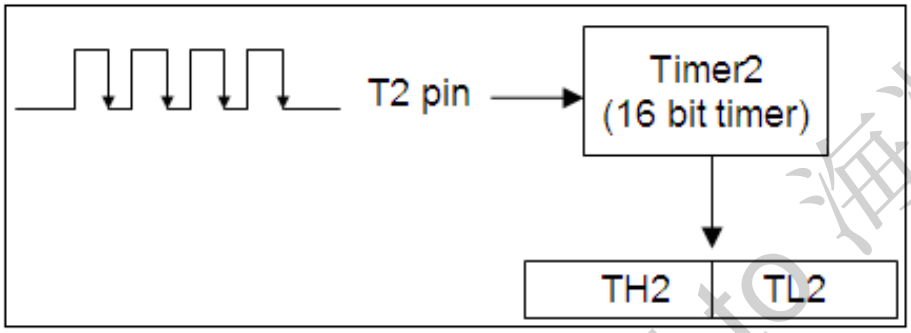

Fig. 7-2: Event counter mode function

7.1.3 Gated timer mode

In this mode, the internal clock which incremented timer 2 is gated by external signal T2. As shown in Fig. 7-3

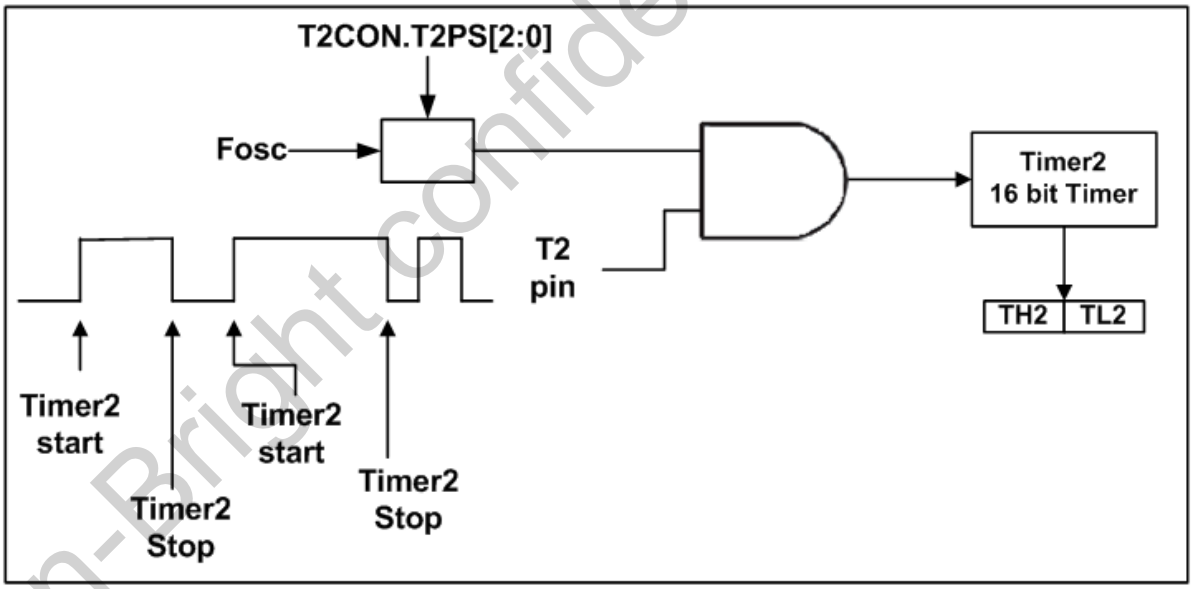

Fig. 7-3: Gated timer mode function

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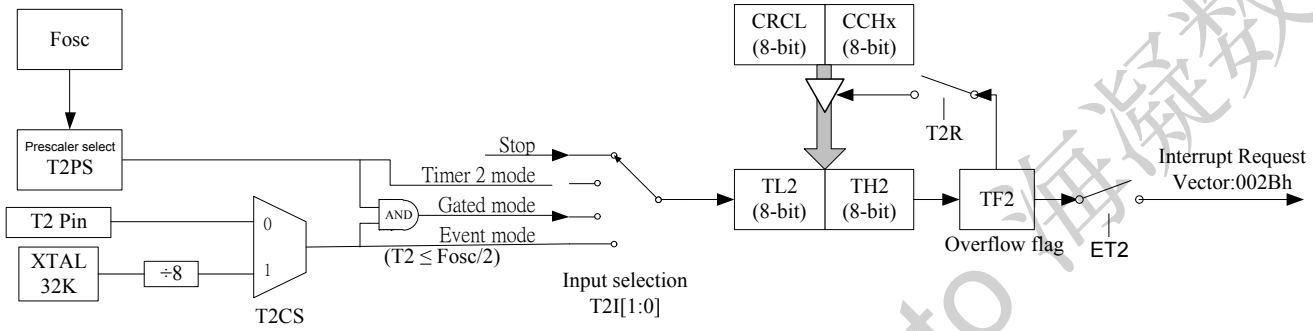
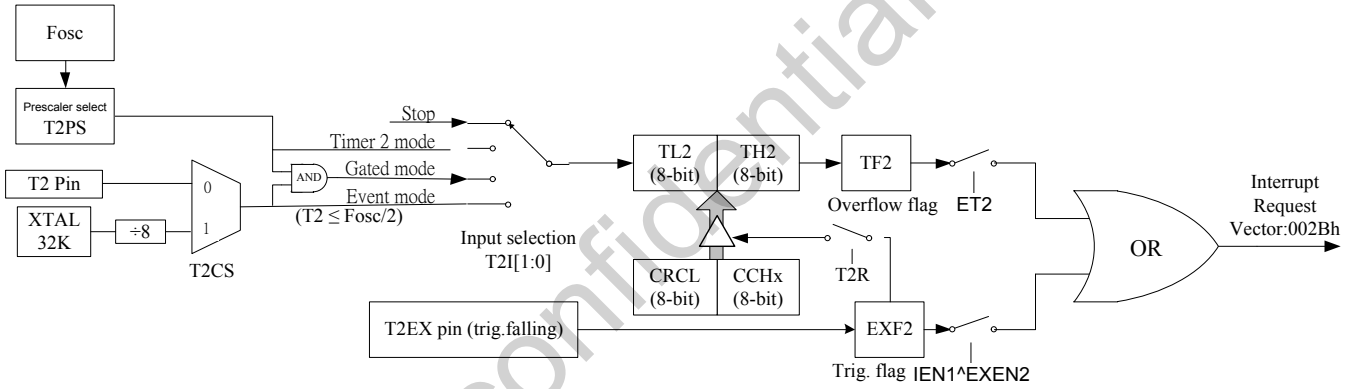
7.1.4 Reload of Timer 2

Reload (16-bit reload from the crc register) can be executed in the following two modes:

Mode 0: Reload signal is generate by a Timer 2 overflows – autoreload.



Mode 1: Reload signal is generate by a negative transition at the corresponding input pin T2EX.



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7.2 Compare function

In the four independent comparators, the value stored in any compare/capture register is compared with the contents of the timer register. The compare modes 0 and 1 are selected by bits C0CAMx. In both compare modes, the results of comparison arrives at Port 1 within the same machine cycle in which the internal compare signal is activated.

7.2.1 Compare Mode 0

In mode 0, when the value in Timer 2 equals the value of the compare register, the output signal changes from low to high. It goes back to a low level on timer overflow. In this mode, writing to the port will have no effect, because the input line from the internal bus and the write-to-latch line are disconnected. As shown in Fig. 7-4 illustrates the function of compare mode 0.

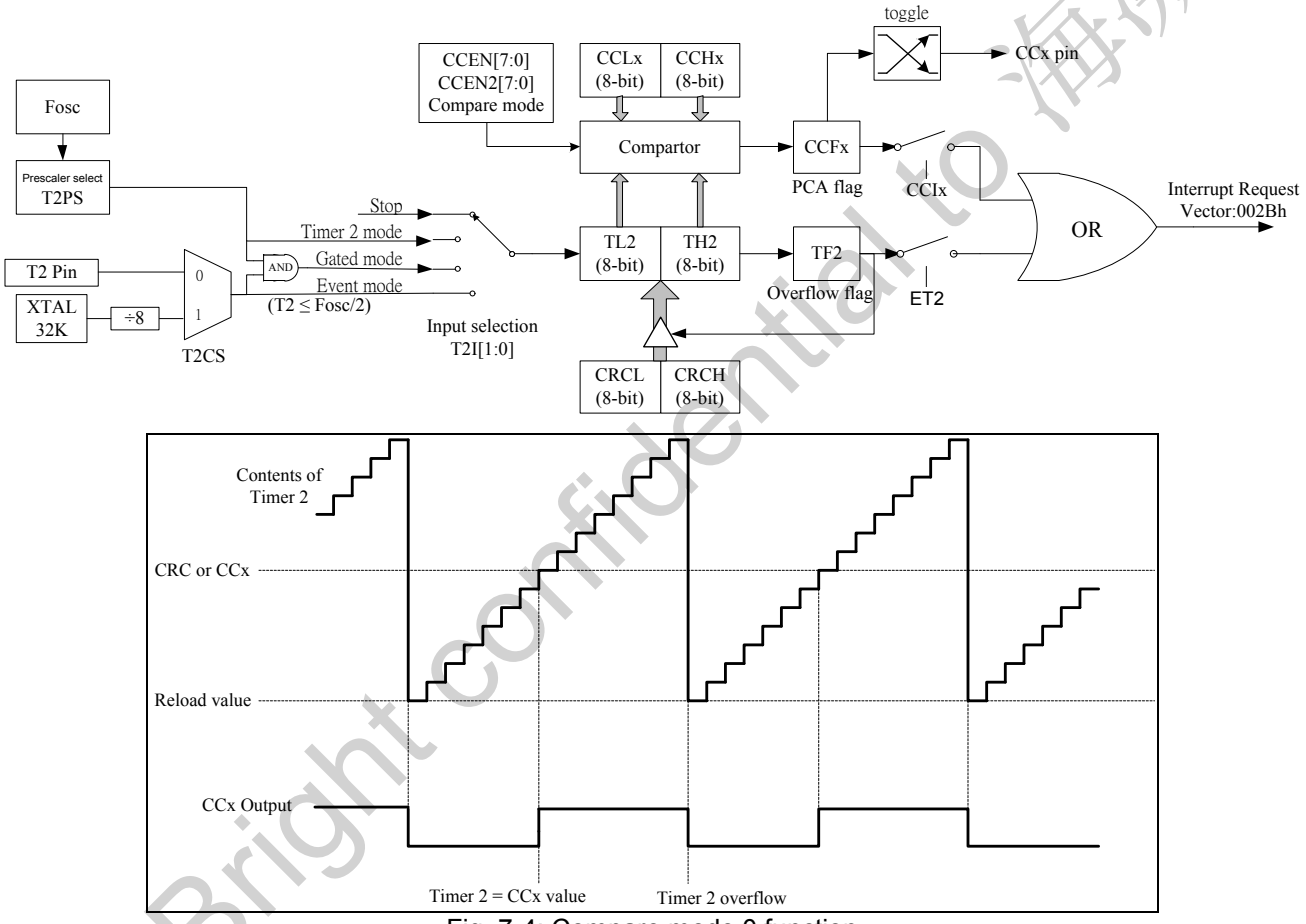

Fig. 7-4: Compare mode 0 function

7.2.2 Compare Mode 1

In compare mode 1, the transition of the output signal can be determined by software. A timer 2 overflow causes no output change. In this mode, both transitions of a signal can be controlled. As shown in Fig. 7-5 and Fig. 7-6 a functional diagram of a register/port configuration in compare Mode 1. In compare Mode 1, the value is written first to the “Shadow Register”, when compare signal is active, this value is transferred to the output register.

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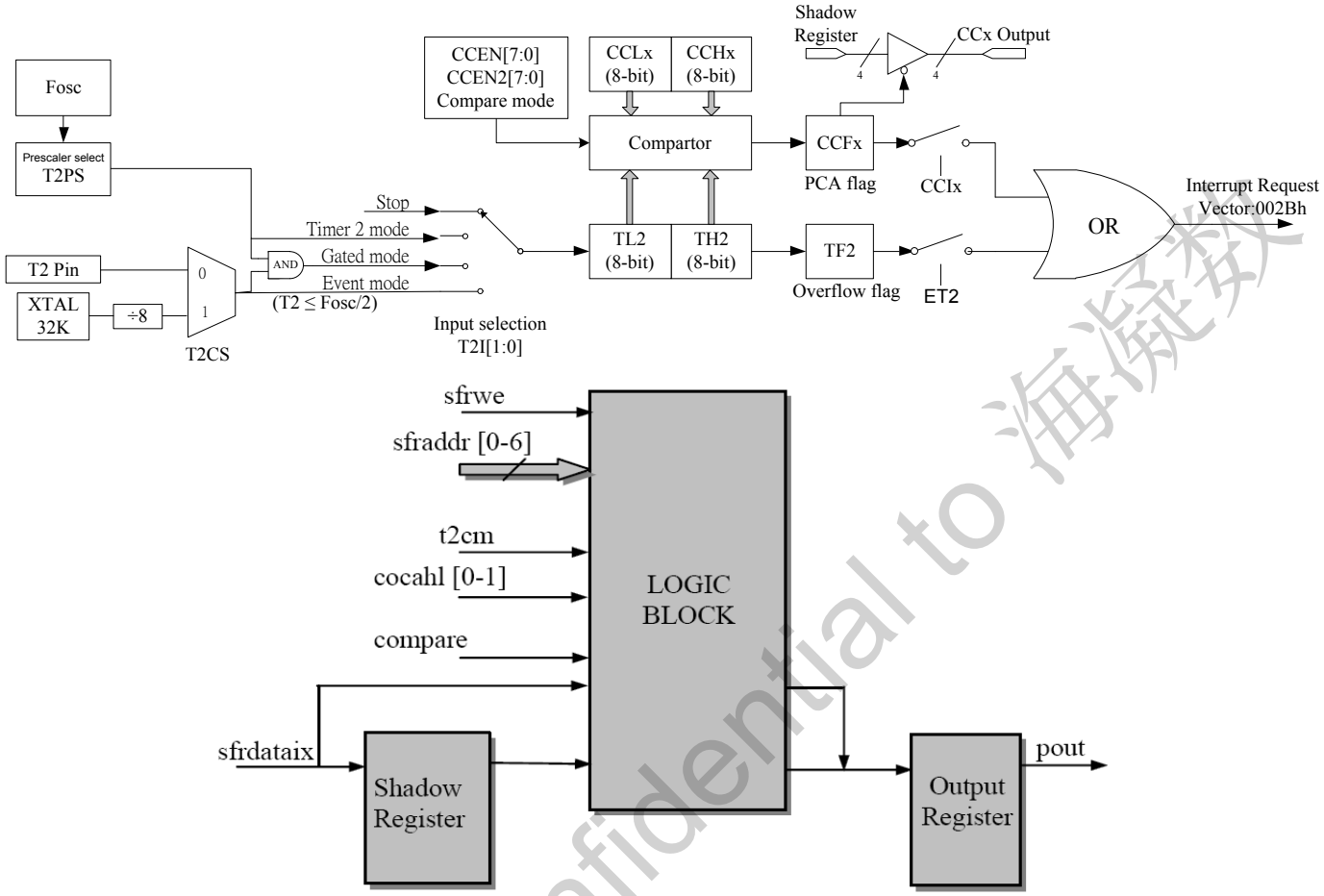

Fig. 7-5: Mode 1 Register/Port Function

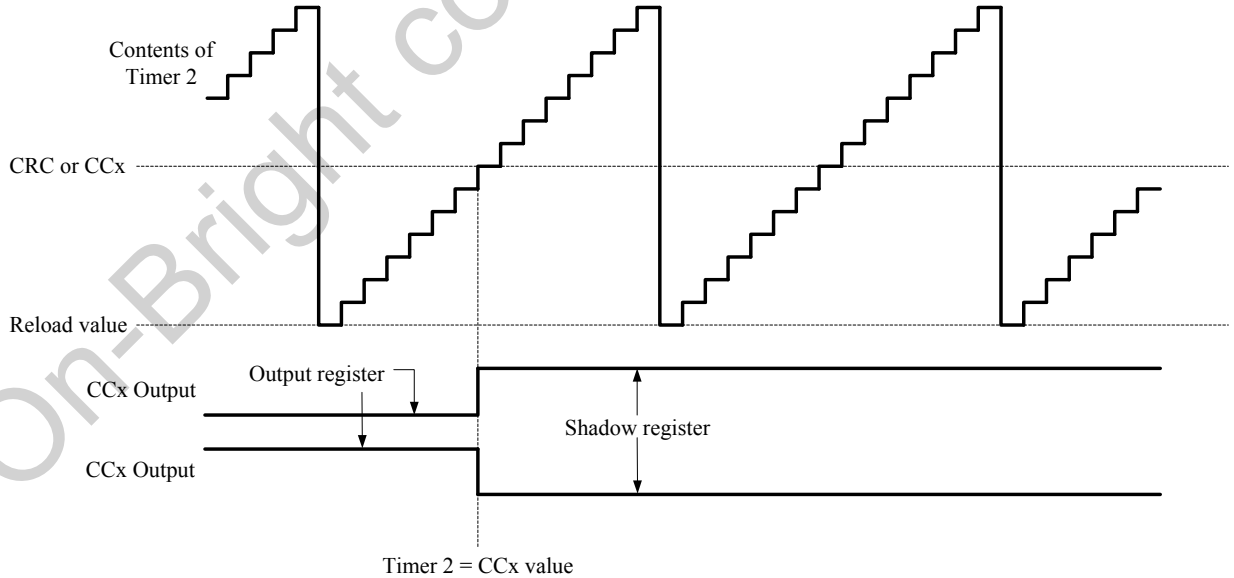

Fig. 7-6: Compare mode 1 function

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7.3 Capture function

Actual timer/counter contents can be saved into registers CCx or CRC upon an external event (mode 0) or a software write operation (mode 1).

7.3.1 Capture Mode 0 (by Hardware)

In mode 0, value capture of Timer 2 is executed when:

(1) Rising edge on input CC0-CC3
(2) Falling edge on input CC0-CC3
(3) Both rising and falling edge on input CC0-CC3

The contents of Timer 2 will be latched into the appropriate capture register. As shown in Fig. 7-7

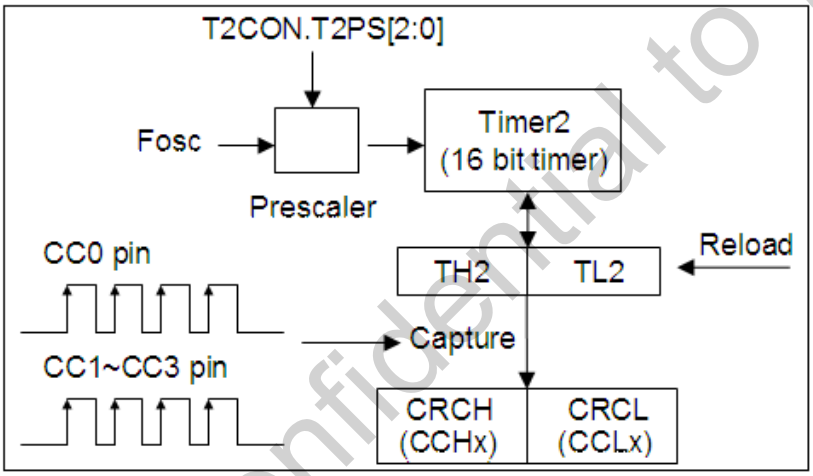

Fig. 7-7: Capture mode 0 function

7.3.2 Capture Mode 1(by Software)

In mode 1, value capture of timer 2 is caused by writing any value into the low-order byte of the dedicated capture register. The value written to the capture register is irrelevant to this function. The contents of Timer 2 will be latched into the appropriate capture register. As shown in Fig. 7-8

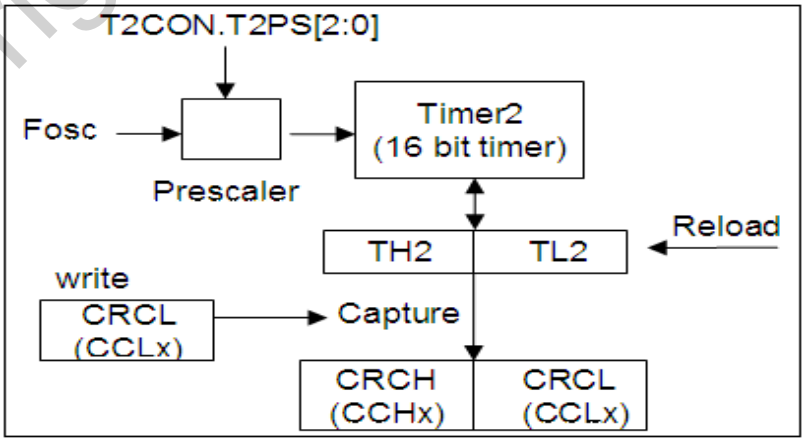

Fig. 7-8: Capture mode 1 function

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8. Serial interface

There are two serial interfaces for data communication in OB39R32T2, they are the so called UART0 and UART1.

As the conventional UART, the communication speed can be selected by configuring the baud rate in SFRs.
These two serial buffers consists of two separate registers, a transmit buffer and a receive buffer. Writing data to the SFR S0BUF or S1BUF sets this data in serial output buffer and starts the transmission. Reading from the S0BUF or S1BUF reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the second byte before the transmission of the first byte is completed.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Serial interface 0											
PCON	Power control	87h	SMOD	-	-	-	-	-	STOP	IDLE	00H
AUX	Auxiliary register	91h	BRGS	-	-	-	IIC1S	UR1S	UR0S	DPS	00H
S0CON	Serial port-0 control register	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
S0RELL	Serial port-0 reload register low byte	AAh	S0REL[7:0]								00H
S0RELH	Serial port-0 reload register high byte	BAh	-	-	-	-	-	-	S0REL[9:8]		00H
S0BUF	Serial port-0 data buffer	99h	S0BUF[7:0]								00H
Serial interface 1											
S1CON	Serial port-1 control register	DCh	S1M		S1M2	REN1	TB81	RB81	TI1	RI1	00H
S1RELL	Serial port-1 reload register low byte	DEh	S1REL[7:0]								00H
S1RELH	Serial port-1 reload register high byte	DFH	-	-	-	-	-	-	S1REL[9:8]		00H
S1BUF	Serial port-1 data buffer	DDh	S1BUF[7:0]								00H

8.1 Serial interface 0

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	-	IIC1S	UR1S	UR0S	DPS	00H

BRGS: Baud rate generator.

BRGS = 0 - baud rate generator from Timer 1.

BRGS = 1 - baud rate generator by S0REL.

UR0S: Serial port-0 Function Select:

UR0S = 0 –Serial port-0 function on P2 (P2.0&P2.1).

UR0S = 1 –Serial port-0 function on P0 (P0.0&P0.1).

UR1S: Serial port-1 Function Select:

UR1S = 0 –Serial port-1 function on P1 (P1.0&P1.1).

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UR1S = 1 –Serial port-1 function on P0 (P0.2&P0.3).

Mnemonic: S0CON **Address: 98h**

7	6	5	4	3	2	1	0	Reset
SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H

SM0, SM1: Serial Port 0 mode selection.

SM0	SM1	Mode
0	0	0
0	1	1
1	0	2
1	1	3

The 4 modes in UART, Mode 0 ~ 3, are explained later.

SM2: Enables multiprocessor communication feature

REN: If set, enables serial reception. Cleared by software to disable reception.

TB8: The 9th transmitted data bit in modes 2 and 3. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB8: In modes 2 and 3, it is the 9th data bit received. In mode 1, if SM2 is 0, RB8 is the stop bit. In mode 0, this bit is not used. Must be cleared by software.

TI: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

The Serial Interface 0 can operate in the following 4 modes:

SM0	SM1	Mode	Description	Board Rate
0	0	0	Shift register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Variable

Here Fosc is the crystal or oscillator frequency.

8.1.1 Mode 0

Pin RXD0 serves as input and output. TXD0 outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI = 0 and REN = 1. In other modes, a start bit when REN = 1 starts receiving serial data. As shown in Fig.8-1 and Fig.8-2.

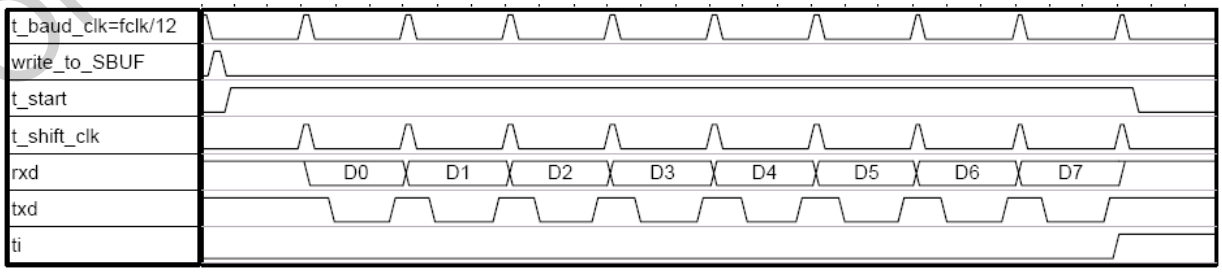

Fig. 8-1: Transmit mode 0

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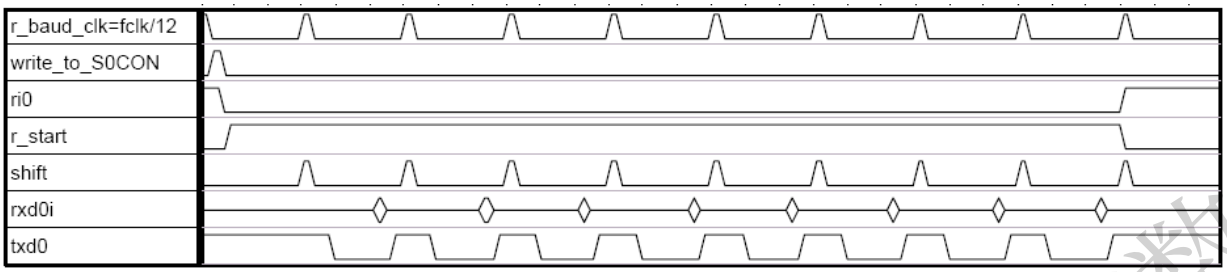

Fig. 8-2: Receive mode 0

8.1.2 Mode 1

Pin RXD0 serves as input, and TXD0 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading SBUF, and stop bit sets the flag RB8 in the Special Function Register S0CON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate. As shown in Fig. 8-3 and Fig. 8-4.

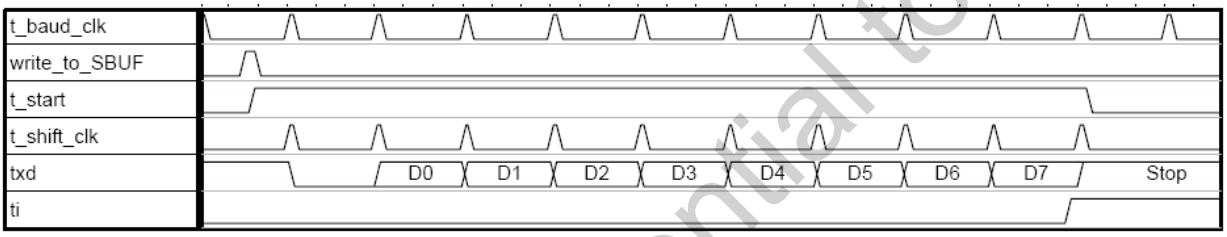

Fig. 8-3: Transmit mode 1

Fig. 8-4: Receive mode 1

8.1.3 Mode 2

This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 (SMOD=1) or 1/64(SMOD=0) of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB8 in S0CON is output as the 9th bit, and at receive, the 9th bit affects RB8 in Special Function Register S0CON.

8.1.4 Mode 3

The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be use to specify baud rate. As shown in Fig. 8-5 and Fig. 8-6.

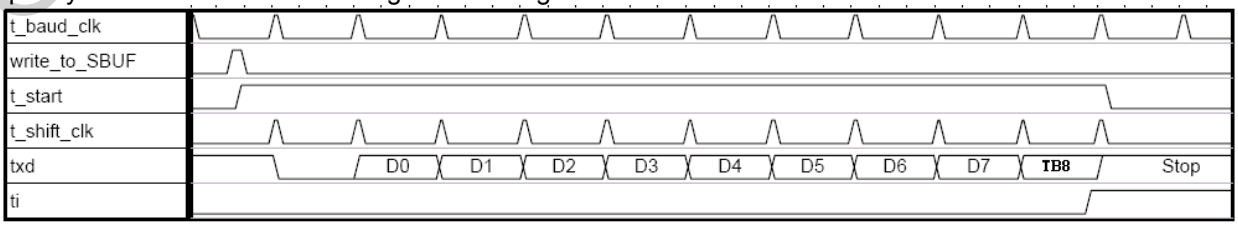

Fig. 8-5: Transmit modes 2 and 3

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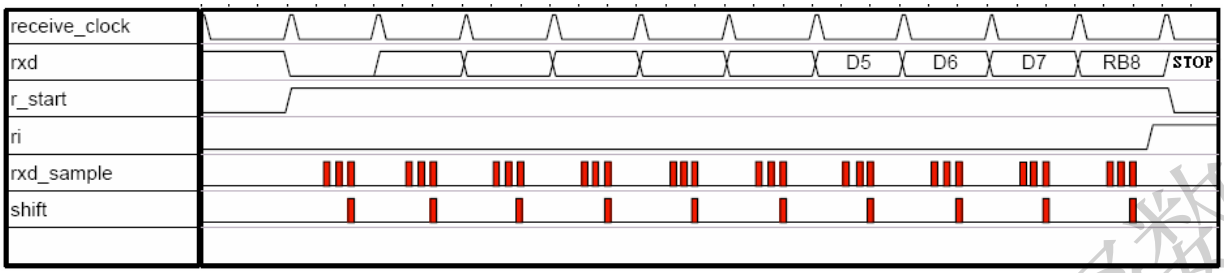

Fig. 8-6: Receive modes 2 and 3

8.1.5 Multiprocessor Communication of Serial Interface

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface can be used for multiprocessor communication. In this case, the slave processors have bit SM2 in S0CON set to 1. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear SM2 and receive the rest of the message, while other slaves will leave SM2 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

8.1.6 Peripheral Frequency control register

Mnemonic: PFCON **Address: D9h**

7	6	5	4	3	2	1	0	Reset
-	-	T3PS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

T1PS[1:0]: Timer1 Prescaler select

T1PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

8.1.7 Baud rate generator

Serial interface modes 1 and 3

8.1.7.1 When BRGS = 0 (in Special Function Register AUX).

(1) T1PS[1:0] is 00

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{osc}}{32 \times 12 \times (256 - TH1)}$$

(2) T1PS[1:0] is 01

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{osc}}{32 \times (256 - TH1)}$$

(3) T1PS[1:0] is 10

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$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{osc}}{32 \times 96 \times (256 - TH1)}$$

8.1.7.2 When BRGS = 1 (in Special Function Register AUX).

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{clk}}{64 \times (2^{10} - \text{S0REL})}$$

8.2 Serial interface 1

Mnemonic: S1CON **Address: DCh**

7	6	5	4	3	2	1	0	Reset
S1M	-	S1M2	REN1	TB81	RB81	TI1	RI1	00H

S1M: Serial Port 1 mode selection.

S1M	Mode
0	A
1	B

S1M2: Enables multiprocessor communication feature

REN1: If set, enables serial reception. Cleared by software to disable reception.

TB81: The 9th transmitted data bit in modes A. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB81: In modes A, it is the 9th data bit received. In mode B, if S1M2 is 0, RB81 is the stop bit. Must be cleared by software.

TI1: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI1: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

The Serial Interface 1 can operate in the following 2 modes:

S1M	Mode	Description	Board Rate
0	A	9-bit UART	Variable
1	B	8-bit UART	Variable

8.2.1 Mode A

This mode is similar to Mode 2 and 3 of Serial interface 0, 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB81 in S1CON is outputted as the 9th bit, and at receive, the 9th bit affects RB81 in Special Function Register S1CON.

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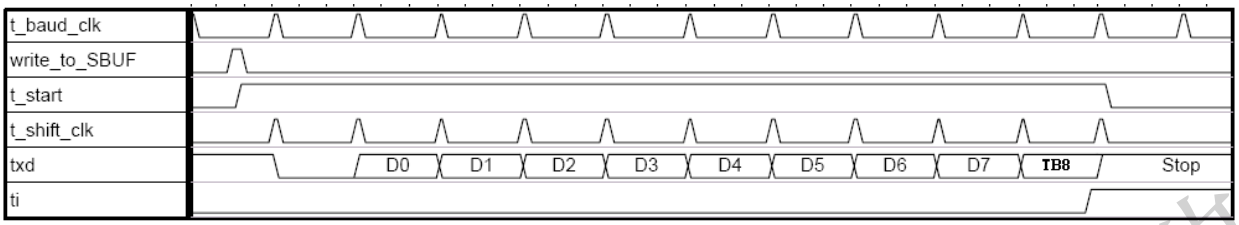

Fig. 8-7: Transmit mode A

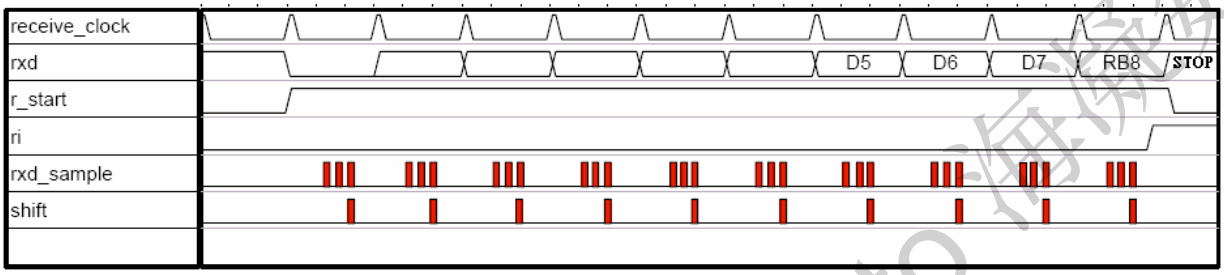

Fig. 8-8: Receive mode A

8.2.2 Mode B

This mode is similar to Mode 1 of Serial interface 0. Pin RXD1 serves as input, and TXD1 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S1BUF, and stop bit sets the flag RB81 in the Special Function Register S1CON. In mode B internal baud rate generator is use to specify the baud rate.

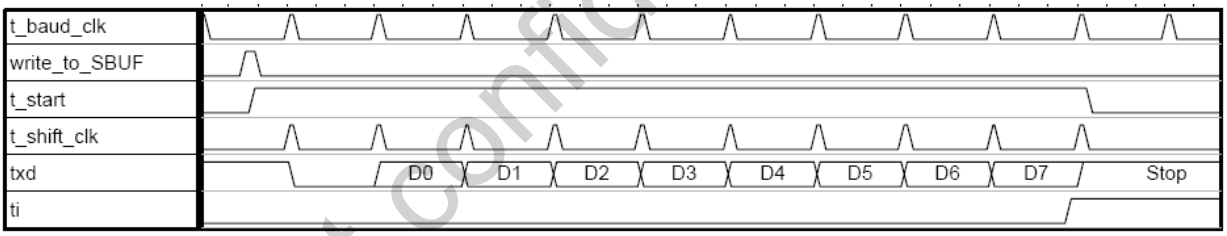

Fig. 9-9: Transmit mode B

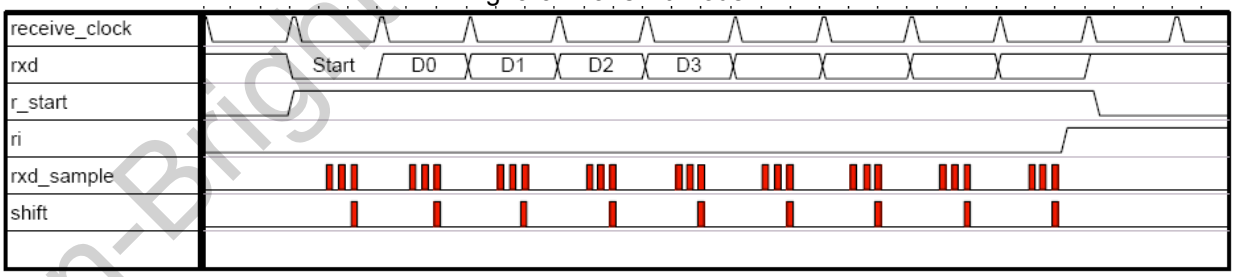

Fig. 8-10: Receive mode B

8.2.3 Multiprocessor Communication of Serial Interface

The feature of receiving 9 bits in Mode A of Serial Interface can be used for multiprocessor communication. In this case, the slave processors have bit S1M2 in S1CON set to 1. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear S1M2 and receive the rest of the message, while other slaves will leave S1M2 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

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8.2.4 Baud rate generator

Serial interface modes A and B

$$\text{Baud Rate} = \frac{F_{clk}}{32 \times \left(2^{10} - \text{S1REL}\right)}$$

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9. Watchdog timer

The Watch Dog Timer (WDT) is an 8-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1, Timer2 and Timer3 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDTRF bit of RSTS register whenever un-predicted reset happened. After an external reset the watchdog timer is disabled and all registers are set to zeros.

The clock of WDT is from 26KHz IRC. The WDT will keep on running even after the system clock has been turned off (for example, in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the MCU to reset. The WDT can be enabled or disabled any time during the normal mode. Please refer the WDTRE bit of WDTRC register. The default WDT time-out period is approximately 157.54ms (WDTRM [3:0] = 0100b).

The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit3 ~ bit0 (WDTRM [3:0]) of Watch Dog Timer Control Register (WDTRC) should be set accordingly. As shown in Table 9-1.

$$WDTRCLK = \frac{\mathrm{26KHz}}{2^{\mathrm{WDTRM}}} \qquad Watchdog\ reset\ time = \frac{256}{\mathrm{WDTRCLK}}$$

$$WDTICLK = \frac{\mathrm{26KHz}}{2^{\mathrm{WDTIM}}} \qquad Watchdog\ Interrupt\ time = \frac{256}{\mathrm{WDTICLK}}$$

Table 9-1: WDT time-out period

WDTRM [3:0]	Divider (26 KHz RC oscillator in)	Reset Time period @ 26KHz	WDTIM [3:0]	Divider (26 KHz RC oscillator in)	Interrupt Time period @ 26KHz
0000	1	9.85ms	0000	8	9.85ms
0001	2	19.69ms	0001	16	19.69ms
0010	4	39.38ms	0010	24	39.38ms
0011	8	78.77ms	0011	32	78.77ms
0100	16	157.54ms(default)	0100	40	157.54ms
0101	32	315.08ms	0101	48	315.08ms
0110	64	630.15ms	0110	56	630.15ms
0111	128	1.26s	0111	64	1.26s
1000	256	2.52s	1000	72	2.52s
1001	512	5.04s	1001	80	5.04s
1010	1024	10.08s	1010	88	10.08s
1011	2048	20.16s	1011	96	20.16s
1100	4096	40.33s	1100	104	40.33s
1101	8192	80.66s	1101	112	80.66s
1110	16384	161.3s	1110	120	161.3s
1111	32768	322.64s	1111	128	322.64s

The program can enable the WDT function by programming 1 to the WDTRE bit. After WDTRE set to 1, the 8 bit-counter starts to count with the selected time base source clock which set by WDTRM [3:0]. It will generate a reset signal when overflows. The WDTRE bit will be cleared to 0 automatically when MCU been reset, either hardware reset or WDT reset. As shown in Fig. 9-1.

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Once the watchdog is started it cannot be stopped. User can refreshed the watchdog timer to zero by writing 0x55 to Watch Dog Timer refresh Key (WDTK) register. This will clear the content of the 8-bit counter and let the counter re-start to count from the beginning. The watchdog timer must be refreshed regularly to prevent reset request signal from becoming active.

When Watchdog timer is overflow, the WDTRF flag will set to one and automatically reset MCU. The WDTRF flag can be clear by software or external reset or power on reset.

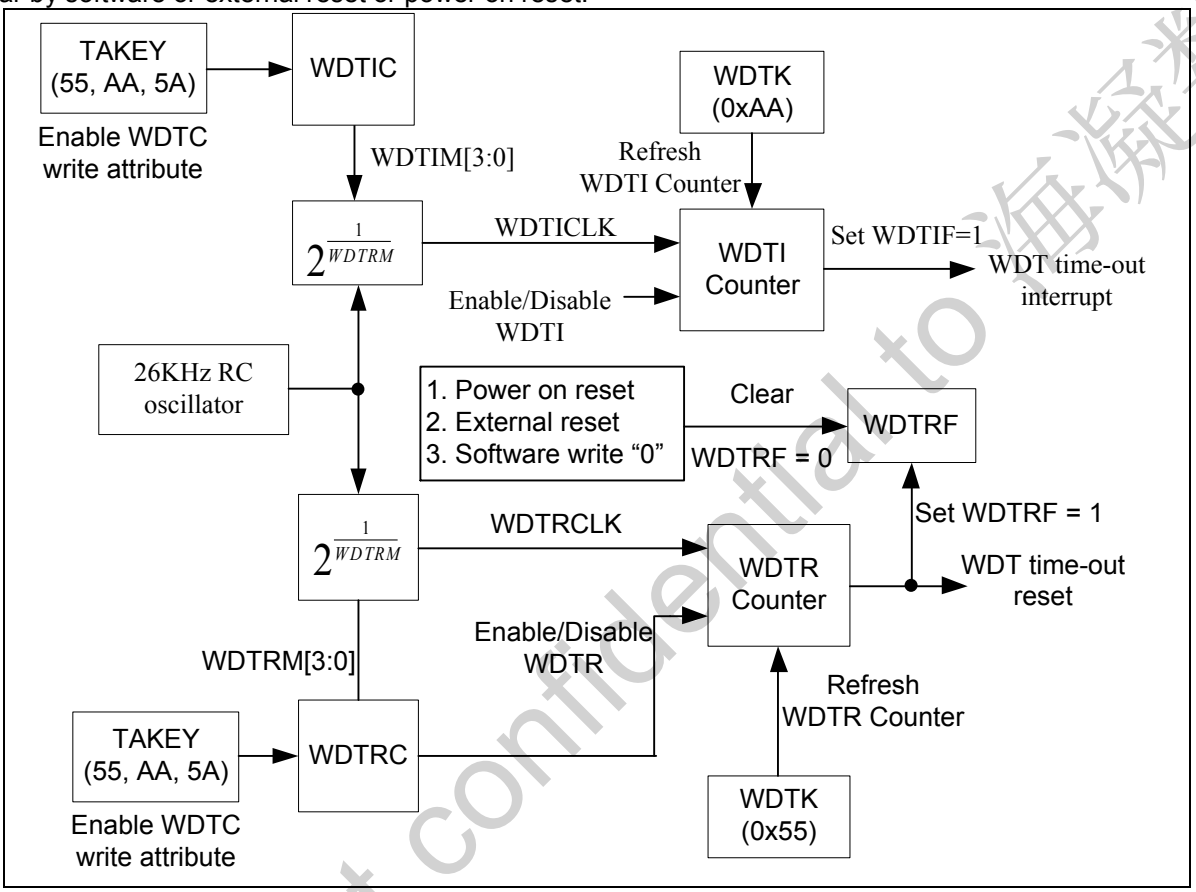

Fig. 9-1: Watchdog timer block diagram

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Watchdog Timer											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
WDTRC	Watchdog timer reset control register	B6h	-	-	WDTRE	-	WDTRM[3:0]				04H
WDTIC	Watchdog timer interrupt control register	FFh	-	-	WDTIE	WDTIOF	WDTIM[3:0]				00H
WDTK	Watchdog timer refresh key	B7h	WDTK[7:0]								00H
RSTS	Reset status register	A1h	-	-	-	-	WDTRF	SWRF	LVRF	PORF	00H

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Mnemonic: TAKEY **Address: F7h**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Watchdog timer control register (WDTRC & WDTIC)is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the WDTRC write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

Mnemonic: WDTRC **Address: B6h**

7	6	5	4	3	2	1	0	Reset
-	-	WDTRE	-	WDTRM [3:0]				04H

WDTRE: Control bit used to enable Watchdog reset timer.

WDTRE = 0 - Disable Watchdog reset timer.

WDTRE = 1 - Enable Watchdog reset timer.

WDTRM [3:0]: WDT clock source divider bit. As seen in Fig. 9-1 to reference the WDT time-out period.

Mnemonic: WDTIC **Address: FFh**

7	6	5	4	3	2	1	0	Reset
-	-	WDTIE	WDTIOF	WDTIM [3:0]				00H

WDTIE: Control bit used to enable Watchdog interrupt timer.

WDTIE = 0 - Disable Watchdog interrupt timer.

WDTIE = 1 - Enable Watchdog interrupt timer.

The function is support interrupt and stop mode wakeup.

WDTIOF: Watchdog Interrupt Timer overflow flag set by hardware when WatchdogInterrupt Timer overflows. This flag can be cleared by software

WDTIM [3:0]: WDT clock source divider bit. As seen in Fig. 9-1 to reference the WDT time-out period.

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	WDTRF	SWRF	LVRF	PORF	00h

WDTRF: Watchdog timer reset flag. When MCU is reset by watchdog, WDTRF flag will be set to one by hardware. This flag clear by software

Mnemonic: WDTK **Address: B7h**

7	6	5	4	3	2	1	0	Reset
WDTK[7:0]								00h

WDTK: Watchdog timer refresh key.

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A programmer must write 0x55 or 0xAA into WDTK register, and then the watchdog reset timer or interrupt timer will be cleared to zero.

For example 1, if enable WDT reset period is 2.52s

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah    ; enable WDTRC write attribute.
MOV WDTRC, #28h    ; Set WDTRM [3:0] = 1000b. Set WDTRE =1 to enable WDT function.
.
.
.
MOV WDTK, #55h     ; Clear WDT reset timer to 0.
```

For example 2, if enable WDT interrupt period is 39.38ms.

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah    ; enable WDTIC write attribute.
MOV WDTIC, #24h    ;Set WDTIM [3:0] = 0100b. ;Set WDTIE =1 to enable WDT function
```

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10. Software RTC

Using low-speed external crystal 32.768KHz. It can operate during stop mode or idle mode. It can be reached when the set time to wake up.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Software RTC											
IEN2	Interrupt Enable 2 register	9AH	-	-	-	IESRTC	IETK	EX3	EWDT	ES1	00H
IRCON2	Interrupt request register 2	97H	-	-		SRTCIF-	TKIF	-	WDTI IF	-	00H
SRTCCON	Software RTC Control	0xF5	SRTCRZ	LXTRF	LXTNF	SRTCE	SRTCOF	-	SRTCP[1:0]		00H

Mnemonic: SRTCCON **Address: h**

7	6	5	4	3	2	1	0	Reset
SRTCRZ	LXTRF	LXTNF	SRTCE	SRTCOF		SRTCP[1:0]		00h

SRTCRZ: Software RTC timer return-to-zero bit
1: Reset RTC timer.
0: Cleared by hardware
※ Software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the SRTCRZ write attribute. That is:
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY , #5Ah

LXTRF: Low speed crystal ready flag (Read only)
0: Not ready
1: Ready
※ The flag indicates when the low speed oscillator is stable after POR or a wake-up has occurred (power-down mode)
※ The flag can only change to a high level if the LXT were used

LXTNF: Low speed crystal oscillator noise filter
0: Disable
1: Enable (20ns)

SRTCE: Control bit used to enable software RTC.
0: Disable software RTC.
1: Enable software RTC.

SRTCOF: SRTC Timer overflow flag set by hardware when SRTC Timer overflows. This flag can be cleared by software

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SRTCP[1:0]: Software RTC timer-out period

SRTCP[1:0]	Period
00	0.5s
01	1s
10	2s
11	4s

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11. Interrupt

The OB39R32T2 provides 18 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register. Each interrupt requested by the corresponding flag could individually be enabled or disabled by the enable bits in SFR's IEN0, IEN1, IEN2.

When the interrupt occurs, the engine will vector to the predetermined address as given in Table 10-1. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction RETI. When an RETI is performed, the processor will return to the instruction that would have been next when interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, and then samples are polled by hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then interrupt request flag is set. On the next instruction cycle the interrupt will be acknowledged by hardware forcing an LCALL to appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of microcontroller when the interrupt occurs. If microcontroller is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles for perform the LCALL.

Table 10-1: Interrupt vectors

	Interrupt Request Flags	Interrupt Vector Address	Keil C Interrupt Number
1	IE0 – External interrupt 0	0003h	0
2	TF0 – Timer 0 interrupt	000Bh	1
3	IE1 – External interrupt 1	0013h	2
4	TF1 – Timer 1 interrupt	001Bh	3
5	RI0/TI 0– Serial channel 0 interrupt	0023h	4
6	TF2/EXF2 – Timer 2 interrupt	002Bh	5
7	IE2 – External interrupt 2	0033h	6
8	IE3 – External interrupt 3	003Bh	7
9	PWMIF – PWM interrupt	0043h	8
10	IICIF1 – IIC1 interrupt	004Bh	9
11	ADCIF – A/D converter interrupt	0053h	10
12	KBIIF –keyboard Interface interrupt	005Bh	11
13	LVIIF – Low Voltage Interrupt	0063h	12
14	IICIF0 – IIC0 interrupt	006Bh	13
15	TF3 – Timer 3 interrupt	0073h	14
16	RI1/TI1 – Serial channel 1 interrupt	0083h	16
17	WDTIF & SRTCIF – Watchdog interrupt & Software RTC interrupt	008Bh	17
18	TKIF – Touch interrupt	009Bh	19

*See Keil C about C51 User's Guide about Interrupt Function description

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Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Interrupt											
IEN0	Interrupt Enable 0 register	A8H	EA	ET3	ET2	ES0	ET1	EX1	ET0	EX0	00H
IEN1	Interrupt Enable 1 register	B8H	EXEN2	EX2	IEIIC0	IELVI	IEKBI	IEADC	IEIIC1	IEPWM	00H
IEN2	Interrupt Enable 2 register	9AH	-	-	-	IESRTC	IETK	EX3	EWDT	ES1	00H
IRCON	Interrupt request register	C0H	EXF2	TF2	IICIF0	LVIIF	KBIIF	ADCIF	IICIF1	PWMIF	00H
IRCON2	Interrupt request register 2	97H	-	-	-	SRTCIF	TKIF	-	WDTIF	-	00H
IP0	Interrupt priority level 0	A9H	-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00H
IP1	Interrupt priority level 1	B9H	-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00H

Mnemonic: IEN0 **Address: A8h**

7	6	5	4	3	2	1	0	Reset
EA	ET3	ET2	ES	ET1	EX1	ET0	EX0	00h

EA: EA=0 – Disable all interrupt.
EA=1 – Enable all interrupt.

ET3: ET3 = 0 – Disable Timer 3 overflow or external reload interrupt.
ET3 = 1 – Enable Timer 3 overflow or external reload interrupt.

ET2: ET2=0 – Disable Timer 2 overflow or external reload interrupt.
ET2=1 – Enable Timer 2 overflow or external reload interrupt.

ES0: ES0=0 – Disable Serial channel 0 interrupt.
ES0=1 – Enable Serial channel 0 interrupt.

ET1: ET1=0 – Disable Timer 1 overflow interrupt.
ET1=1 – Enable Timer 1 overflow interrupt.

EX1: EX1=0 – Disable external interrupt 1.
EX1=1 – Enable external interrupt 1.

ET0: ET0=0 – Disable Timer 0 overflow interrupt.
ET0=1 – Enable Timer 0 overflow interrupt.

EX0: EX0=0 – Disable external interrupt 0.
EX0=1 – Enable external interrupt 0.

Mnemonic: IEN1 **Address: B8h**

7	6	5	4	3	2	1	0	Reset
EXEN2	EX2	IEIIC0	IELVI	IEKBI	IEADC	IEIIC1	IEPWM	00H

EXEN2: Timer 2 reload interrupt enable.
EXEN2 = 0 – Disable Timer 2 external reload interrupt.
EXEN2 = 1 – Enable Timer 2 external reload interrupt.

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EX2: EX2 = 0 – Disable external interrupt 2.

EX2 = 1 – Enable external interrupt 2.

IEIIC0: IIC0 interrupt enable.

IEIIC0 = 0 – Disable IIC0 interrupt.

IEIIC0 = 1 – Enable IIC0 interrupt.

IELVI: LVI interrupt enable.

IELVI = 0 – Disable LVI interrupt.

IELVI = 1 – Enable LVI interrupt.

IEKBI: KBI interrupt enable

IEKBI = 0 – Disable KBI interrupt.

IEKBI = 1 – Enable KBI interrupt.

IEADC: A/D converter interrupt enable

IEADC = 0 – Disable ADC interrupt.

IEADC = 1 – Enable ADC interrupt.

IEIIC1: IIC1 interrupt enable.

IEIIC1 = 0 – Disable IIC1 interrupt.

IEIIC1 = 1 – Enable IIC1 interrupt.

IEPWM: PWM interrupt enable.

IEPWM = 0 – Disable PWM interrupt.

IEPWM = 1 – Enable PWM interrupt.

Mnemonic: IEN2 **Address: 9Ah**

7	6	5	4	3	2	1	0	Reset
-	-	-	IESRTC	IETK	EX3	EWDT	ES1	00H

IESRTC: IESRTC = 0 – Disable Software RTC interrupt.

IESRTC = 1 – Enable Software RTC interrupt.

IETK: IETK = 0 – Disable Touch Key interrupt.

IETK = 1 – Enable Touch Key interrupt.

EX3: EX3 = 0 – Disable external interrupt 3.

EX3 = 1 – Enable external interrupt 3.

EWDT: Enable Watch dog interrupt.

EWDT = 0 – Disable Watch dog interrupt.

EWDT = 1 – Enable Watch dog interrupt.

ES1: Enable Serial 1 interrupt.

ES1 = 0 – Disable Serial 1 interrupt.

ES1 = 1 – Enable Serial 1 interrupt.

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Mnemonic: IRCON **Address: C0h**

7	6	5	4	3	2	1	0	Reset
EXF2	TF2	IICIF	LVIIF	KBIIF	ADCIF	IICIF1	PWMIF	00H

EXF2: Timer 2 external reload flag. Must be cleared by software.

TF2: Timer 2 overflow flag. Must be cleared by software.

IICIF0: IIC0 interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

LVIIF: LVI interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

KBIIF KBI interrut flag. Must be cleared by software.

ADCIF: A/D converter end interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

IICIF1: IIC1 interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

PWMIF: PWM interrut flag. Hardware will clear this flag automatically when enter interrupt vector.

Mnemonic:IRCON2 **Address: 97h**

7	6	5	4	3	2	1	0	Reset
-	-	-	SRTCIF	TKIF	-	WDTIF	-	00H

SRTCIF: Software RTC interrupt flag. Must be cleared by software.

TKIF: Touch Key interrupt flag. Must be cleared by software.

WDTIF: Watch dog interrupt flag. Must be cleared by software.

11.1 Priority level structure

All interrupt sources are combined in groups.

Table 10-2: Priority level groups

Groups		
External interrupt 0	Serial channel 1 interrupt	PWM interrupt
Timer 0 interrupt	Watchdog interrupt & Software RTC interrupt	IIC1 interrupt
External interrupt 1	Timer 3 interrupt	ADC interrupt
Timer 1 interrupt	External interrupt 2	KBI interrupt
Serial channel 0 interrupt	External interrupt 3	LVI interrupt
Touch interrupt	Timer 2 interrupt	IIC0 interrupt

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level will be received simultaneously, an internal polling sequence determines which request is serviced first.

Mnemonic: IP0 **Address: A9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00h

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Mnemonic: IP1 **Address: B9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00h

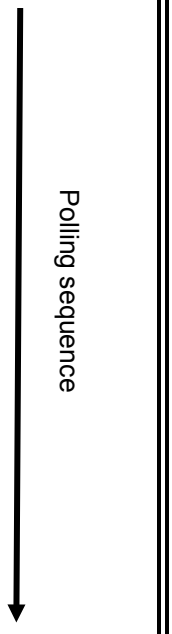
Table 10-3: Priority levels

IP1.x	IP0.x	Priority Level
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

Table 10-4: Groups of priority

Bit	Group		
IP1.0, IP0.0	External interrupt 0	Serial channel 1 interrupt	PWM interrupt
IP1.1, IP0.1	Timer 0 interrupt	Watchdog interrupt & Software RTC interrupt	IIC1 interrupt
IP1.2, IP0.2	External interrupt 1	Timer 3 interrupt	ADC interrupt
IP1.3, IP0.3	Timer 1 interrupt	External interrupt 2	KBI interrupt
IP1.4, IP0.4	Serial channel 0 interrupt	External interrupt 3	LVI interrupt
IP1.5, IP0.5	Touch interrupt	Timer 2 interrupt	IIC0 interrupt

Table 10-5: Polling sequence

Interrupt source	Sequence
External interrupt 0	
Serial channel 1 interrupt	
PWM interrupt	
Timer 0 interrupt	
Watchdog interrupt & Software RTC interrupt	
IIC1 interrupt	
External interrupt 1	
Timer3 interrupt	
ADC interrupt	
Timer 1 interrupt	
External interrupt 2	
KBI interrupt	
Serial channel 0 interrupt	
External interrupt 3	
LVI interrupt	
Touch Key interrupt	
Timer 2 interrupt	
IIC0 interrupt	

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12. Power Management Unit

Power management unit serves two power management modes, IDLE and STOP, for the users to do power saving function.

Mnemonic: PCON **Address: 87h**

7	6	5	4	3	2	1	0	Reset
SMOD	-	-	-	-	-	STOP	IDLE	00h

STOP: Stop mode control bit. Setting this bit turning on the Stop Mode.
Stop bit is always read as 0

IDLE: Idle mode control bit. Setting this bit turning on the Idle Mode.
Idle bit is always read as 0

12.1 Idle mode

Setting the IDLE bit of PCON register invokes the IDLE mode. The IDLE mode leaves internal clocks and peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any interrupts or a reset.

12.2 Stop mode

Setting the STOP bit of PCON register invokes the STOP mode. All internal clocking in this mode is turn off. The CPU will exit this state from a no-clocked interrupt (external INT0/1/2/3, LVI, KBI and Watchdog interrupt) or a reset (WDTR and LVR) condition. Internally generated interrupts (timer, serial port ...) have no effect on stop mode since they require clocking activity.

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13. IIC function

The IIC module uses the SCL (clock) and the SDA (data) line to communicate with external IIC interface. Its speed can be selected to 400Kbps (maximum) by software setting the IICBR [2:0] control bit. The IIC module provided 2 interrupts (RXIF, TXIF). It will generate START, repeated START and STOP signals automatically in master mode and can detects START, repeated START and STOP signals in slave mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

The interrupt vector is 6Bh.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
IIC0 function											
IIC0CTL	IIC0 control register	F9h	IIC0EN	MSS0	MAS0	AB0_EN	BF0_EN	IIC0BR[2:0]			04H
IIC0S	IIC0 status register	F8h	-	MPIF0	LAIF0	RXIF0	TXIF0	RXAK0	TXAK0	RW or BB	00H
IIC0A1	IIC0 Address 1 register	FAh	IIC0A1[7:1]							MATCH 1or RW1	A0H
IIC0A2	IIC0 Address 2 register	FBh	IIC0A2[7:1]							MATCH 2 or RW2	60H
IIC0RWD	IIC0 Read/ Write register	FCh	IIC0RWD[7:0]								00H
IIC0EBT	IIC0 Enaable Bus Transaction	FDh	FU0_EN		-	-	-	-	-	-	00H
IIC1 function											
AUX	Auxiliary register	91h	BRGS	-	-	-	IIC1S	UR1S	UR0S	DPS	00H
IIC1CTL	IIC1 control register	E9h	IIC1EN	MSS1	MAS1	AB1_EN	BF1_EN	IIC1BR[2:0]			04H
IIC1S	IIC1 status register	E8h	-	MPIF1	LAIF1	RXIF1	TXIF1	RXAK1	TXAK1	RW or BB	00H
IIC1A1	IIC1 Address 1 register	EAh	IIC1A1[7:1]							MATCH 1or RW1	A0H
IIC1A2	IIC1 Address 2 register	EBh	IIC1A2[7:1]							MATCH 2 or RW2	60H
IIC1RWD	IIC1 Read/ Write register	ECh	IIC1RWD[7:0]								00H
IIC1EBT	IIC1 Enaable Bus Transaction	EDh	FU1_EN		-	-				-	00H

13.1 IIC interface 0

Mnemonic: IIC0CTL **Address: F9h**

7	6	5	4	3	2	1	0	Reset
IIC0EN	MSS0	MAS0	AB0_EN	BF0_EN	IIC0BR[2:0]			04h

IIC0EN: Enable IIC0 module

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IIC0EN = 1 is Enable

IIC0EN = 0 is Disable.

MSS0: Master or slave mode select.

MSS0 = 1 is master mode.

MSS0 = 0 is slave mode.

*The software must set this bit before setting others register.

MAS0: Master address select (master mode only)

MAS0 = 0 is to use IIC0A1.

MAS0 = 1 is to use IIC0A2.

AB0_EN: Arbitration lost enable bit. (Master mode only)

If set AB0_EN bit, the hardware will check arbitration lost. Once arbitration lost occurred, hardware will return to IDLE state. If this bit is cleared, hardware will not care arbitration lost condition. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

BF0_EN: Bus busy enable bit. (Master mode only)

If set BF0_EN bit, hardware will not generate a start condition to bus until BF=0. Clear this bit will always generate a start condition to bus when FU0_EN[7:6] is set to 10. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

IIC0BR[2:0]: Baud rate selection (master mode only), where Fosc is the external crystal or oscillator frequency. The default is Fosc/(512+5) for users' convenience.

IIC0BR[2:0]	Baud rate
000	Fosc/(32+5)
001	Fosc/64+5)
010	Fosc/(128+5)
011	Fosc/(256+5)
100	Fosc/(512+5)
101	Fosc/(1024+5)
110	Fosc/(2048+5)
111	Fosc/(4096+5)

Mnemonic: IIC0S **Address: F8H**

7	6	5	4	3	2	1	0	Reset
-	MPIF0	LAIF0	RXIF0	TXIF0	RXAK0	TXAK0	RW or BB	00H

MPIF0: The Stop condition Interrupt Flag

The stop condition occurred and this bit will be set. Software need to clear this bit

LAIF0: Arbitration lost bit. (Master mode only)

The Arbitration Interrupt Flag, the bus arbitration lost occurred and this bit will be set. Software need to clear this bit

RXIF0: The data Receive Interrupt Flag (RXIF0) is set after the IIC0RWD (IIC0 Read Write Data Buffer) is loaded with a newly receive data.

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TXIF0: The data Transmit Interrupt Flag (TXIF0) is set when the data of the IIC0RWD (IIC0 Read Write Data Buffer) is downloaded to the shift register.

RXAK0: The Acknowledge Status indicate bit. When clear, it means an acknowledge signal has been received after the complete 8 bits data Transmit on the bus.

TXAK0: The Acknowledge status Transmit bit. When received complete 8 bits data, this bit will set (NoAck) or clear (Ack) and Transmit to master to indicate the receive status.

RW or BB: Master Mode:

BB : Bus busy bit
If detect SCL=0 or SDA=0 or bus start, this bit will be set. If detect stop,this bit will be cleared. This bit can be cleared by software to return ready state.

Slave Mode:
RW:The slave mode read (received) or wrote (Transmit) on the IIC bus. When this bit is clear, the slave module received data on the IIC bus (SDA).(Slave mode only).
As shown in Fig. 12-1.

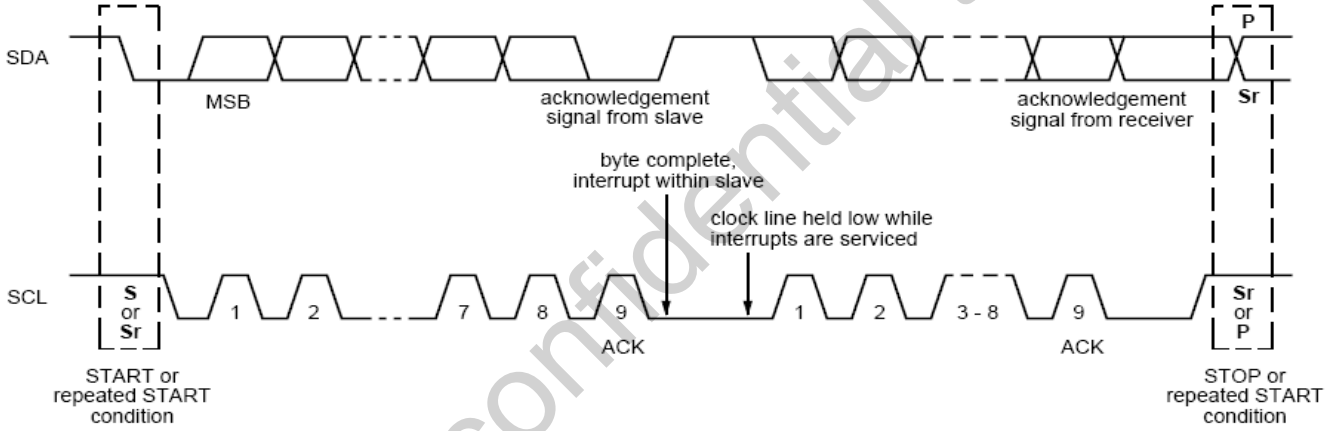

Fig. 12-1: Acknowledgement bit in the 9th bit of a byte transmission

Mnemonic: IIC0A1 **Address: FAH**

7	6	5	4	3	2	1	0	Reset
IIC0A1[7:1]							Match1 or RW1	A0H
R/W							R or R/W	

Slave mode:

IIC0A1[7:1]: IIC0 Address registers

This is the first 7-bit address for this slave module. It will be checked when an address (from master) is received

Match1: When IIC0A1 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.

Master mode:

IIC0A1[7:1]: IIC0 Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW1: This bit will be sent out as RW of the slave side if the module has set the FU0_EN[7:6] = 10. It appears at the 8th bit after the IIC address as below figure. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the

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module is in master Transmit mode. As shown in Fig. 12-2.

RW1=1, master receive mode

RW1=0, master Transmit mode

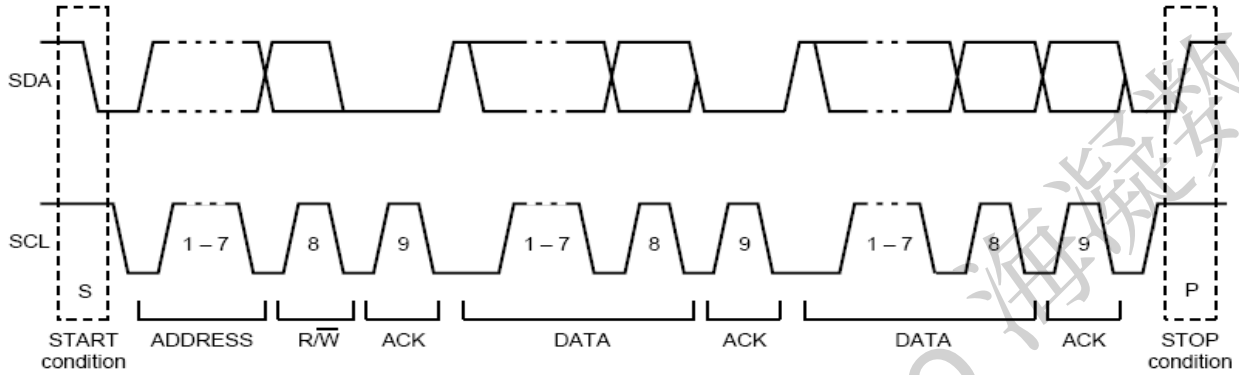

Fig. 12-2: RW bit in the 8th bit after IIC address

Mnemonic: IIC0A2 **Address: FBH**

7	6	5	4	3	2	1	0	Reset
IIC0A2[7:1]							Match2 or RW2	60H
R/W							R or R/W	

Slave mode:

IIC0A2[7:1]: IIC0 Address registers

This is the second 7-bit address for this slave module.

It will be checked when an address (from master) is received

Match2: When IIC0A2 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.

Master mode:

IIC0A2[7:1]: IIC0 Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW2: This bit will be sent out as RW of the slave side if the module has set the FU0_EN[7:6] = 10. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master Transmit mode.

RW2=1, master receive mode

RW2=0, master Transmit mode

Mnemonic: IIC0RWD **Address: FCh**

7	6	5	4	3	2	1	0	Reset
IIC0RWD[7:0]								00h

IIC0RWD[7:0]: IIC0 read write data buffer.

In receiving (read) mode, the received byte is stored here.

In Transmitting mode, the byte to be shifted out through SDA stays here.

Mnemonic: IIC0EBT **Address: FDH**

7	6	5	4	3	2	1	0	Reset

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FU0_EN	-	-	-	-	-	-	00H

Master Mode：

00: reserved

01: IIC bus module will enable read/write data transfer on SDA and SCL.

10: IIC bus module generate a start condition on the SDA/SCL, then send out address which is stored in the IIC0A1/IIC0A2(selected by MAS control bit)

11: IIC bus module generates a stop condition on the SDA/SCL.

FU0_EN[7:6] will be auto-clear by hardware, so setting FU0_EN[7:6] repeatedly is necessary.

Slave mode:

01: FU0_EN[7:6] should be set as 01 only. The other value is inhibited.

Notice:

FU0_EN[7:6] should be set as 01 before read/write data transfer for bus release; otherwise, SCL will be locked(pull low).

FU0_EN[7:6] should be set as 01 after read/write data transfer for receiving a stop condition from bus master.

In Transmit data mode(slave mode), the output data should be filled into IIC0RWD before setting FU0_EN[7:6] as 01.

FU0_EN[7:6] will be auto-clear by hardware, so setting FU0_EN[7:6] repeatedly is necessary.

13.2 IIC interface 1

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	-	IIC1S	UR1S	UR0S	DPS	00H

IIC1S: IIC1 Function Select:

UR1S = 0 – IIC1 function on P1 (P1.4&P1.5).

UR1S = 1 – IIC1 function on P3 (P3.5&P3.6).

Mnemonic: IIC1CTL **Address: E9h**

7	6	5	4	3	2	1	0	Reset
IIC1EN	MSS1	MAS1	AB1_EN	BF1_EN	IIC1BR[2:0]			04h

IIC1EN: Enable IIC1 module

IIC1EN = 1 is Enable

IIC1EN = 0 is Disable.

MSS1: Master or slave mode select.

MSS1 = 1 is master mode.

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MSS1 = 0 is slave mode.

*The software must set this bit before setting others register.

MAS1: Master address select (master mode only)

MAS1 = 0 is to use IIC1A1.

MAS1 = 1 is to use IIC1A2.

AB1_EN: Arbitration lost enable bit. (Master mode only)

If set AB1_EN bit, the hardware will check arbitration lost. Once arbitration lost occurred, hardware will return to IDLE state. If this bit is cleared, hardware will not care arbitration lost condition. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

BF1_EN: Bus busy enable bit. (Master mode only)

If set BF1_EN bit, hardware will not generate a start condition to bus until BF=0. Clear this bit will always generate a start condition to bus when FU1_EN[7:6] is set to 10. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

IIC1BR[2:0]: Baud rate selection (master mode only), where Fosc is the external crystal or oscillator frequency. The default is Fosc/(128+5) for users' convenience.

IIC1BR[2:0]	Baud rate
000	Fosc/(8+5)
001	Fosc/(16+5)
010	Fosc/(32+5)
011	Fosc/(64+5)
100	Fosc/(128+5)
101	Fosc/(256+5)
110	Fosc/(512+5)
111	Fosc/(1024+5)

Mnemonic: IIC1S **Address: E8H**

7	6	5	4	3	2	1	0	Reset
-	MPIF1	LAIF1	RXIF1	TXIF1	RXAK1	TXAK1	RW or BB	00H

MPIF1: The Stop condition Interrupt Flag

The stop condition occurred and this bit will be set. Software need to clear this bit

LAIF1: Arbitration lost bit. (Master mode only)

The Arbitration Interrupt Flag, the bus arbitration lost occurred and this bit will be set. Software need to clear this bit

RXIF1: The data Receive Interrupt Flag (RXIF1) is set after the IIC1RWD (IIC1 Read Write Data Buffer) is loaded with a newly receive data.

TXIF1: The data Transmit Interrupt Flag (TXIF1) is set when the data of the IIC1RWD (IIC1 Read Write Data Buffer) is downloaded to the shift register.

RXAK1: The Acknowledge Status indicate bit. When clear, it means an acknowledge signal has been received after the complete 8 bits data Transmit on the bus.

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TXAK1: The Acknowledge status Transmit bit. When received complete 8 bits data, this bit will set (NoAck) or clear (Ack) and Transmit to master to indicate the receive status.

RW or BB: Master Mode:

BB : Bus busy bit
If detect SCL=0 or SDA=0 or bus start, this bit will be set. If detect stop,this bit will be cleared. This bit can be cleared by software to return ready state.

Slave Mode:
RW:The slave mode read (received) or wrote (Transmit) on the IIC bus. When this bit is clear, the slave module received data on the IIC bus (SDA).(Slave mode only).
As shown in Fig.12-1.

Mnemonic: IIC1A1 **Address:EAH**

7	6	5	4	3	2	1	0	Reset
IIC1A1[7:1]							Match1 or RW1	A0H
R/W							R or R/W	

Slave mode:

IIC1A1[7:1]: IIC1 Address registers

This is the first 7-bit address for this slave module. It will be checked when an address (from master) is received

Match1: When IIC1A1 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.

Master mode:

IIC1A1[7:1]: IIC1 Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW1: This bit will be sent out as RW of the slave side if the module has set the FU1_EN[7:6] = 10. It appears at the 8th bit after the IIC address as below figure. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master Transmit mode. As shown in Fig.12-2.

RW1=1, master receive mode

RW1=0, master Transmit mode

Mnemonic: IIC1A2 **Address:EBH**

7	6	5	4	3	2	1	0	Reset
IIC1A2[7:1]							Match2 or RW2	60H
R/W							R or R/W	

Slave mode:

IIC1A2[7:1]: IIC1 Address registers

This is the second 7-bit address for this slave module.

It will be checked when an address (from master) is received

Match2: When IIC1A2 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.

Master mode:

IIC1A2[7:1]: IIC1 Address registers

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This 7-bit address indicates the slave with which it wants to communicate.

RW2: This bit will be sent out as RW of the slave side if the module has set the FU1_EN[7:6] = 10. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master Transmit mode.

RW2=1, master receive mode

RW2=0, master Transmit mode

Mnemonic: IIC1RWD **Address: ECh**

7	6	5	4	3	2	1	0	Reset
IIC1RWD[7:0]								00h

IIC1RWD[7:0]: IIC1 read write data buffer.

In receiving (read) mode, the received byte is stored here.

In Transmitting mode, the byte to be shifted out through SDA stays here.

Mnemonic: IIC1EBT **Address: EDH**

7	6	5	4	3	2	1	0	Reset
FU1_EN		-	-	-	-	-	-	00H

Master Mode：

00: reserved

01: IIC bus module will enable read/write data transfer on SDA and SCL.

10: IIC bus module generate a start condition on the SDA/SCL, then send out address which is stored in the IIC1A1/IIC1A2(selected by MAS control bit)

11: IIC bus module generates a stop condition on the SDA/SCL.

FU1_EN[7:6] will be auto-clear by hardware, so setting FU1_EN[7:6] repeatedly is necessary.

Slave mode:

01: FU1_EN[7:6] should be set as 01 only. The other value is inhibited.

Notice:

FU1_EN[7:6] should be set as 01 before read/write data transfer for bus release; otherwise, SCL will be locked(pull low).

FU1_EN[7:6] should be set as 01 after read/write data transfer for receiving a stop condition from bus master.

In Transmit data mode(slave mode), the output data should be filled into IIC1RWD before setting FU1_EN[7:6] as 01.

FU1_EN[7:6] will be auto-clear by hardware, so setting FU1_EN[7:6] repeatedly is necessary.

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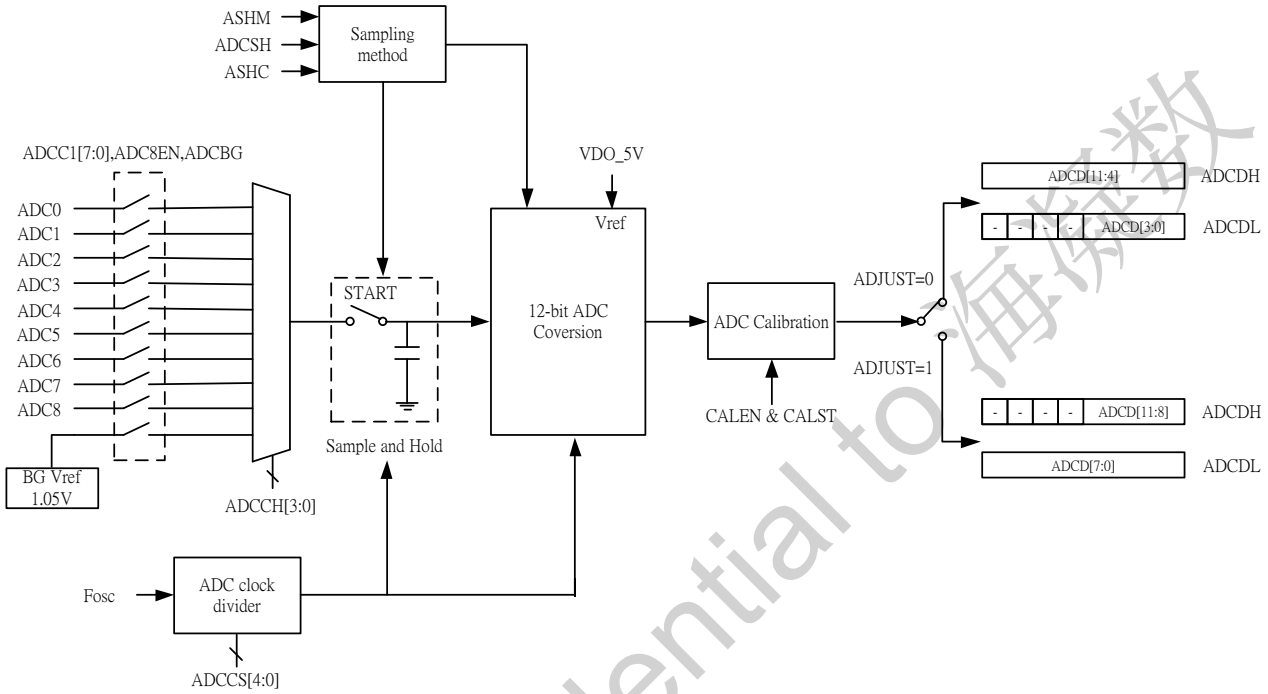
14. ADC

The OB39R32T2 provides ten channels 12-bit ADC. The Digital output DATA [11:0] were put into ADCD [11:0].



The ADC SFR show as below:

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
ADC											
ADCC1	ADC Control 1	ABH	ADC7EN	ADC6EN	ADC5EN	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	00H
ADCC2	ADC Control 2	ACH	START	ADJUST	ASHM	ASHC	ADCCH[3:0]				00H
ADCDH	ADC Data High	ADH	ADCDH [7:0]								00H
ADCDL	ADC Data Low	AEH	ADCDL [7:0]								00H
ADCCS	ADC Clock Select	AFH	ADCBGE	ADC8EN	-	ADCCS[4:0]					00H
ADCSH	ADC Sample and Hold Time	EFH	ADCSH[7:0]								00H

ADC Calibration:

Mnemonic	Description	Indirect	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
ADCCAL	ADC Calibration	FFFFH	-	-	-	-	-	-	CALEN	CALST	02H

Mnemonic: ADCC1 **Address: ABH**

7	6	5	4	3	2	1	0	Reset
ADC7EN	ADC6EN	ADC5EN	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	00H

ADC7EN: ADC channel 7 enable.

0: Disable ADC channel 7

1: Enable ADC channel 7

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ADC6EN: ADC channel 6 enable.

0: Disable ADC channel 6

1: Enable ADC channel 6

ADC5EN: ADC channel 5 enable.

0: Disable ADC channel 5

1: Enable ADC channel 5

ADC4EN: ADC channel 4 enable.

0: Disable ADC channel 4

1: Enable ADC channel 4

ADC3EN: ADC channel 3 enable.

0: Disable ADC channel 3

1: Enable ADC channel 3

ADC2EN: ADC channel 2 enable.

0: Disable ADC channel 2

1: Enable ADC channel 2

ADC1EN: ADC channel 1 enable.

0: Disable ADC channel 1

1: Enable ADC channel 1

ADC0EN: ADC channel 0 enable.

0: Disable ADC channel 0

1: Enable ADC channel 0

Mnemonic: ADCC2 **Address: ACH**

7	6	5	4	3	2	1	0	Reset
START	ADJUST	ASHM	ASHC	ADCCH[3:0]				00H

START: When this bit is set, the ADC will be start single-shot conversion.

ADJUST: Adjust the format of ADC conversion DATA.

0: (default value)

ADC data high byte ADCDH [7:0] = ADCD [11:4].

ADC data low byte ADCDL [3:0] = ADCD [3:0].

1:

ADC data high byte ADCDH [3:0] = ADCD [11:8].

ADC data low byte ADCDL [7:0] = ADCD [7:0].

ASHM: ADC sample and hold mode :

ASHM=0: ADC sampling time is controlled by hardware.

ASHM=1: ADC sampling time is controlled by firmware.

ASHC: ADC sample and hold control bit. This control bit for ASHM=1.

ASHC=0: Disable ADC sampling.

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ASHC=1: Enable ADC sampling.

ADCCH[3:0]: ADC channel select.

ADCCH [3:0]	Channel
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
Others	Bandgap reference voltage

ADJUST = 0:

Mnemonic: ADCDH **Address: ADH**

7	6	5	4	3	2	1	0	Reset
ADCD[11:4]								00H

Mnemonic: ADCDL **Address: AEH**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	ADCD[3:0]				00H

ADJUST = 1:

Mnemonic: ADCDH **Address: ADH**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	ADCD[11:8]				00H

Mnemonic: ADCDL **Address: AEH**

7	6	5	4	3	2	1	0	Reset
ADCD[7:0]								00H

ADCD[11:0]: ADC data register.

Mnemonic: ADCSH **Address: EFH**

7	6	5	4	3	2	1	0	Reset
ADCSH[7:0]								00H

ADCSH[7:0]: ADC sample and hold time register. This register for ASHM=0.

Mnemonic: ADCCS **Address: AFH**

7	6	5	4	3	2	1	0	Reset
ADCBGE	ADC8EN	-	ADCCS[4:0]					00H

ADCBGE: ADC bandgap reference voltage channel enable.

(bandgap reference voltage 1.05V +/- 2%)

0: Disable

1: Enable

ADC8EN: ADC channel 8 enable.

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0: Disable ADC channel 8

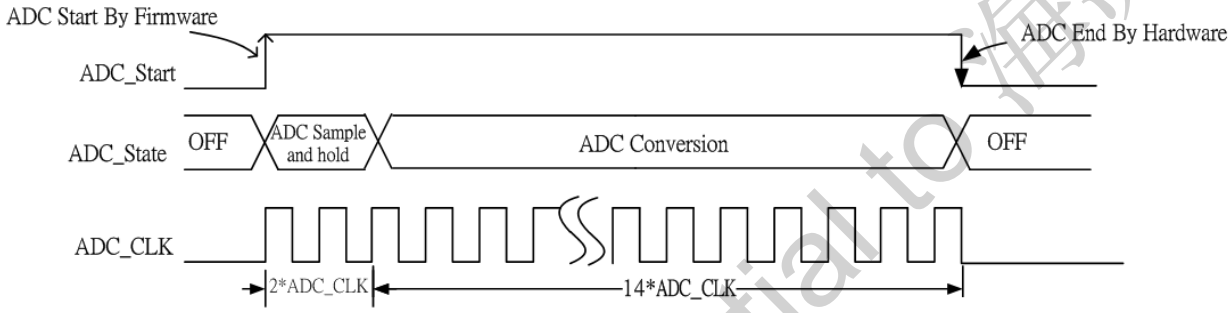
1: Enable ADC channel 8

ADCCS[4:0]: ADC clock select.

$$ADC\_Clock = \frac{\text{Fclk}}{6 \times (ADCCS[4:0] + 1)}$$

If ASHM=0 , ADCSH=0x00:

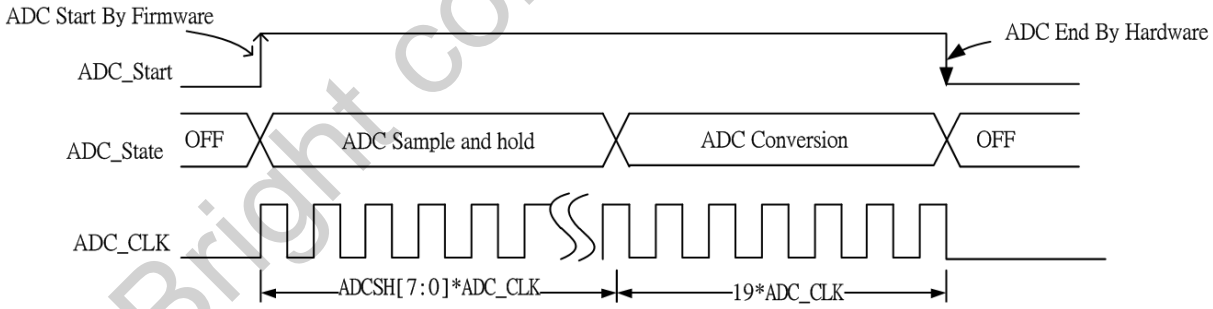
$$ADC\_Conversion\_Rate = \frac{\text{ADC\_Clock}}{16}$$



If ASHM=0 , ADCSH≠0x00:

$$ADC\_Conversion\_Rate = \frac{\text{ADC\_Clock}}{19 + \text{ADCSH}[7:0]}$$

※Sample and hold time by hardware control decisions.



If ASHM=1:

$$ADC\_Conversion\_Rate = \frac{\text{ADC\_Clock}}{16} + F/W\_Sampling\_Time$$

※Sample and hold time by firmware control decisions.

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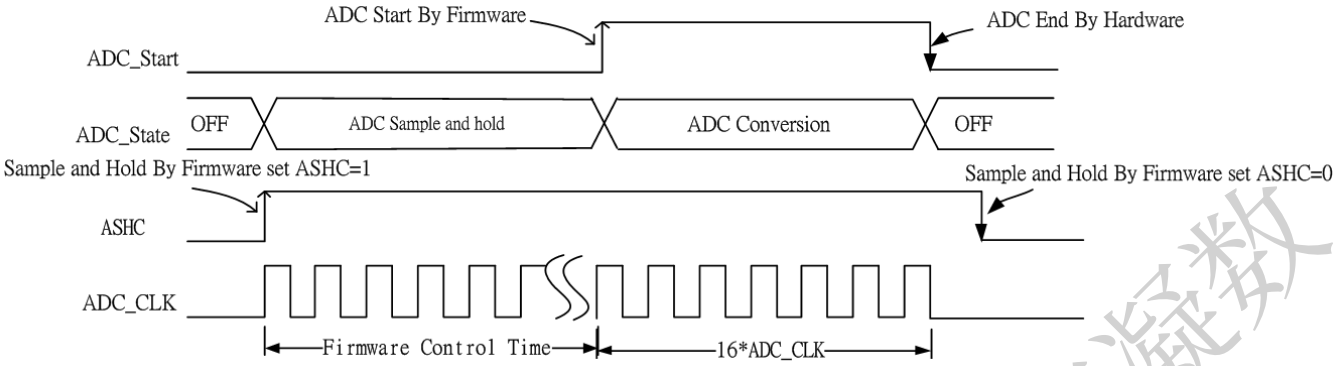

Mnemonic: ADCCAL **Indirect Address: FFFFH**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	CALEN	CALST	02H

CALEN: ADC calibration enable

0: Disable

1: Enable

※ If CALEN and ADCxEN both set to "1", ADC execute conversion according to the calibrated parameter. It will cost some conversion time to complete ADC conversion.

CALST: ADC calibration start

0: Calibration complete (Hardware will clear this bit automatically to indicate the calibration has been finished)

1: Start calibration (Software set this bit to start calibration)

Calibration for sample code:
C language:

```
unsigned char xdata ADCCAL  _at_ 0xFFFF;
void ADC_Calibration(bit bEnable)
{
   if(bEnable==1)
   {
      ADCCAL=0x00;   // Set ADCCAL=0x00;
      ADCCAL=0x03;    // Set ADCCAL=0x03;
      while((ADCCAL&0x01)==0x01);    // End wait for ADC calibration
   }
}
void main(void)
{
      :
      :
      ADC_Calibration(1);       //ADC Calibration
}
```

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Assembly language:

```
ADCCAL equ 0xFFFF
    :
ADC_Calibration:
    mov DPTR,#ADCCAL
    mov A,#0x00
    movx @DPTR,A        ;set ADCCAL=0x00;
    mov A,#0x03
    movx @DPTR,A        ;set ADCCAL=0x03;
WAIT:
    movx A,@DPTR
    anl A,#0x01
    jnz WATT            ; End wait for ADC calibration
    ret
```

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15. LVI & LVR – Low Voltage Interrupt and Low Voltage Reset

The interrupt vector 63h

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
LVR											
RSTS	Reset status register	A1h	-	-	-	-	WDTRF	SWRF	LVRF	PORF	00H
LVC	Low voltage control register	E6h	LVI_EN	LVRLPE	LVRE	LVIF	-	-	LVIS[1:0]		6xH

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	WDTRF	SWRF	LVRF	PORF	00H

LVRF: Low voltage reset flag.

When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.

PORF: Power on reset flag.

When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

Mnemonic: LVC **Address: E6h**

7	6	5	4	3	2	1	0	Reset
LVI_EN	LVRLPE	LVRE	LVIF	-	-	LVIS[1:0]		60H

LVI_EN: Low voltage interrupt function enable bit.

LVI_EN = 0 - disable low voltage detect function.

LVI_EN = 1 - enable low voltage detect function.

LVRLPE: External low voltage reset function (Low Power)enable bit.

LVRLPE = 0 - disable external low voltage reset(Low Power) function.

LVRLPE = 1 - enable external low voltage reset(Low Power) function.

Note:Low Power LVR = 1.2 V

LVRE: External low voltage reset function enable bit.

LVRXE = 0 - disable external low voltage reset function.

LVRXE = 1 - enable external low voltage reset function.

Note:Normal LVR = 1.55V / 2.7 V

LVIF: Low Voltage interrupt Flag(i.e., Low Voltage Interrupt Status Flag)

LVIS[1:0]: LVI level select:

00: 1.80V

01: 2.80V

10: 3.30V

11: 4.00V

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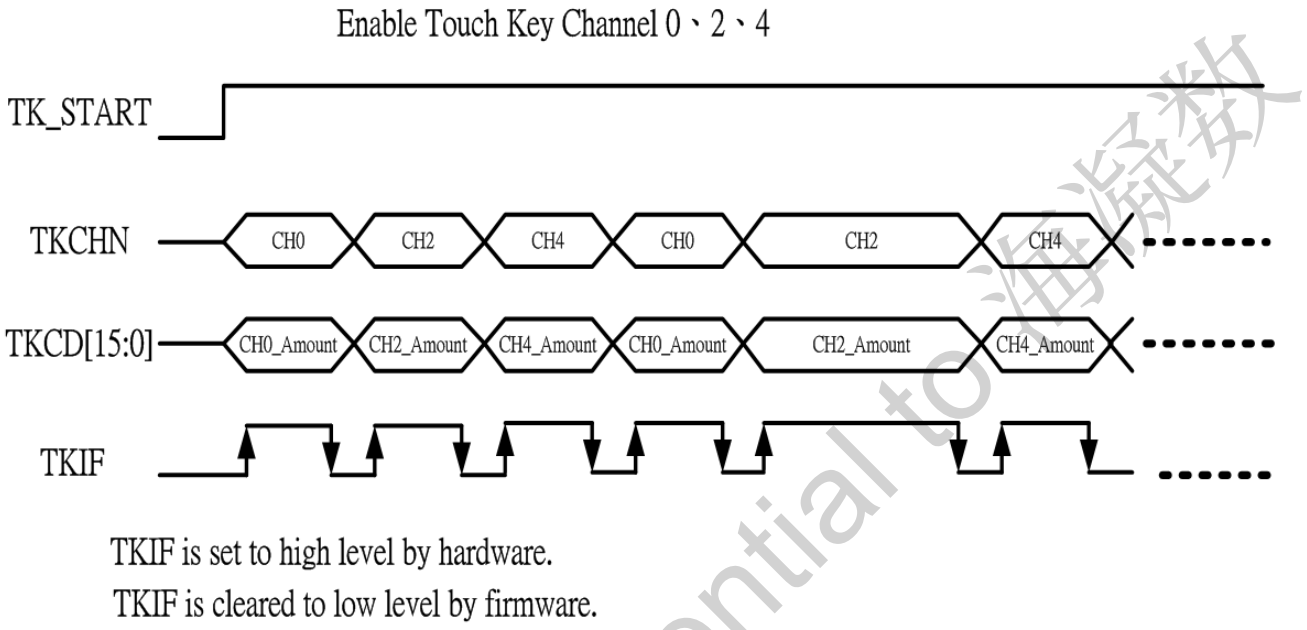
16. Touch Sense Unit



TKIF is set to high level by hardware.
TKIF is cleared to low level by firmware.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Interrupt											
IEN2	Interrupt Enable 2 register	9AH	-	-	-	IESRTC	IETK	EX3	EWDT	ES1	00H
IRCON2	Interrupt request register 2	97H	-	-	-	SRTCIF	TKIF	-	WDT IF	-	00H
TKCON	Touch Key Control Reg.	9BH	TK_START	TK_PS	-	-	TK_SPEED[3:0]				00H
TKSW	Touch Key Switch Reg.	9CH	TKSIF	LEDSIF		NSP	VTK[1:0]		DTS[1:0]		00H
TKCHN	Touch Key Channel Number Reg.	9DH	-	-	-	TKCHN[4:0]					00H
TKCDL	Touch Key Capture Data Low-byte Reg.	9EH	TKCD[7:0]								00H
TKCDH	Touch Key Capture Data Hi-byte Reg.	9FH	TKCD[15:8]								00H
TKSTATUS0	Touch Key Status 0 Reg.	FEH	TKSTATUS0[7:0]								00H
TKSTATUS1	Touch Key Status 1 Reg.	BBH	TKSTATUS1[15:8]								00H
TKSTATUS2	Touch Key Status 2 Reg.	93H	TKSTATUS2[23:16]								00H

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Description	Indirect	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	Reset
TKEN0	FFF3H	TK7EN	TK6EN	TK5EN	TK4EN	TK3EN	TK2EN	TK1EN	TK0EN	00H
TKEN1	FFF2H	TK15EN	TK14EN	TK13EN	TK12EN	TK11EN	TK10EN	TK9EN	TK8EN	00H
TKEN2	FFF1H	TK23EN	TK22EN	TK21EN	TK20EN	TK19EN	TK18EN	TK17EN	TK16EN	00H
TKRUNTIME	FFF4H	TKRUNTIME[7:0]								00H
TKPSSR	FFF5H	TKPSSR[7:0]								07H
TKWKTRICNT	FFF6H	TKWKTRICNT[7:0]								02H

Description	Indirect	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	Reset
TK0TRIGH	0x05B4	TK0TRIG[15:8]								unknown
TK0TRIGL	0x05B5	TK0TRIG[7:0]								unknown
TK1TRIGH	0x05B6	TK1TRIG[15:8]								unknown
TK1TRIGL	0x05B7	TK1TRIG[7:0]								unknown
TK2TRIGH	0x05B8	TK2TRIG[15:8]								unknown
TK2TRIGL	0x05B9	TK2TRIG[7:0]								unknown
TK3TRIGH	0x05BA	TK3TRIG[15:8]								unknown
TK3TRIGL	0x05BB	TK3TRIG[7:0]								unknown
TK4TRIGH	0x05BC	TK4TRIG[15:8]								unknown
TK4TRIGL	0x05BD	TK4TRIG[7:0]								unknown
TK5TRIGH	0x05BE	TK5TRIG[15:8]								unknown
TK5TRIGL	0x05BF	TK5TRIG[7:0]								unknown
TK6TRIGH	0x05C0	TK6TRIG[15:8]								unknown
TK6TRIGL	0x05C1	TK6TRIG[7:0]								unknown
TK7TRIGH	0x05C2	TK7TRIG[15:8]								unknown
TK7TRIGL	0x05C3	TK7TRIG[7:0]								unknown
TK8TRIGH	0x05C4	TK8TRIG[15:8]								unknown
TK8TRIGL	0x05C5	TK8TRIG[7:0]								unknown
TK9TRIGH	0x05C6	TK9TRIG[15:8]								unknown
TK9TRIGL	0x05C7	TK9TRIG[7:0]								unknown
TK10TRIGH	0x05C8	TK10TRIG[15:8]								unknown
TK10TRIGL	0x05C9	TK10TRIG[7:0]								unknown
TK11TRIGH	0x05CA	TK11TRIG[15:8]								unknown
TK11TRIGL	0x05CB	TK11TRIG[7:0]								unknown
TK12TRIGH	0x05CC	TK12TRIG[15:8]								unknown
TK12TRIGL	0x05CD	TK12TRIG[7:0]								unknown
TK13TRIGH	0x05CE	TK13TRIG[15:8]								unknown
TK13TRIGL	0x05CF	TK13TRIG[7:0]								unknown
TK14TRIGH	0x05D0	TK14TRIG[15:8]								unknown

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TK14TRIGL	0x05D1	TK14TRIG[7:0]	unknown
TK15TRIGH	0x05D2	TK15TRIG[15:8]	unknown
TK15TRIGL	0x05D3	TK15TRIG[7:0]	unknown
TK16TRIGH	0x05D4	TK16TRIG[15:8]	unknown
TK16TRIGL	0x05D5	TK16TRIG[7:0]	unknown
TK17TRIGH	0x05D6	TK17TRIG[15:8]	unknown
TK17TRIGL	0x05D7	TK17TRIG[7:0]	unknown
TK18TRIGH	0x05D8	TK18TRIG[15:8]	unknown
TK18TRIGL	0x05D9	TK18TRIG[7:0]	unknown
TK19TRIGH	0x05DA	TK19TRIG[15:8]	unknown
TK19TRIGL	0x05DB	TK19TRIG[7:0]	unknown
TK20TRIGH	0x05DC	TK20TRIG[15:8]	unknown
TK20TRIGL	0x05DD	TK20TRIG[7:0]	unknown
TK21TRIGH	0x05DE	TK21TRIG[15:8]	unknown
TK21TRIGL	0x05DF	TK21TRIG[7:0]	unknown
TK22TRIGH	0x05E0	TK22TRIG[15:8]	unknown
TK22TRIGL	0x05E1	TK22TRIG[7:0]	unknown
TK23TRIGH	0x05E2	TK23TRIG[15:8]	unknown
TK23TRIGL	0x05E3	TK23TRIG[7:0]	unknown
TK0TRICNT	0x05E6	TK0TRICNT[7:0]	unknown
TK1TRICNT	0x05E7	TK1TRICNT[7:0]	unknown
TK2TRICNT	0x05E8	TK2TRICNT[7:0]	unknown
TK3TRICNT	0x05E9	TK3TRICNT[7:0]	unknown
TK4TRICNT	0x05EA	TK4TRICNT[7:0]	unknown
TK5TRICNT	0x05EB	TK5TRICNT[7:0]	unknown
TK6TRICNT	0x05EC	TK6TRICNT[7:0]	unknown
TK7TRICNT	0x05ED	TK7TRICNT[7:0]	unknown
TK8TRICNT	0x05EE	TK8TRICNT[7:0]	unknown
TK9TRICNT	0x05EF	TK9TRICNT[7:0]	unknown
TK10TRICNT	0x05F0	TK10TRICNT[7:0]	unknown
TK11TRICNT	0x05F1	TK11TRICNT[7:0]	unknown
TK12TRICNT	0x05F2	TK12TRICNT[7:0]	unknown
TK13TRICNT	0x05F3	TK13TRICNT[7:0]	unknown
TK14TRICNT	0x05F4	TK14TRICNT[7:0]	unknown
TK15TRICNT	0x05F5	TK15TRICNT[7:0]	unknown
TK16TRICNT	0x05F6	TK16TRICNT[7:0]	unknown
TK17TRICNT	0x05F7	TK17TRICNT[7:0]	unknown
TK18TRICNT	0x05F8	TK18TRICNT[7:0]	unknown
TK19TRICNT	0x05F9	TK19TRICNT[7:0]	unknown
TK20TRICNT	0x05FA	TK20TRICNT[7:0]	unknown

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TK21TRICNT	0x05FB	TK21TRICNT[7:0]	unknown
TK22TRICNT	0x05FC	TK22TRICNT[7:0]	unknown
TK23TRICNT	0x05FD	TK23TRICNT[7:0]	unknown

Mnemonic: IEN2 **Address: 9Ah**

7	6	5	4	3	2	1	0	Reset
-	-	-	IESRTC	IETK	EX3	EWDT	ES1	00H

IETK: IETK = 0 – Disable Touch Key interrupt.

IETK = 1 – Enable Touch Key interrupt.

Mnemonic:IRCON2 **Address: 97h**

7	6	5	4	3	2	1	0	Reset
-	-	-	SRTCIF	TKIF	-	WDTIF	-	00H

TKIF: Touch Key interrupt flag. Must be cleared by software.

Mnemonic: TKEN0 **Indirect Address: 0xFFF3**

7	6	5	4	3	2	1	0	Reset
TK7EN	TK6EN	TK5EN	TK4EN	TK3EN	TK2EN	TK1EN	TK0EN	00H

TK7EN: Touch key channels 7 enable.
TK7EN = 1 – Enable touch key channel 7
TK6EN: Touch key channels 6 enable.
TK6EN = 1 – Enable touch key channel 6
TK5EN: Touch key channels 5 enable.
TK5EN = 1 – Enable touch key channel 5
TK4EN: Touch key channels 4 enable.
TK4EN = 1 – Enable touch key channel 4
TK3EN: Touch key channels 3 enable.
TK3EN = 1 – Enable touch key channel 3
TK2EN: Touch key channels 2 enable.
TK2EN = 1 – Enable touch key channel 2
TK1EN: Touch key channels 1 enable.
TK1EN = 1 – Enable touch key channel 1
TK0EN: Touch key channels 0 enable.
TK0EN = 1 – Enable touch key channel 0

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Mnemonic: TKEN1 **Indirect Address: 0xFFF2**

7	6	5	4	3	2	1	0	Reset
TK15EN	TK14EN	TK13EN	TK12EN	TK11EN	TK10EN	TK9EN	TK8EN	00H

TK15EN: Touch key channels 15 enable.
TK15EN = 1 – Enable touch key channel 15
TK14EN: Touch key channels 14 enable.
TK14EN = 1 – Enable touch key channel 14
TK13EN: Touch key channels 13 enable.
TK13EN = 1 – Enable touch key channel 13
TK12EN: Touch key channels 12 enable.
TK12EN = 1 – Enable touch key channel 12
TK11EN: Touch key channels 11 enable.
TK11EN = 1 – Enable touch key channel 11
TK10EN: Touch key channels 10 enable.
TK10EN = 1 – Enable touch key channel 10
TK9EN: Touch key channels 9 enable.
TK9EN = 1 – Enable touch key channel 9
TK8EN: Touch key channels 8 enable.
TK8EN = 1 – Enable touch key channel 8

Mnemonic: TKEN2 **Indirect Address: 0xFFF1**

7	6	5	4	3	2	1	0	Reset
TK23EN	TK22EN	TK21EN	TK20EN	TK19EN	TK18EN	TK17EN	TK16EN	00H

TK23EN: Touch key channels 23 enable.
TK23EN = 1 – Enable touch key channel 23
TK22EN: Touch key channels 22 enable.
TK22EN = 1 – Enable touch key channel 22
TK21EN: Touch key channels 21 enable.
TK21EN = 1 – Enable touch key channel 21
TK20EN: Touch key channels 20 enable.
TK20EN = 1 – Enable touch key channel 20
TK19EN: Touch key channels 19 enable.
TK19EN = 1 – Enable touch key channel 19
TK18EN: Touch key channels 18 enable.
TK18EN = 1 – Enable touch key channel 18
TK17EN: Touch key channels 17 enable.
TK17EN = 1 – Enable touch key channel 17
TK16EN: Touch key channels 16 enable.
TK16EN = 1 – Enable touch key channel 16

Mnemonic: TKCON **Address: 9BH**

7	6	5	4	3	2	1	0	Reset
TK_ START	TK_PS	-	-	TK_SPEED[3:0]				00H

TK_START: 0 = The touch key will disable.
1 = The touch key will enable.
TK_PS: This register is select input clock for the touch key counter.
0— Input clock=44Mhz

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1— Input clock=22Mhz

TK_SPEED[3:0]: This register is select the charging speed of touch sensor.
TK_SPEED="0000" Charge Level 0 (fastest)
TK_SPEED="0001" Charge Level 1
:
TK_SPEED="1111" Charge Level 15 (slowest)

Mnemonic: TKSW **Address: 9CH**

7	6	5	4	3	2	1	0	Reset
TKSIF	LEDSIF	-	NSP	VTK[1:0]		DTS[1:0]		00H

TKSIF: The flag is set by hardware when touch function starts operating.
Must be cleared by software.

LEDSIF: The flag is set by hardware when LED function starts operating and touch function is turned on.
Must be cleared by software.

NSP: Port status of TK that currently have not been scanned (starting TK)
0—Floating.
1—Determined by the GPIO port setting.

VTK[1:0]: Touch the module voltage selection.

VTK[1:0]	Power Select	VDD working range
00	MCU VDD	2.2V ~ 5.5V
01	TK LDO	4.0V~ 5.5V
10	TK LDO	3.3V~ 5.5V
11	TK LDO	2.7V~ 5.5V

DTS[1:0]: Discharge time selection.
00—64*45ns
01—128*45ns
10—192*45ns
11—224*45ns

Mnemonic: TKCHN **Address: 9Dh**

7	6	5	4	3	2	1	0	Reset
-	-	-	TKCHN[4:0]					00H

TKCHN[4:0]: This register indicates the counter scanning channels (Read only).

Mnemonic: TKCDL **Address: 9Eh**

7	6	5	4	3	2	1	0	Reset
TKCD[7:0]								00H

TKCD[7:0]: This register for 16 bits counter low byte contents (Read only).

Mnemonic: TKCDH **Address: 9Fh**

7	6	5	4	3	2	1	0	Reset
TKCD[15:8]								00H

TKCD[15:8]: This register for 16 bits counter high byte contents (Read only).

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Mnemonic: TKRUNTIME **Indirect Address: 0xFFF4**

7	6	5	4	3	2	1	0	Reset
TKRUNTIME[7:0]								00H

TKRUNTIME[7:0]: Touch key running time.

This setting is valid only when LED and Touch function is enable. This value determines the touch running time.

Touch Key Running Time= TKRUNTIME[7:0]/ LED Clock

※ If TKRUNTIME=" 0x00 " , LED and Touch key share pad is disable.

Mnemonic: TKPSSR **Indirect Address: 0xFFF5**

7	6	5	4	3	2	1	0	Reset
TKPSSR [7:0]								07H

TKPSSR [7:0]: This setting is for the sampling rate of the touch key in power saving mode.
Sampling Rate=26KHz/[256*(TKPSSR [7:0]+1)]

Mnemonic: TKWKTRICNT **Indirect Address: 0xFFF6**

7	6	5	4	3	2	1	0	Reset
TKWKTRICNT [7:0]								02H

TKWKTRICNT [7:0]: This setting is for wake-up after the touch key reaches the trigger value in power saving mode.

Mnemonic: TKxTRIGH、TKxTRIGL **Indirect Address: 0x04B4~0x04E3**

7	6	5	4	3	2	1	0	Reset
TKxTRIG[15:8]								00H
TKxTRIG[7:0]								00H

TKxTRIG [15:0]: This setting the touch key trigger value.

Mnemonic: TKxTRICNT **Indirect Address: 0x04E6~0x04FD**

7	6	5	4	3	2	1	0	Reset
TKxTRICNT [7:0]								00H

TKxTRICNT [7:0]: This records the number of triggers.

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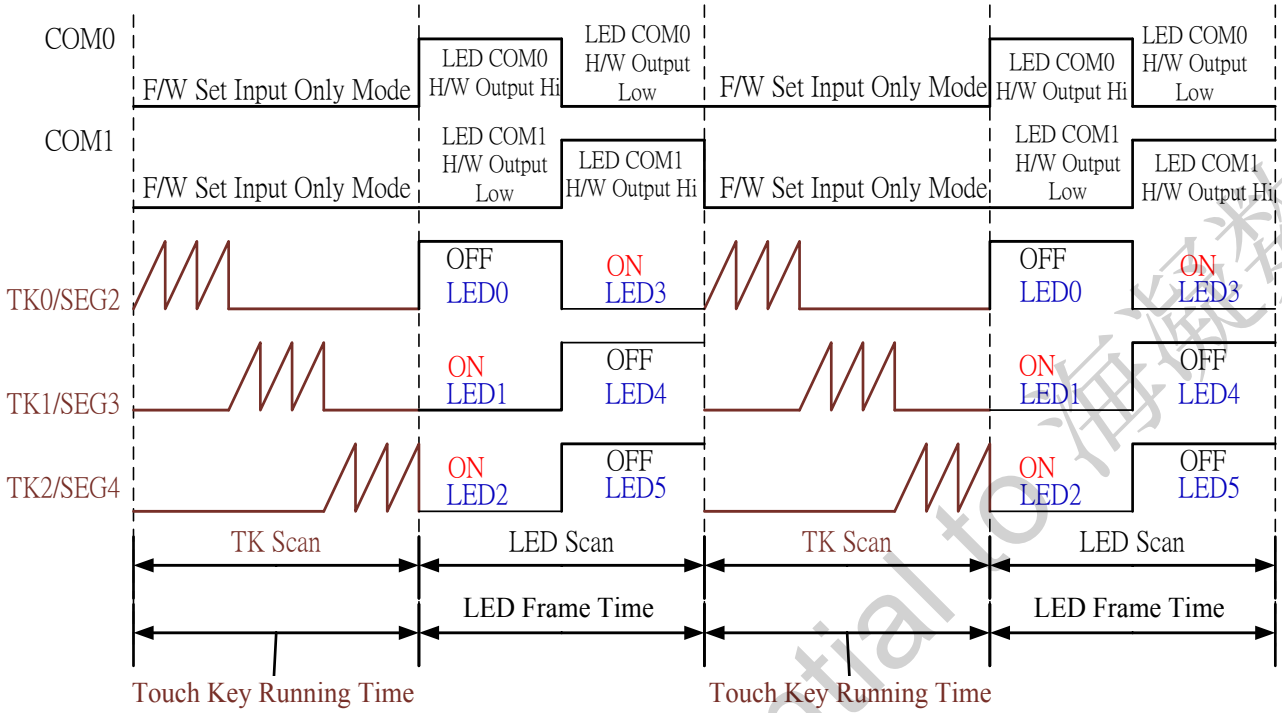
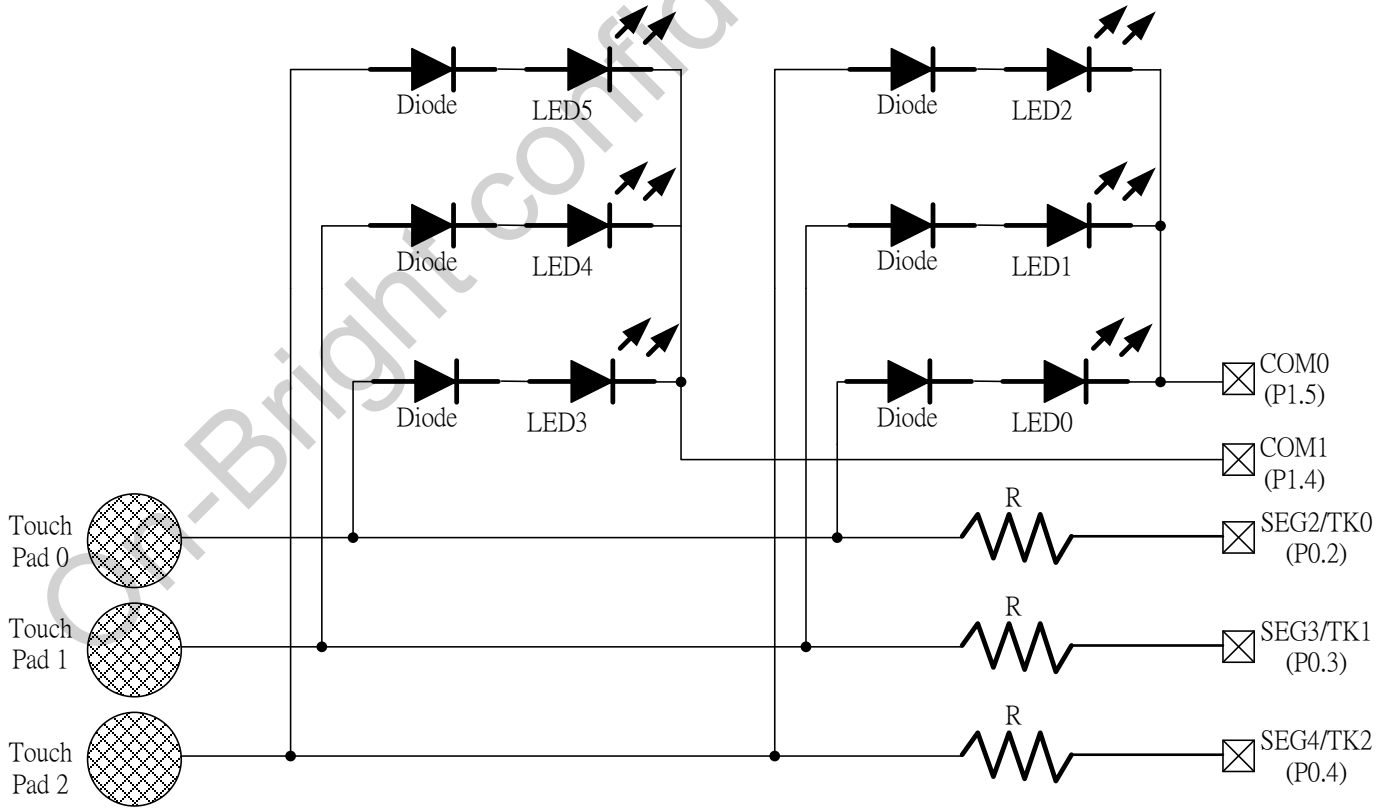
Touch Key & LED Share Timing



Touch Key & LED Share Application Circuit



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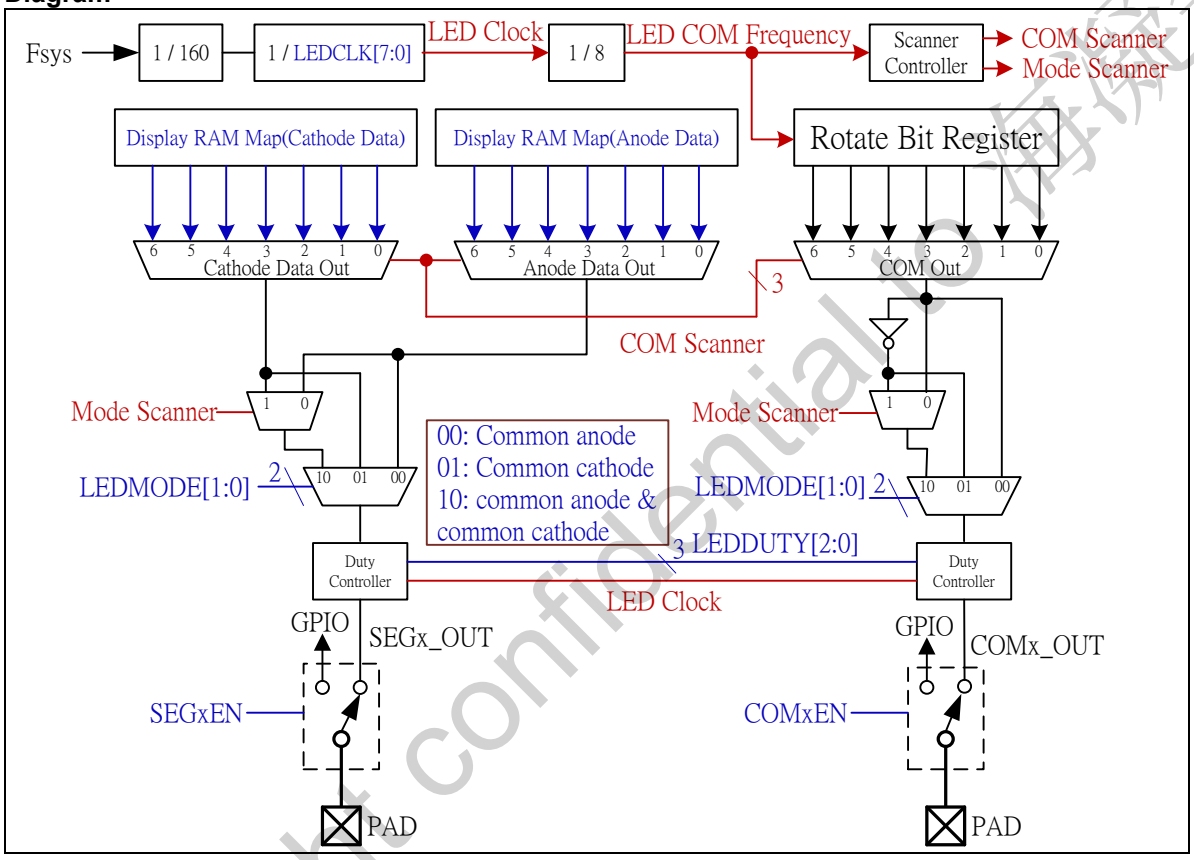
17. LED Driver

- LED selectable duty : 1/8~8/8(full-duty)
- LED maximum SEG-driver 16 pins, COM-driver 7 pins
- Support common anode、 common cathode and multi-mode waveform.

Block Diagram



Description	Indirect	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	RST
COMEN	0xFF1C	-	COM6EN	COM5EN	COM4EN	COM3EN	COM2EN	COM1EN	COM0EN	0x00
SEGEN0	0xFF1D	SEG7EN	SEG6EN	SEG5EN	SEG4EN	SEG3EN	SEG2EN	SEG1EN	SEG0EN	0x00
SEGEN1	0xFF1E	SEG15EN	SEG14EN	SEG13EN	SEG12EN	SEG11EN	SEG10EN	SEG9EN	SEG8EN	0x00
LEDCON	0xFF1F	LEDEN	-	LEDMODE[1:0]		-	LEDDUTY[2:0]			0x00
LEDCLK	0xFF20	LEDCLK[7:0]								0x00

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17.1 Display RAM Map

The display RAM is a static 28x8 bits RAM which stores the LED data. A logic "1" state in the RAM bit cell indicates the "ON" state of the corresponding LED segment. Similarly, logic "0" indicates the "OFF" state.

Description	Indirect	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	RST
COM0_AH	0xFF00	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM0_AL	0xFF01	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM1_AH	0xFF02	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM1_AL	0xFF03	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM2_AH	0xFF04	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM2_AL	0xFF05	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM3_AH	0xFF06	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM3_AL	0xFF07	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM4_AH	0xFF08	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM4_AL	0xFF09	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM5_AH	0xFF0A	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM5_AL	0xFF0B	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM6_AH	0xFF0C	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM6_AL	0xFF0D	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM0_CH	0xFF0E	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM0_CL	0xFF0F	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM1_CH	0xFF10	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM1_CL	0xFF11	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM2_CH	0xFF12	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM2_CL	0xFF13	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM3_CH	0xFF14	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM3_CL	0xFF15	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM4_CH	0xFF16	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM4_CL	0xFF17	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM5_CH	0xFF18	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM5_CL	0xFF19	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00
COM6_CH	0xFF1A	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	0x00
COM6_CL	0xFF1B	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	0x00

Mnemonic: COMEN **Indirect Address: 0xFF1C**

7	6	5	4	3	2	1	0	Reset
-	COM6EN	COM5EN	COM4EN	COM3EN	COM2EN	COM1EN	COM0EN	00H

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COM6EN: 1: COM6 enable

0: COM6 disable

COM5EN: 1: COM5 enable

0: COM5 disable

※COM5 and SEG1 cannot both be enabled.

COM4EN: 1: COM4 enable

0: COM4 disable

※COM4 and SEG0 cannot both be enabled.

COM3EN: 1: COM3 enable

0: COM3 disable

COM2EN: 1: COM2 enable

0: COM2 disable

COM1EN: 1: COM1 enable

0: COM1 disable

COM0EN: 1: COM0 enable

0: COM0 disable

Mnemonic: SEGEN0 **Indirect Address: 0xFF1D**

7	6	5	4	3	2	1	0	Reset
SEG7EN	SEG6EN	SEG5EN	SEG4EN	SEG3EN	SEG2EN	SEG1EN	SEG0EN	00H

SEG7EN: 1: SEG7 enable

0: SEG7 disable

SEG6EN: 1: SEG6 enable

0: SEG6 disable

SEG5EN: 1: SEG5 enable

0: SEG5 disable

SEG4EN: 1: SEG4 enable

0: SEG4 disable

SEG3EN: 1: SEG3 enable

0: SEG3 disable

SEG2EN: 1: SEG2 enable

0: SEG2 disable

SEG1EN: 1: SEG1 enable

0: SEG1 disable

※COM5 and SEG1 cannot both be enabled.

SEG0EN: 1: SEG0 enable

0: SEG0 disable

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※COM4 and SEG0 cannot both be enabled.

Mnemonic: SEGEN1 **Indirect Address: 0xFF1E**

7	6	5	4	3	2	1	0	Reset
SEG15EN	SEG14EN	SEG13EN	SEG12EN	SEG11EN	SEG10EN	SEG9EN	SEG8EN	00H

SEG15EN: 1: SEG15 enable
0: SEG15 disable
SEG14EN: 1: SEG14 enable
0: SEG14 disable
SEG13EN: 1: SEG13 enable
0: SEG13 disable
SEG12EN: 1: SEG12 enable
0: SEG12 disable
SEG11EN: 1: SEG11 enable
0: SEG11 disable
SEG10EN: 1: SEG10 enable
0: SEG10 disable
SEG9EN: 1: SEG9 enable
0: SEG9 disable
SEG8EN: 1: SEG8 enable
0: SEG8 disable

Mnemonic: LEDCON **Indirect Address: 0xFF1F**

7	6	5	4	3	2	1	0	Reset
LEDEN	-	LEDMODE[1:0]		-	LEDDUTY[2:0]			00H

LEDEN: 1: LED scan enable
0: LED scan disable
LEDMODE[1:0]: LED mode Select:
00: Select common anode.
01: Select common cathode.
10: Select common anode & common cathode. (Does not support the use of touch buttons at the same time)
11: Reserve
LEDDUTY[2:0]: LED duty select:
001:1/8 duty
010:2/8 duty
011:3/8 duty
100:4/8 duty

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101:5/8 duty

110:6/8 duty

111:7/8 duty

000:8/8duty

Mnemonic: LEDCLK **Indirect Address: 0xFF20**

7	6	5	4	3	2	1	0	Reset
LEDCLK[7:0]								00H

LEDCLK: LED clock select:

LED Clock = Fsys / [160*(LEDCLK[7:0]+1)]

LED COM Frequency = LED Clock/8

LED Frame Rata= LED COM Frequency /(COM enable Number)

LED Frame Time=(COM enable Number) / LED COM Frequency

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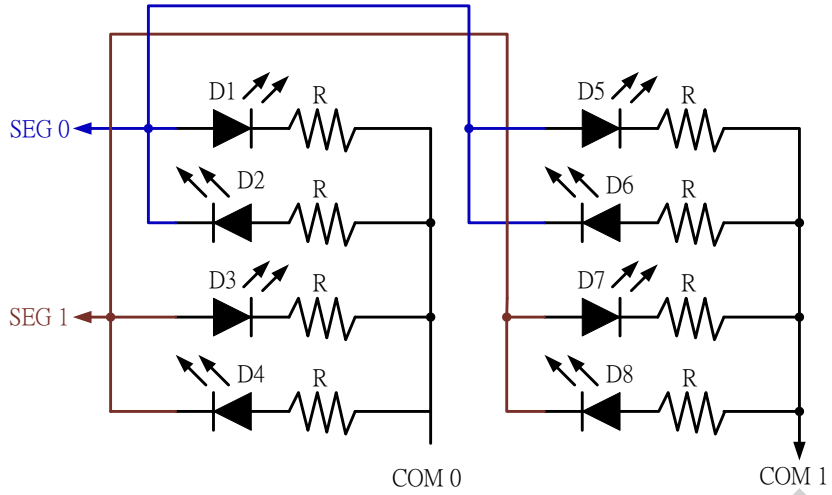
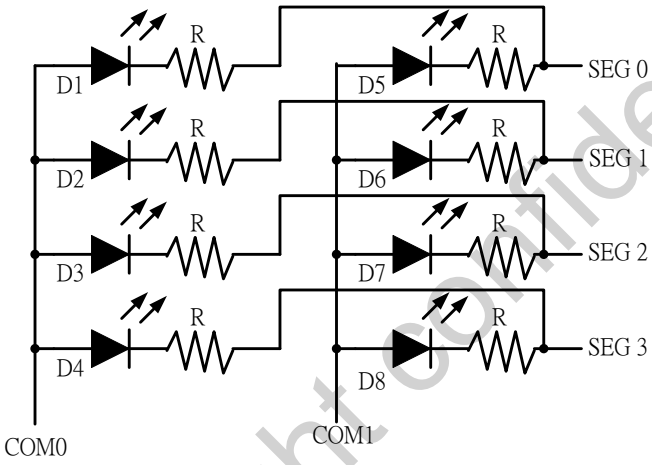
17.2 LED application circuit

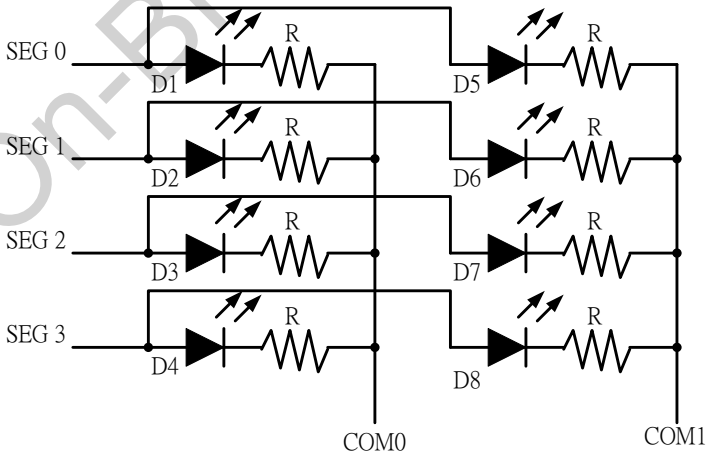
17.2.1 Common Anode & Common Cathode Mode



17.2.2 Common Anode Mode



17.2.3 Common Cathode Mode



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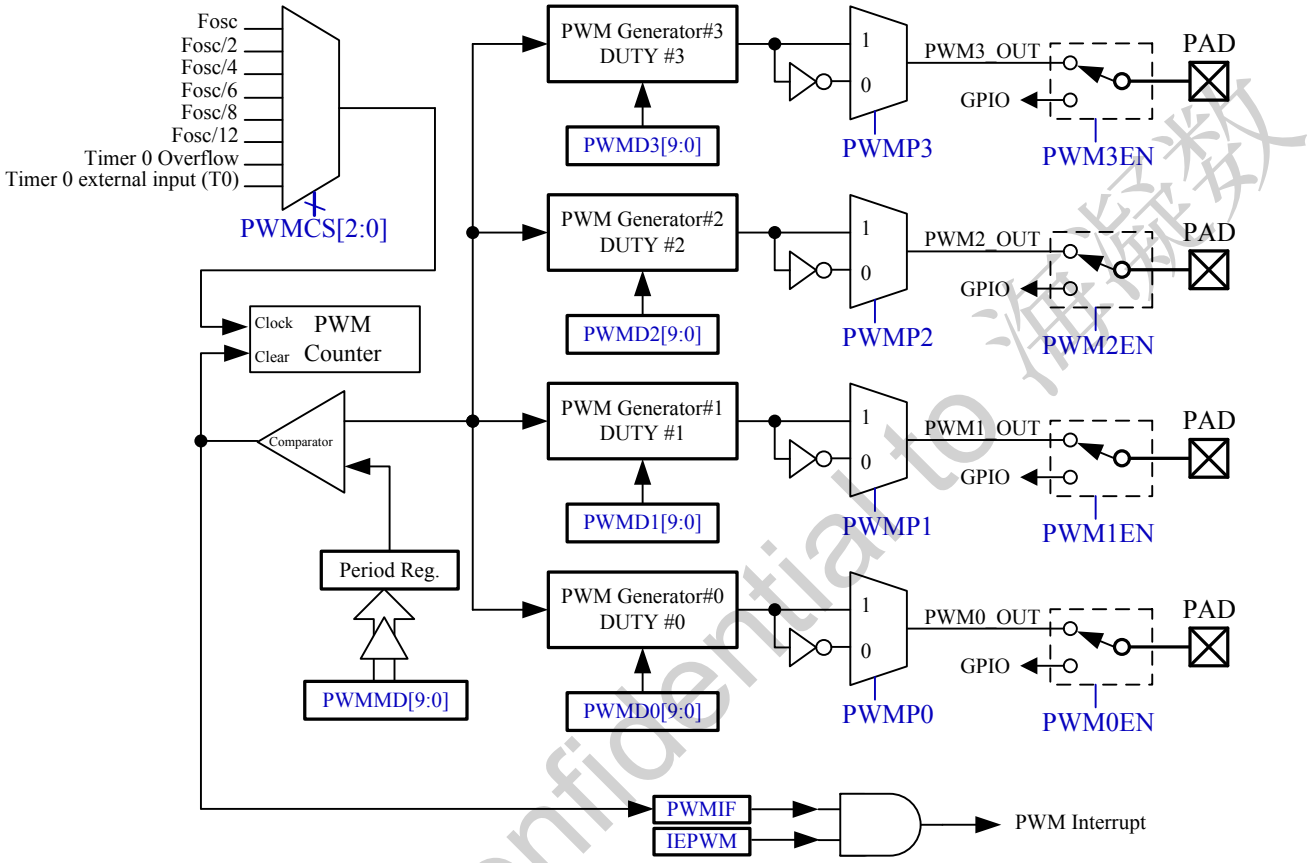
18. PWM - Pulse Width Modulation

The OB39R32T2 provides four channel PWM output.



Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
PWM											
PWMC	PWM Control register	B5h	PWMCS[2:0]			-	PWM3EN	PWM2EN	PWM1EN	PWM0EN	00H
PWMD0H	PWM 0 Data register high byte	BDh	PWMP0	-	-	-	-	-	PWMD0[9:8]		00H
PWMD0L	PWM 0 Data register low byte	BCh	PWMD0[7:0]								00H
PWMD1H	PWM 1 Data register high byte	BFh	PWMP1	-	-	-	-	-	PWMD1[9:8]		00H
PWMD1L	PWM 1 Data register low byte	BEh	PWMD1[7:0]								00H
PWMD2H	PWM 2 Data register high byte	B2h	PWMP2	-	-	-	-	-	PWMD2[9:8]		00H
PWMD2L	PWM 2 Data register low byte	B1h	PWMD2[7:0]								00H
PWMD3H	PWM 3 Data register high byte	B4h	PWMP3	-	-	-	-	-	PWMD3[9:8]		00H
PWMD3L	PWM 3 Data register low byte	B3h	PWMD3[7:0]								00H
PWMMDH	PWM Max Data register high byte	CFh	-	-	-	-	-	-	PWMMD[9:8]		00H

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PWMMDL	PWM Max Data register low byte	CEh	PWMMD[7:0]	FFH

Mnemonic: PWMC **Address: B5h**

7	6	5	4	3	2	1	0	Reset
PWMCS[2:0]			-	PWM3EN	PWM2EN	PWM1EN	PWM0EN	00H

PWMCS[2:0]: PWM clock select.

PWMCS [2:0]	Mode
000	Fosc
001	Fosc/2
010	Fosc/4
011	Fosc/6
100	Fosc/8
101	Fosc/12
110	Timer 0 overflow
111	Timer 0 external input (P0.0/T0)

PWM3EN: PWM channel 3 enable control bit.

PWM3EN = 1 – PWM channel 3 enable.

PWM3EN = 0 – PWM channel 3 disable.

PWM2EN: PWM channel 2 enable control bit.

PWM2EN = 1 – PWM channel 2 enable.

PWM2EN = 0 – PWM channel 2 disable.

PWM1EN: PWM channel 1 enable control bit.

PWM1EN = 1 – PWM channel 1 enable.

PWM1EN = 0 – PWM channel 1 disable.

PWM0EN: PWM 0 enable control bit.

PWM0EN = 1 – PWM channel 0 enable.

PWM0EN = 0 – PWM channel 0 disable.

Mnemonic: PWMD0H **Address: BDh**

7	6	5	4	3	2	1	0	Reset
PWMP0	-	-	-	-	-	PWMD0[9:8]		00H

Mnemonic: PWMD0L **Address: BCh**

7	6	5	4	3	2	1	0	Reset
PWMD0[7:0]								00H

PWMP0: PWM channel 0 idle polarity select.

"0" – PWM channel 0 will idle low.

"1" – PWM channel 0 will idle high.

PWMD0[9:0]: PWM channel 0 data register.

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Mnemonic: PWMD1H **Address: BFh**

7	6	5	4	3	2	1	0	Reset
PWMP1	-	-	-	-	-	PWMD1[9:8]		00H

Mnemonic: PWMD1L **Address: BEh**

7	6	5	4	3	2	1	0	Reset
PWMD1[7:0]								00H

PWMP1: PWM channel 1 idle polarity select.

"0" – PWM channel 1 will idle low.

"1" – PWM channel 1 will idle high.

PWMD1[9:0]: PWM channel 1 data register.

Mnemonic: PWMD2H **Address: B2h**

7	6	5	4	3	2	1	0	Reset
PWMP2	-	-	-	-	-	PWMD2[9:8]		00H

Mnemonic: PWMD2L **Address: B1h**

7	6	5	4	3	2	1	0	Reset
PWMD2[7:0]								00H

PWMP2: PWM channel 2 idle polarity select.

"0" – PWM channel 2 will idle low.

"1" – PWM channel 2 will idle high.

PWMD2[9:0]: PWM channel 2 data register.

Mnemonic: PWMD3H **Address: B4h**

7	6	5	4	3	2	1	0	Reset
PWMP3	-	-	-	-	-	PWMD3[9:8]		00H

Mnemonic: PWMD3L **Address: B3h**

7	6	5	4	3	2	1	0	Reset
PWMD3[7:0]								00H

PWMP3: PWM channel 3 idle polarity select.

"0" – PWM channel 3 will idle low.

"1" – PWM channel 3 will idle high.

PWMD3[9:0]: PWM channel 3 data register.

Mnemonic: PWMMDH **Address: CFh**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	PWMMD[9:8]		00H

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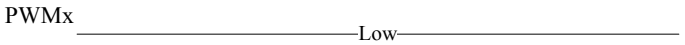
Mnemonic: PWMMDL **Address: CEh**

7	6	5	4	3	2	1	0	Reset
PWMMD[7:0]								FFH

PWMMD[9:0]: PWM Max Data register.

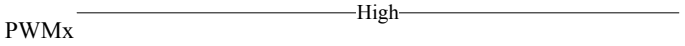
PWM count from 0000h to PWMMD[9:0]. When PWM count data equal PWMMD[9:0] is overflow.

PWMPx = 0 & PWMDx = 00h



PWMPx = 0 & PWMDx ≠ 00h

PWMPx = 1 & PWMDx = 00h



PWMPx = 1 & PWMDx ≠ 00h

$$\text{PWM period} = \frac{\text{PWMMD} + 1}{\text{PWM clock}}$$

$$\text{Leader pulse} = \frac{\text{PWMDx}}{\text{PWM clock}}$$

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19. KBI – Keyboard Interface

Keyboard interface (KBI) can be connected to an 8 x n matrix keyboard or any similar devices. It has 8 inputs with programmable interrupt capability on either high or low level. These 8 inputs are through P2 or P0 and can be the external interrupts to leave from the idle and stop modes. The 8 inputs are independent from each other but share the same interrupt vector 5Bh.

KBI	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
KBI function											
KBLS	KBI level selection	F1h	KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0	00H
KBE	KBI input enable	F2h	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0	00H
KBF	KBI flag	F3h	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0	00H
KBD	KBI De-bounce control register	F4h	KBDEN	-	-	-	-	-	KBD[1:0]		00H

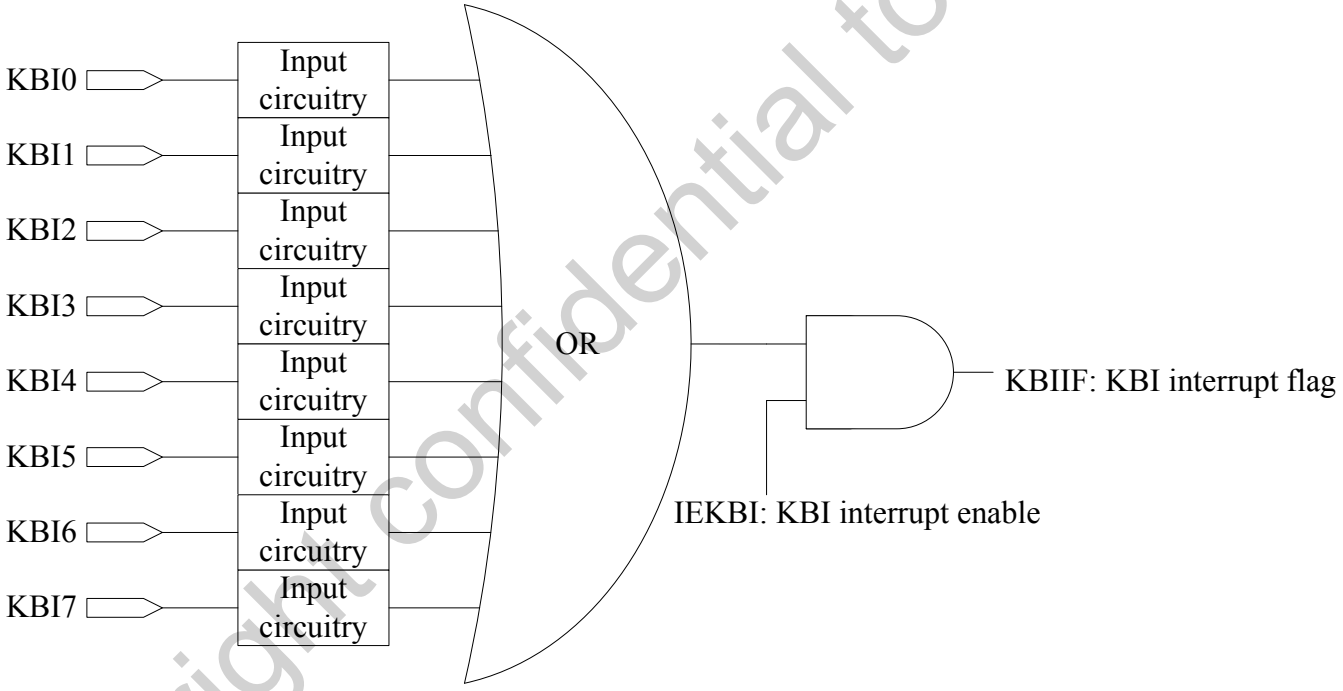

Figure 18- 1 keyboard interface block diagram

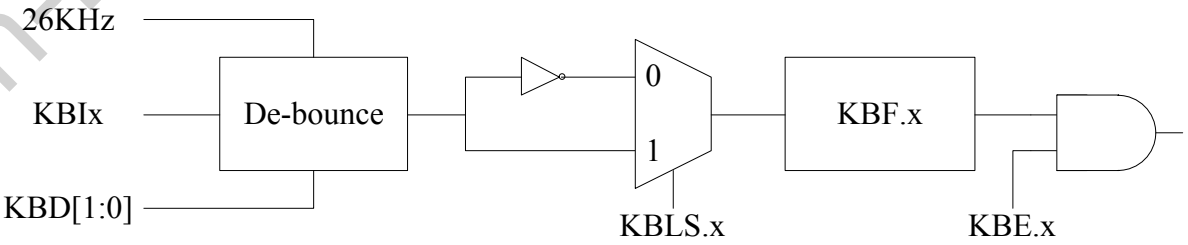

Figure 18-2 keyboard input circuitry

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Mnemonic: KBLS **Address: F1H**

7	6	5	4	3	2	1	0	Reset
KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0	00H

KBLS7: Keyboard line 7 level selection bit

Cleared to enable a low level detection on KBI7.

Set to enable a high level detection on KBI7.

KBLS6: Keyboard line 6 level selection bit

Cleared to enable a low level detection on KBI6.

Set to enable a high level detection on KBI6.

KBLS5: Keyboard line 5 level selection bit

Cleared to enable a low level detection on KBI5.

Set to enable a high level detection on KBI5.

KBLS4: Keyboard line 4 level selection bit

Cleared to enable a low level detection on KBI4.

Set to enable a high level detection on KBI4.

KBLS3: Keyboard line 3 level selection bit

Cleared to enable a low level detection on KBI3.

Set to enable a high level detection on KBI3.

KBLS2: Keyboard line 2 level selection bit

Cleared to enable a low level detection on KBI2.

Set to enable a high level detection on KBI2.

KBLS1: Keyboard line 1 level selection bit

Cleared to enable a low level detection on KBI1.

Set to enable a high level detection on KBI1.

KBLS0: Keyboard line 0 level selection bit

Cleared to enable a low level detection on KBI0.

Set to enable a high level detection on KBI0.

Mnemonic: KBE **Address: F2H**

7	6	5	4	3	2	1	0	Reset
KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0	00H

KBE7: Keyboard line 7 enable bit

Cleared to enable standard I/O pin.

Set to enable KBF7 bit in KBF register to generate an interrupt request.

KBE6: Keyboard line 6 enable bit

Cleared to enable standard I/O pin.

Set to enable KBF7 bit in KBF register to generate an interrupt request.

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KBE5: Keyboard line 5 enable bit

Cleared to enable standard I/O pin.

Set to enable KBF5 bit in KBF register to generate an interrupt request.

KBE4: Keyboard line 4 enable bit

Cleared to enable standard I/O pin.

Set to enable KBF4 bit in KBF register to generate an interrupt request.

KBE3: Keyboard line 3 enable bit

Cleared to enable standard I/O pin.

Set to enable KBF3 bit in KBF register to generate an interrupt request.

KBE2: Keyboard line 2 enable bit

Cleared to enable standard I/O pin.

Set to enable KBF2 bit in KBF register to generate an interrupt request.

KBE1: Keyboard line 1 enable bit

Cleared to enable standard I/O pin.

Set to enable KBF1 bit in KBF register to generate an interrupt request.

KBE0: Keyboard line 0 enable bit

Cleared to enable standard I/O pin.

Set to enable KBF0 bit in KBF register to generate an interrupt request.

Mnemonic: KBF **Address: F3H**

7	6	5	4	3	2	1	0	Reset
KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0	00H

KBF7: Keyboard line 7 flag

Set by hardware when the KBI7 detects a programmed level. It generates a keyboard interrupt request if the KBE7 in KBE register is set. Must be cleared by software.

KBF6: Keyboard line 6 flag

Set by hardware when the KBI6 detects a programmed level. It generates a keyboard interrupt request if the KBE6 in KBE register is set. Must be cleared by software.

KBF5: Keyboard line 5 flag

Set by hardware when the KBI5 detects a programmed level. It generates a keyboard interrupt request if the KBE5 in KBE register is set. Must be cleared by software.

KBF4: Keyboard line 4 flag

Set by hardware when the KBI4 detects a programmed level. It generates a keyboard interrupt request if the KBE4 in KBE register is set. Must be cleared by software.

KBF3: Keyboard line 3 flag

Set by hardware when the KBI3 detects a programmed level. It generates a keyboard interrupt request if the KBE3 in KBE register is set. Must be cleared by software.

KBF2: Keyboard line 2 flag

Set by hardware when the KBI2 detects a programmed level. It generates a keyboard

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interrupt request if the KBE2 in KBE register is set. Must be cleared by software.

KBF1: Keyboard line 1 flag

Set by hardware when the KBI1 detects a programmed level. It generates a keyboard interrupt request if the KBE1 in KBE register is set. Must be cleared by software.

KBF0: Keyboard line 0 flag

Set by hardware when the KBI0 detects a programmed level. It generates a keyboard interrupt request if the KBE0 in KBE register is set. Must be cleared by software.

Mnemonic: KBD **Address:F4H**

7	6	5	4	3	2	1	0	Reset
KBDEN	-	-	-	-	-	KBD[1:0]		00H

KBDEN: Enable KBI de-bounce function. The default KBI function is enabled.

KBDEN = 0, enable KBI de-bounce function. The de-bounce time is selected by KBD [1:0].

KBDEN = 1, disable KBI de-bounce function. The KBI input pin without de-bounce mechanism.

KBD[1:0]: Select KBI de-bounce time. If KBDEN = “0”, the default de-bounce time is 320 ms.

KBD[1:0] = 00, the de-bounce time is 320 ms.

KBD[1:0] = 01, the de-bounce time is 160 ms.

KBD[1:0] = 10, the de-bounce time is 80 ms.

KBD[1:0] = 11, the de-bounce time is 40 ms.

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20. In-System Programming (Internal ISP)

The OB39R32T2 can generate flash control signal by internal hardware circuit. Users utilize flash control register, flash address register and flash data register to perform the ISP function without removing the OB39R32T2 from the system.

The OB39R32T2 provides internal flash control signals which can do flash program/chip erase/page erase/protect functions. User need to design and use any kind of interface which OB39R32T2 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

20.1 ISP service program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the OB39R32T2 for the ISP purpose.

The ISP service programs were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between OB39R32T2 and host device which output data to the OB39R32T2. For example, if user utilize UART interface to receive/Transmit data between OB39R32T2 and host device, the ISP service program should include baud rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.

The ISP service program can be initiated under OB39R32T2 active or idle mode. It can not be initiated under power down mode.

20.2 Lock Bit (N)

The Lock Bit N has two functions: one is for service program size configuration and the other is to lock the ISP service program space from flash erase function.

The ISP service program space address range $D800 to $F7FF. It can be divided as blocks of N*1K byte. (N=0 to 8). When N=0 means no ISP function. When N=1 means ISP service program occupies 1K byte. The maximum ISP service program allowed is 8K byte when N=8.

After N determined, OB39R32T2 will reserve the ISP service program space downward from the top of the program address $F7FF. Please see section 3.1 program memory diagram for this ISP service program space structure.

The lock bit N function is different from the flash protect function. The flash erase function can erase all of the flash memory except for the locked ISP service program space. If the flash not has been protected, the content of ISP service program still can be read. If the flash has been protected, the overall content of flash program memory space including ISP service program space can not be read. As given in Table 19-1.

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Table 19-1 ISP code area

N	ISP service program address
0	No ISP service program
1	1K bytes ($F400h ~ $F7FFh)
2	2K bytes ($F000h ~ $F7FFh)
3	3K bytes ($EC00h ~ $F7FFh)
4	4K bytes ($E800h ~ $F7FFh)
5	5K bytes ($E400h ~ $F7FFh)
6	6K bytes ($E000h ~ $F7FFh)
7	7K bytes ($DC00h ~ $F7FFh)
8	8K bytes ($D800h ~ $F7FFh)

ISP service program configurable in N*1K byte (N= 0 ~ 8)

20.3 Program the ISP Service Program

After Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If user needs to erase the locked ISP service program, he can do it by writer only. User can not change ISP service program when OB39R32T2 was in system.

20.4 Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are four ways to do so:

(1) Blank reset. Power on reset with first flash address blank ($0000=#FFH) will load the PC with start address of ISP service program.

(2) Execute jump instruction can load the start address of the ISP service program to PC.

(3) Enter's ISP service program by hardware setting. User can force OB39R32T2 enter ISP service program by setting P0.2, P0.3 "active low" or P0.4 " active low" during power on reset period. In application system design, user should take care of the setting of P0.2, P0.3 or P0.4 at reset period to prevent OB39R32T2 from entering ISP service program.

(4) Enter's ISP service program by hardware setting, the P2.0(RXD0) or P1.1(RXD1) will be detected the two clock signals during power on reset period.

During the strobe window, the hardware will detect the status of P0.2, P0.3 or P0.4. If they meet one of above conditions, chip will switch to ISP mode automatically.

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There are 5 kinds of entry mechanisms for user different applications. This entry method will select on the writer or ISP.

(1) First Address Blank. i.e. $0000 = 0xFF. And triggered by Internal reset signal. (Entry mechanism 1)
(2) P0.2 = 0 & P0.3 = 0. And triggered by Internal reset signal. (Entry mechanism 2)
(3) P0.4 = 0. And triggered by Internal reset signal. (Entry mechanism 3)
(4) P2.0 input 2 clocks. And triggered by Internal reset signal. (Entry mechanism 4)
(5) P1.1 input 2 clocks. And triggered by Internal reset signal. (Entry mechanism 5)

20.5 ISP register – TAKEY, IFCON, ISPFAH, ISPFAL, ISPFD and ISPFC

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
ISP function											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
IFCON	Interface Control register	8Fh	-	CDPR	-	-	-	-	-	ISPE	00H
ISPFAH	ISP Flash Address – High register	E1h	ISPFAH [7:0]								FFH
ISPFAL	ISP Flash Address - Low register	E2h	ISPFAL [7:0]								FFH
ISPFD	ISP Flash Data register	E3h	ISPFD [7:0]								FFH
ISPFC	ISP Flash Control register	E4h	EMF1	EMF2	EMF3	EMF4	EMF5	ISPF[2:0]			00H

Mnemonic: TAKEY **Address: F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

ISP enable bit (ISPE) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the ISPE bit write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

Mnemonic: IFCON **Address: 8FH**

7	6	5	4	3	2	1	0	Reset
-	CDPR	-	-	-	-	-	ISPE	00H

The bit 0 (ISPE) of IFCON is ISP enable bit. User can enable overall OB39R32T2 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0. The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally. ISP registers ISPFAH, ISPFAL, ISPFD and ISPFC are read-only by default. Software must be set ISPE bit to 1 to enable these 4 registers write attribute.

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Mnemonic: ISPFAH **Address: E1H**

7	6	5	4	3	2	1	0	Reset
ISPFAH[7:0]								FFH

ISPFAH [7:0]: Flash address-high for ISP function

Mnemonic: ISPFAL **Address: E2H**

7	6	5	4	3	2	1	0	Reset
ISPFAL[7:0]								FFH

ISPFAL [7:0]: Flash address-Low for ISP function

The ISPFAH & ISPFAL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

Mnemonic: ISPFD **Address: E3H**

7	6	5	4	3	2	1	0	Reset
ISPFD[7:0]								FFH

ISPFD [7:0]: Flash data for ISP function.

The ISPFD provide the 8-bit data register for ISP function.

Mnemonic: ISPFC **Address: E4H**

7	6	5	4	3	2	1	0	Reset
EMF1	EMF2	EMF3	EMF4	EMF5	ISPF[2:0]			00H

EMF1: Entry mechanism (1) flag, clear by reset. (Read only)

EMF2: Entry mechanism (2) flag, clear by reset. (Read only)

EMF3: Entry mechanism (3) flag, clear by reset. (Read only)

EMF4: Entry mechanism (4) flag, clear by reset. (Read only)

EMF5: Entry mechanism (5) flag, clear by reset. (Read only)

ISPF [2:0]: ISP function select bit.

ISPF[2:0]	ISP function
000	Byte program
001	Chip protect
010	Page erase
011	Chip erase
100	Write option
101	Read option
110	Erase option
111	Finish flag

One page of flash memory is 1K byte

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The choice ISP function will start to execute once the software write data to ISPFC register.

To perform byte program/page erases ISP function, user need to specify flash address at first. When performing page erase function, OB39R32T2 will erase entire page which flash address indicated by ISPFAH & ISPFAL registers located within the page.

e.g. flash address: $ X000

page erase function will erase from $X000 to $X3FF

To perform the chip erase ISP function, OB39R32T2 will erase all the flash program memory except the ISP service program space. To perform chip protect ISP function, the OB39R32T2 flash memory content will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah    ; enable ISPE write attribute
ORL IFCON, #01H    ; enable OB39R32T2 ISP function
MOV ISPFAH, #10H   ; set flash address-high, 10H
MOV ISPFAL, #05H   ; set flash address-low, 05H
MOV ISPFD, #22H    ; set flash data to be programmed, data = 22H
MOV ISPFC, #00H    ; start to program #22H to the flash address $1005H
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah    ; enable ISPE write attribute
ANL IFCON, #0FEH   ; disable OB39R32T2 ISP function
```

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Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VDD	Supply voltage	2.2	-	5.5	V	

DC Characteristics

TA = -40℃ to 85℃, VCC =2.2~ 5.5V

Symbol	Parameter	Valid	Min	Typical	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0,1,2,3			0.2Vcc	V	
VIL2	Input Low-voltage	XT32KI			0.2Vcc	V	-
VIH1	Input High-voltage	Port 0,1,2,3	0.8Vcc			V	-
VIH2	Input High-voltage	XT32KI	0.8Vcc			V	-
Vhys	Hysteresis voltage	Port 0,1,2,3		0.2		V	VCC=5V
Vhys	Hysteresis voltage	IIC0		0.4		V	VCC=5V
Vhys	Hysteresis voltage	IIC1		0.6		V	VCC=5V
IOL	Sink Current	Port 0,1,2,3	40			mA	VOL=0.45V VCC=5V
			25			mA	VOL=0.45V VCC=3V
IOL1	Sink Current	COM0~COM6	88			mA	VOL=0.45V VCC=5V
			65			mA	VOL=0.45V VCC=3V
IOH	Source Current (Pull-Up)	Port 0,1,2,3	0.36			mA	VOH=2.6V VCC=5V
			0.07			mA	VOH=2.4V VCC=3V
IOH1	Source Current (Push-Pull)	Port 0,1,2,3	20			mA	VOH=4.5V VCC=5V
			10			mA	VOH=2.6V VCC=3V
IOH2	Source Current (Push-Pull)	COM0~COM6	88			mA	VOH=4.5V VCC=5V
			65			mA	VOH=2.6V VCC=3V
CIO	Pin Capacitance	-	-	-	10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	2.2V~5V	-	4	5	mA	Active mode, IRC=22.1184MHz 25 ℃
			-	2.3	2.6	mA	Idle mode, IRC=22.1184MHz 25 ℃
			-	3	7	uA	Power down mode 25 ℃

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ADC Characteristics

	Symbol	Test Condition	MIN	TYP	MAX	Unit
Operation	VDD	VDD	3		5.5	V
Resolution					12	bit
Conversion time				$16t_{ADC}$		us
Sample rate				230k		Hz
Integral Non-Linearity Error	INL		-2		2	LSB
Differential Non-Linearity	DNL		-1		1	LSB
Clock frequency	ADCCLK				4	MHz

LVI& LVR Characteristics

VCC	LVR		
	Min	Typical	Max
2.2V ~ 5.5V	VIL=1.45V	VIL=1.55V	VIL=1.65V
3V ~ 5.5V	VIL=2.5V	VIL=2.7V	VIL=2.9V

VCC	LVI		
	Min	Typical	Max
LVIS[1:0] = 00	VIL=1.71V	VIL=1.80V	VIL=1.89V
LVIS[1:0] = 01	VIL=2.66V	VIL=2.80V	VIL=2.94V
LVIS[1:0] = 10	VIL=3.135V	VIL=3.30V	VIL=3.465V
LVIS[1:0] = 11	VIL=3.80V	VIL=4.00V	VIL=4.20V

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