HARRIS SEMICONDUCTOR

CD74FCT521T

December 1996

Fast CMOS 8-Bit Identity Comparator

Features

- **Advanced 0.8 micron CMOS Technology**
- **CD74FCT521T is Pin Compatible with Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

The CD74FCT521T is an 8-bit identity comparator. When two words of up to eight bits are compared, a bit-for-bit match of the two words provides a LOW output. The comparison can be extended over multiple words by the expansion input. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Ordering Information

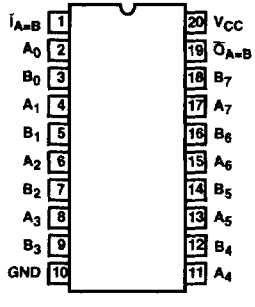
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT521ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521BTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521BTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521TQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT521T
(QSOP, SOIC)
TOP VIEW



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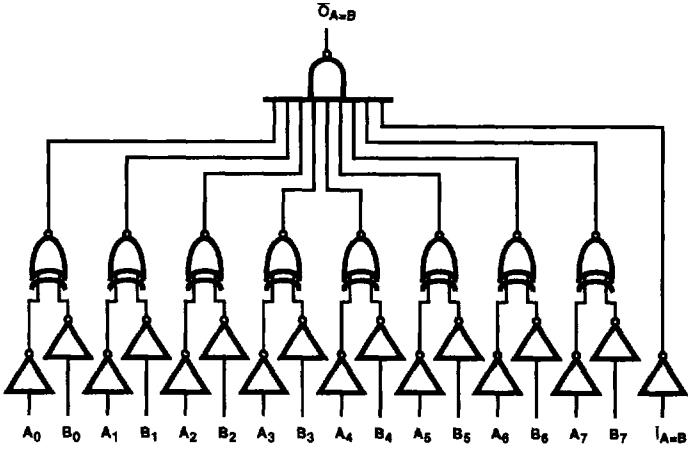
OCTAL 5V FCT
5V FCT 25Ω

Functional Block Diagram



TRUTH TABLE

(NOTE 1) INPUTS		(NOTE 1) OUTPUTS
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B (Note 2)	L
L	A ≠ B	H
H	A = B (Note 2)	H
H	A ≠ B	H

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)
A_0 - A_7	Word A Inputs
B_0 - B_7	Word B Inputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 8)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 9)	I_{CCD}	V_{CC} = Max, Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 11)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 10)	mA

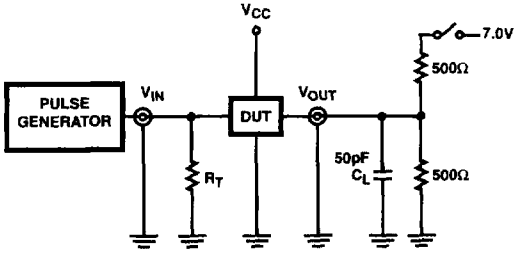
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T (NOTE 13) MIN	T MAX	AT (NOTE 13) MIN	AT MAX	BT (NOTE 13) MIN	BT MAX	CT (NOTE 13) MIN	CT MAX	DT (NOTE 13) MIN	DT MAX	UNITS
Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	10.0	1.5	7.2	1.5	5.5	1.5	4.5	1.5	4.2	ns
Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	t_{PLH}, t_{PHL}		1.5	9.0	1.5	6.0	1.5	4.6	1.5	4.1	1.5	3.8	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. *Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.*
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
12. *See test circuit and wave forms.*
13. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

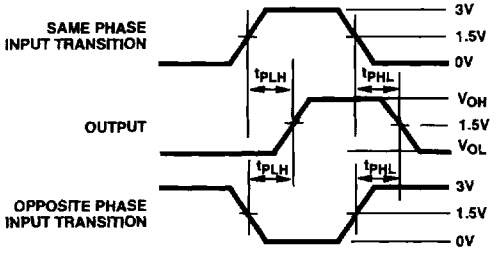


FIGURE 2. PROPAGATION DELAY