HI-200, HI-201

August 1997

Dual/Quad SPST, CMOS Analog Switches

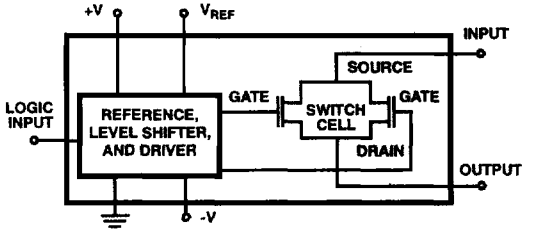
Features

- Analog Voltage Range ..... ±15V
- Analog Current Range 80mA
- Turn-On Time 240ns
- Low r_{ON} 55Ω
- Low Power Dissipation 15mW
- TTL/CMOS Compatible

Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks

Functional Diagram



Description

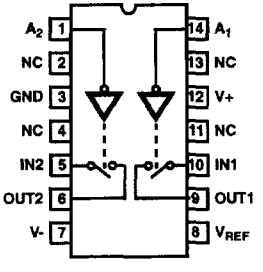
HI-200/HI-201 are monolithic devices comprising independently selectable SPST switches which feature fast switching speeds (HI-200 240ns, and HI-201 185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltage up to the supply rails and for signal current up to 80mA. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200/HI-201 are ideal components for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and operational amplifier gain switching networks.

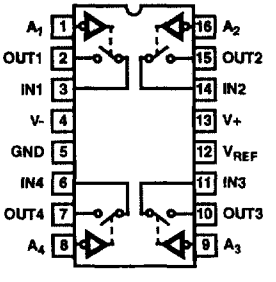
HI-200 is a dual SPST CMOS analog switch available in DIP and (TO-99) metal cans and is pin compatible with other available "200 series" switches. For MIL-STD-883 compliant parts, request the HI-200/883 data sheet.

Pinouts

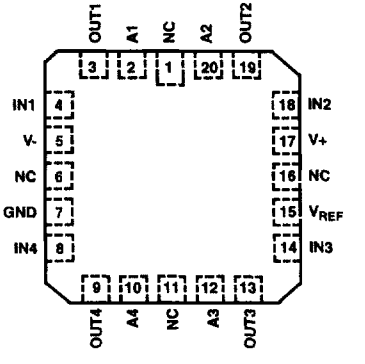
HI-200 (CERDIP, PDIP, SOIC)
TOP VIEW



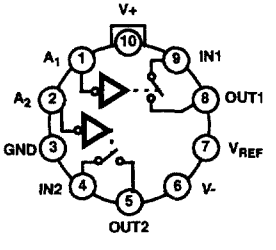
HI-201 (CERDIP, PDIP, SOIC)
TOP VIEW



HI-201 (PLCC, CLCC)
TOP VIEW



HI-200 (METAL CAN)
TOP VIEW



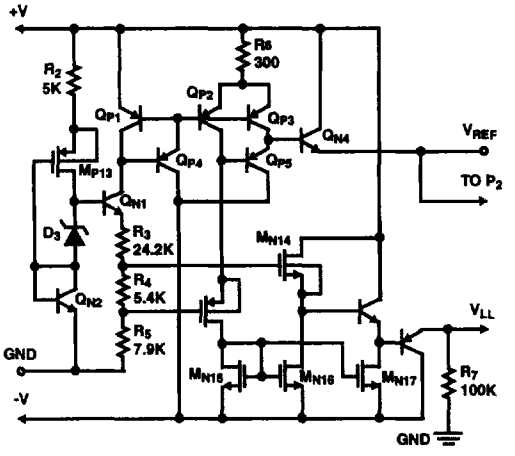
File Number **3121.2**

Ordering Information

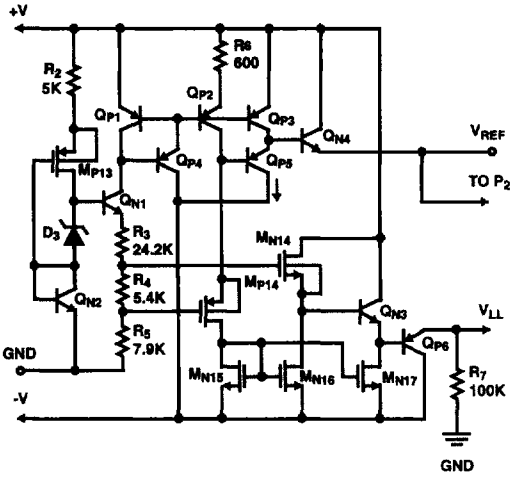
PART NUMBER	TEMPERATURE RANGE (°C)	PACKAGE	PKG. NO.
HI2-0200-5	0 to 75	10 Pin Metal Can	T10.B
HI1-0200-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0200-4	-25 to 85	10 Pin Metal Can	T10.B
HI3-0200-5	0 to 75	14 Ld PDIP	E14.3
HI1-0200-7	0 to 75 + 96 Hr. Burn-In	14 Ld CERDIP	F14.3
HI1-0200-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0200-4	-25 to 85	14 Ld CERDIP	F14.3
HI2-0200-2	-55 to 125	10 Pin Metal Can	T10.B
HI9P0200-5	0 to 75	14 Ld SOIC	M14.15
HI1-0200/883	-55 to 125	14 Ld CERDIP	F14.3
HI2-0200/883	-55 to 125	10 Pin Metal Can	T10.B
HI1-0201-7	0 to 75 + 96 Hr. Burn-In	16 Ld CERDIP	F16.3
HI1-0201-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0201-4	-25 to 85	16 Ld CERDIP	F16.3
HI4P0201-5	0 to 75	20 Ld PLCC	N20.35
HI9P0201-5	0 to 75	16 Ld SOIC	M16.15
HI9P0201-9	-40 to 85	16 Ld SOIC	M16.15
HI1-0201-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-0201-5	0 to 75	16 Ld PDIP	E16.3
HI1-0201/883	-55 to 125	16 Ld CERDIP	F16.3
HI4-0201/883	-55 to 125	20 Ld CLCC	J20.A

Schematic Diagrams

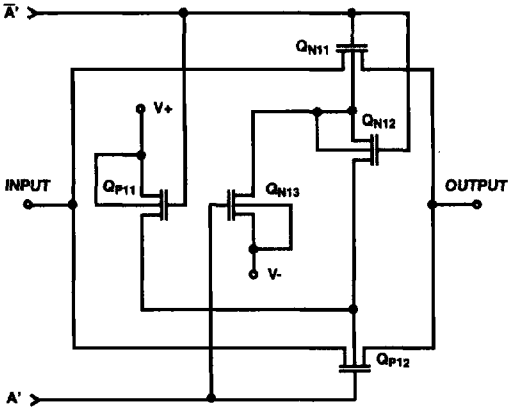
TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL
HI-200



TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL
HI-201

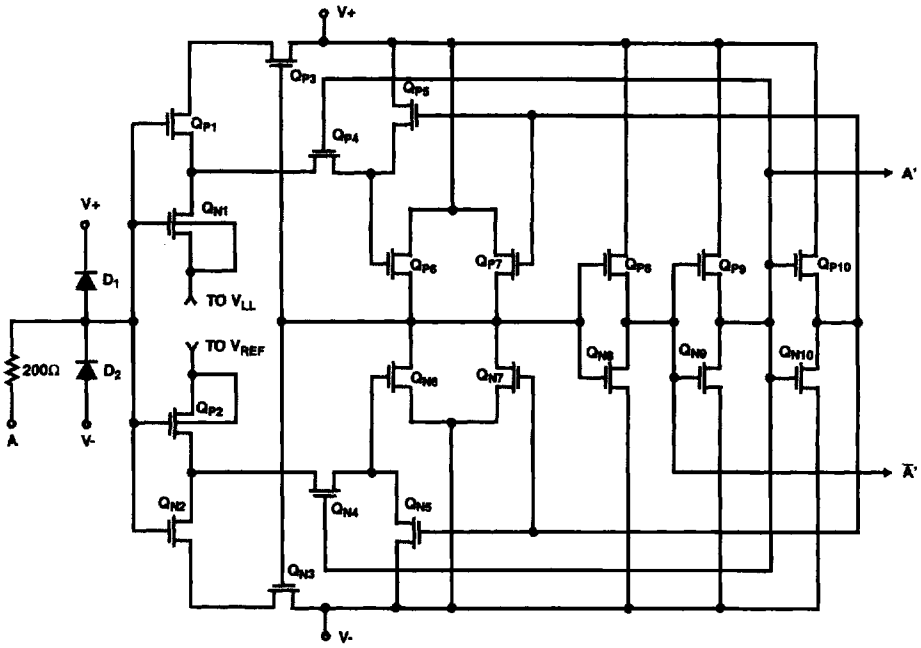


SWITCH CELL



Schematic Diagrams (Continued)

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Supply Voltage ..... 44V (±22)
V_{REF} to Ground ..... 20V, -5V
Digital Input Voltage ..... $+V_{SUPPLY}$ 4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) ..... $+V_{SUPPLY}$ 2.0V
$-V_{SUPPLY}$ -2.0V

Operating Conditions

Temperature Ranges
HI-200-2, HI-201-2 ..... -55°C to 125°C
HI-200-4, HI-201-4 ..... -25°C to 85°C
HI-200-5, HI-201-5 ..... 0°C to 75°C
HI200-9, HI201-9 ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld CERDIP Package (/883 Versions)	80	24
14 Ld CERDIP Package (Non /883 Versions)	95	40
16 Ld CERDIP Package (/883 Versions)	75	20
16 Ld CERDIP Package (Non /883 Versions)	90	35
PLCC Package	80	N/A
PDIP Package	100	N/A
14 Ld SOIC Package	120	N/A
16 Ld SOIC Package	115	N/A
10 Pin Metal Can Package (HI-200 Only)	160	75
20 Ld CLCC Package (HI-201 Only)	65	13

Maximum Storage Temperature ..... -65°C to 150°C
Maximum Junction Temperature (Hermetic) ..... 175°C
Maximum Junction Temperature (Plastic) ..... 150°C
Maximum Lead Temperature (Soldering, 10s) ..... 300°C
(PLCC and SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics

Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-200, HI-201-2/883			HI-200, HI201 -4, -5, -7, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Switch On Time, t_{ON}									
HI-200		25	-	240	500	-	240	-	ns
HI-201		25	-	185	500	-	185	-	ns
		Full	-	1000	-	-	1000	-	ns
Switch Off Time, t_{OFF}									
HI-200		25	-	330	500	-	500	-	ns
HI-201		25	-	220	500	-	220	-	ns
		Full	-	1000	-	-	1000	-	ns
"Off Isolation"	(Note 4)								
HI-200		25	-	70	-	-	70	-	dB
HI-201		25	-	80	-	-	80	-	dB
Input Switch Capacitance, $C_{S(OFF)}$		25	-	5.5	-	-	5.5	-	pF
Output Switch Capacitance, $C_{D(OFF)}$		25	-	5.5	-	-	5.5	-	pF
Output Switch Capacitance, $C_{D(ON)}$		25	-	11	-	-	11	-	pF
Digital Input Capacitance, C_A		25	-	5	-	-	5	-	pF
Drain-to-Source Capacitance, $C_{DS(OFF)}$		25	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH}		Full	2.4	-	-	2.4	-	-	V
Input Leakage Current (High or Low), I_A	(Note 2)	Full	-	-	1.0	-	-	1.0	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	(Note 1)	25	-	55	70	-	55	80	Ω
		Full	-	80	100	-	72	100	Ω

Electrical Characteristics Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-200, HI-201-2/883			HI-200, HI201 -4, -5, -7, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Off Input Leakage Current, $I_{S(OFF)}$	(Note 6)	25	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
Off Output Leakage Current, $I_{D(OFF)}$	(Note 6)	25	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
On Leakage Current, $I_{D(ON)}$	(Note 6)	25	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
$I_{S(OFF)}$		25	-	2	5	-	2	50	nA
HI-201		Full	-	-	500	-	-	250	nA
$I_{D(OFF)}$		25	-	2	5	-	2	50	nA
HI-201		Full	-	35	500	-	35	250	nA
$I_{D(ON)}$		25	-	2	5	-	2	50	nA
HI-201		Full	-	-	500	-	-	250	nA
POWER REQUIREMENTS (Note 5)									
Power Dissipation, P_D		25	-	15	-	-	15	-	mW
		Full	-	-	60	-	-	60	mW
Current, I+		25	-	0.5	-	-	0.5	-	mA
		Full	-	-	2.0	-	-	2.0	mA
Current, I-		25	-	0.5	-	-	0.5	-	mA
		Full	-	-	2.0	-	-	2.0	mA

NOTES:

2. V_{OUT} = ±10V, I_{OUT} = 1mA.
3. Digital Inputs are MOS gates: typical leakage is < 1nA.
4. V_{AH} = 4V.
5. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = $3V_{RMS}$, f = 100kHz.
6. V_A = +3V or V_A = 0V for Both Switches.
7. Refer to Leakage Current Measurements (Figure 4).

Performance Curves and Test Circuits T_A = 25°C, V_{SUPPLY} = 15V, V_{AH} = 2.4V, V_{AL} = 0.8V and V_{REF} = Open

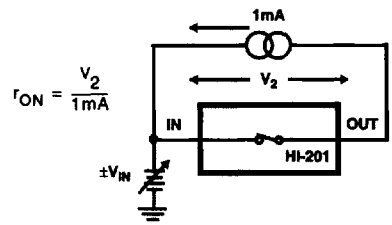


FIGURE 1. ON RESISTANCE vs ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE

Performance Curves and Test Circuits $T_A = 25°C$, $V_{SUPPLY} = 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$ and V_{REF} = Open (Continued)

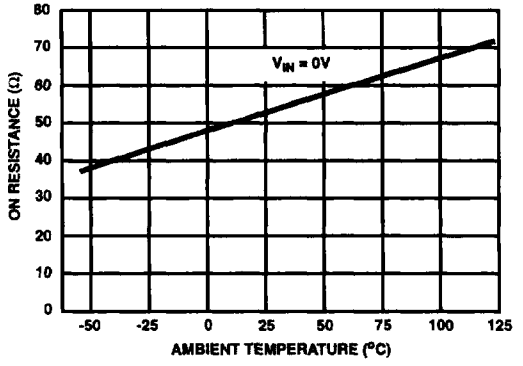


FIGURE 2. ON RESISTANCE vs TEMPERATURE

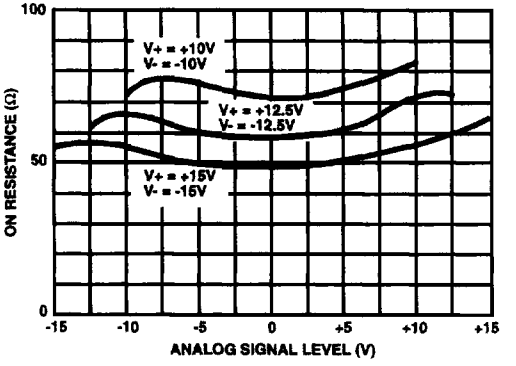


FIGURE 3. HI-201 ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

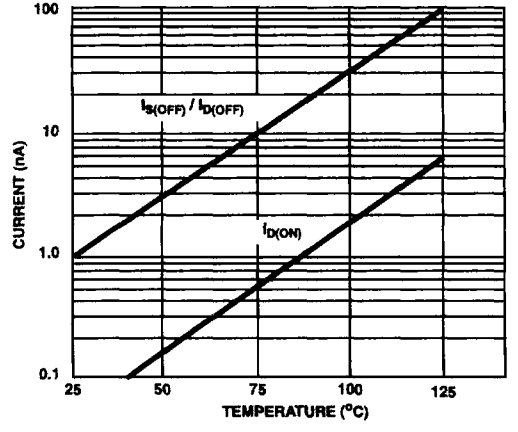


FIGURE 4A. HI-201 SWITCH LEAKAGE CURRENT vs TEMPERATURE

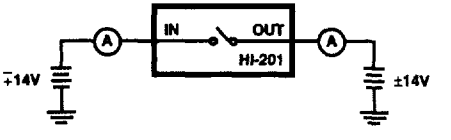


FIGURE 4B. OFF LEAKAGE CURRENT vs TEMPERATURE

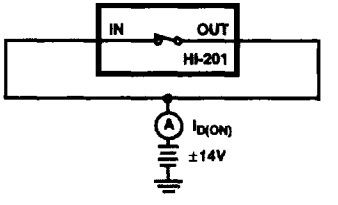


FIGURE 4C. ON LEAKAGE CURRENT vs TEMPERATURE

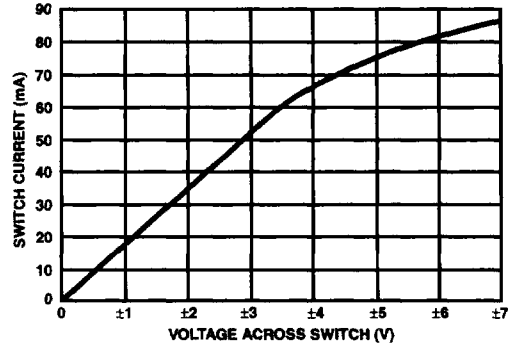


FIGURE 5A.

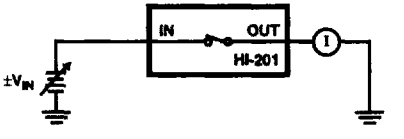


FIGURE 5B.

FIGURE 5. SWITCH CURRENT vs VOLTAGE

Switching Waveforms

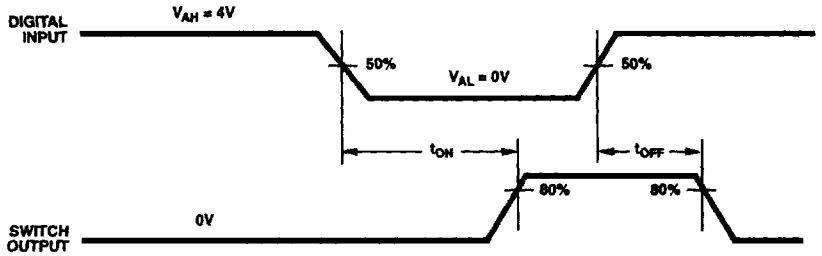
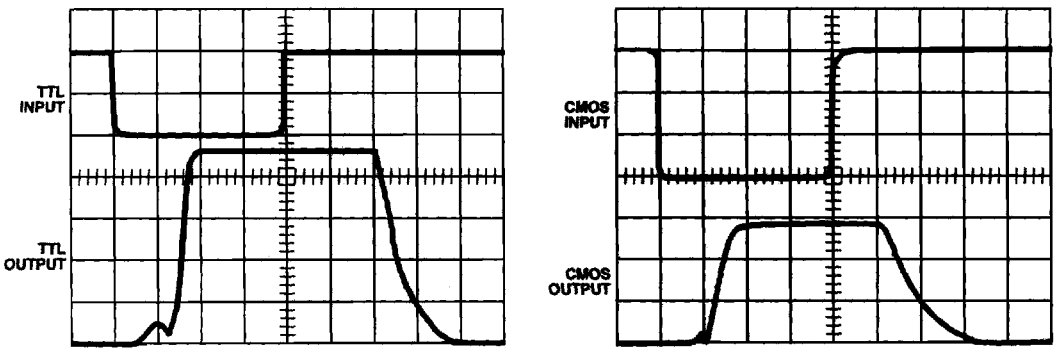


FIGURE 6. LOGIC "0" = SWITCH ON



t_{ON}, t_{OFF} (TTL INPUT), V_{IN} = +4V
Vertical: 2V/Div.
Horizontal: 100ns/Div.

t_{ON}, t_{OFF} (TTL INPUT), V_{IN} = +15V
Vertical: 5V/Div.
Horizontal: 100ns/Div.

FIGURE 7. TTL INPUT

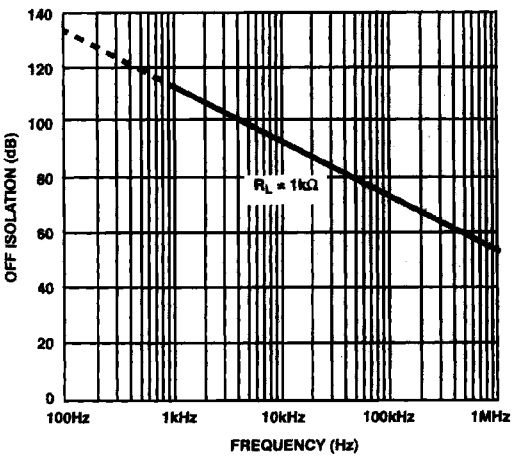


FIGURE 8. OFF ISOLATION vs FREQUENCY

For more information see Application Notes AN520, AN521, AN531, AN532 and AN557.

Single Supply

The switch operation of the HI-200/201 is dependent upon an internally generated switching threshold voltage optimized for ±15V power supplies. The HI-200/201 does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels (±15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

For further information see Application Notes AN520, AN521, AN531, AN532, AN543 and AN557.

Die Characteristics

DIE DIMENSIONS:

54 mils x 79 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION:

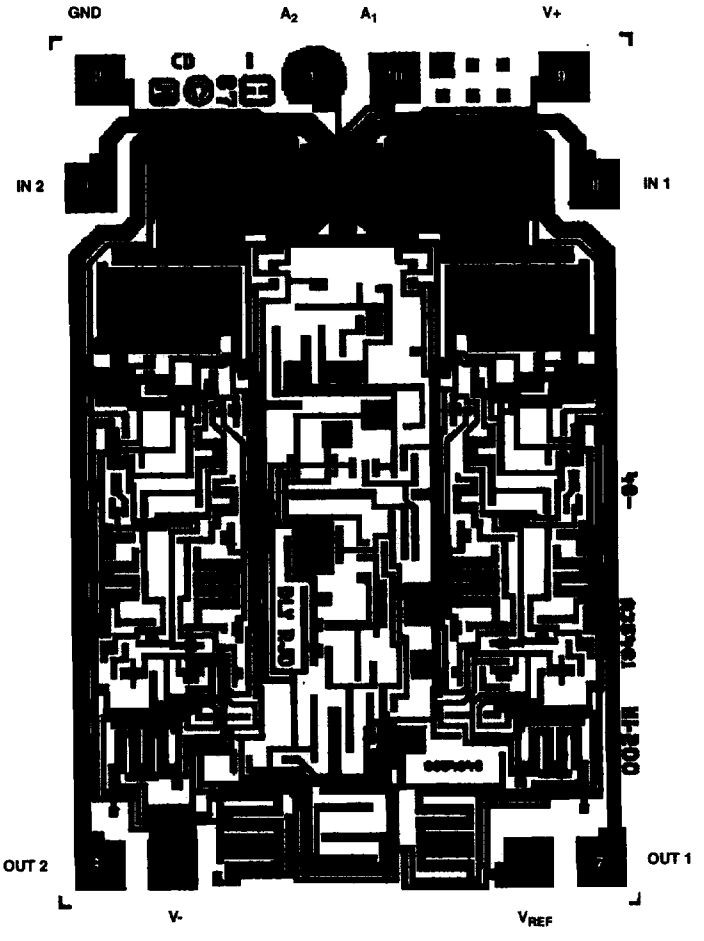
Type: Nitride over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

2×10^5 A/cm^2 at 25mA

Metallization Mask Layout

HI-200



Die Characteristics

DIE DIMENSIONS:

81 mils x 85 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

2×10^5 A/cm^2 at 25mA

Metallization Mask Layout

HI-201