

8-Channel/Differential 4-Channel, CMOS High Speed Analog Multiplexer

August 1997

Features

- Access Time (Typical) 130ns
- Settling Time 250ns (0.1%)
- Low Leakage (Typical)
 - $I_{S(OFF)}$ 10pA
 - $I_{D(OFF)}$ 15pA
- Low Capacitance (Max)
 - $C_{S(OFF)}$ 5pF
 - $C_{D(OFF)}$ 10pF
- Off Isolation at 500kHz 45dB (Min)
- Low Charge Injection Error 25mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

Description

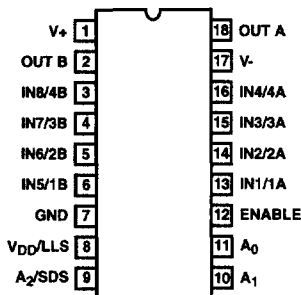
The HI-518 is a monolithic, dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518 to be user programmed either as a single ended 8-Channel multiplexer by connecting 'Out A' to 'Out B' and using A_2 as a digital address input, or as a 4-Channel differential multiplexer by connecting A_2 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current ($I_{DOFF} < 100pA$ at 25°C) and fast settling ($t_{SETTLE} = 800ns$ to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

Ordering Information

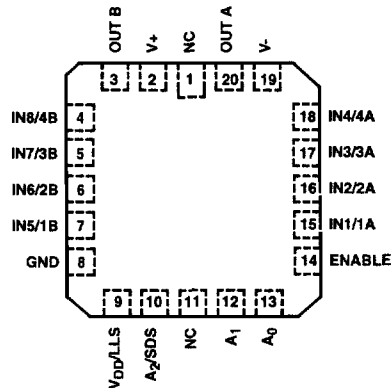
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------|------------------|--------------|----------|
| HI3-0518-5 | 0 to 75 | 18 Ld PDIP | E18.3 |
| HI1-0518-5 | 0 to 75 | 18 Ld CERDIP | F18.3 |
| HI1-0518-2 | -55 to 125 | 18 Ld CERDIP | F18.3 |
| HI1-0518-8 | -55 to 125 | 18 Ld CERDIP | F18.3 |
| HI4P0518-5 | 0 to 75 | 20 Ld PLCC | N20.35 |
| HI4-0518-8 | -55 to 125 | 20 Ld CLCC | J20.A |

Pinouts

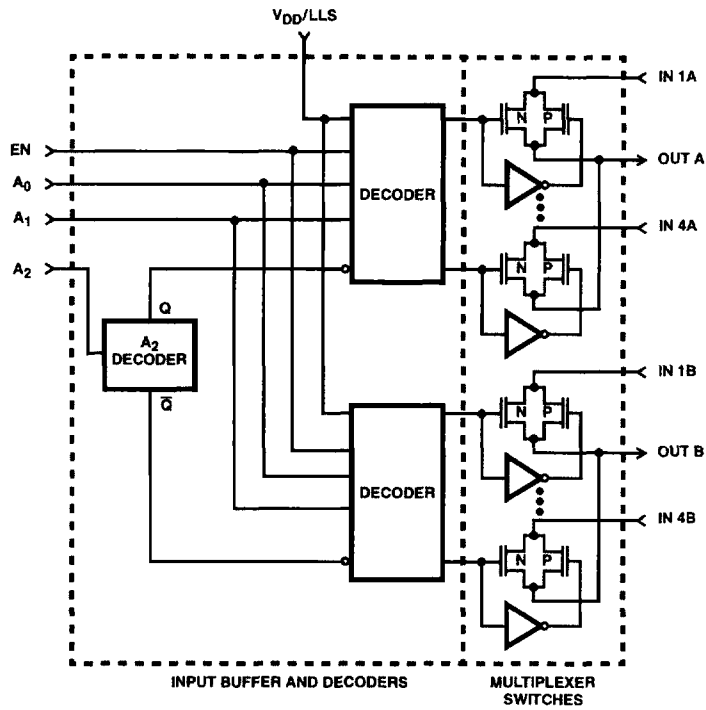
HI-518 (CERDIP, PDIP)
TOP VIEW



HI-518 (CLCC, PLCC)
TOP VIEW



Functional Block Diagram



| A ₂ DECODE | | |
|-----------------------|---|-----------|
| A ₂ | Q | \bar{Q} |
| H | H | L |
| L | L | H |
| V- | L | L |

Absolute Maximum Ratings (Note 1)

| | |
|--|----------|
| V+ to V- | 33V |
| Analog Input Voltage | |
| +V _{IN} | (V+) +2V |
| -V _{IN} | (V-) -2V |
| Digital Input Voltage | |
| TTL Levels Selected (V _{DD} /LLS Pin = GND or Open) | |
| +V _A | +6V |
| -V _A | -6V |
| +A ₂ /SDS | (V+) +2V |
| -A ₂ /SDS | (V-) -2V |
| CMOS Levels Selected (V _{DD} /LLS Pin = V _{DD}) | |
| +V _A | (V+) +2V |
| -V _A | -2V |

Thermal Information

| | | |
|--|-------------------------------|----------------------|
| Thermal Resistance (Typical, Note 1) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| PDIP Package | 90 | N/A |
| PLCC Package | 80 | N/A |
| CERDIP Package | 70 | 18 |
| CLCC Package | 65 | 14 |
| Maximum Junction Temperature | | |
| CERDIP, CLCC Packages | 175°C | |
| PDIP, PLCC, SOIC Packages | 150°C | |
| Maximum Storage Temperature Range | -65°C to 150°C | |
| Maximum Lead Temperature (Soldering 10s) | 300°C (PLCC - Lead Tips Only) | |

Operating Conditions

Temperature Ranges

| | |
|-------------|----------------|
| HI-518-2,-8 | -55°C to 125°C |
| HI-518-5 | 0°C to 75°C |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND (Note 1), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | HI-518-2, -8 | | | HI-518-5 | | | UNITS |
|---|-----------------|-----------|--------------------|------|--------------------|--------------------|------|--------------------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SWITCHING CHARACTERISTICS | | | | | | | | | |
| Access Time, t _A | | 25 | - | 130 | 175 | - | 130 | 175 | ns |
| | | Full | - | - | 225 | - | - | 225 | ns |
| Break-Before-Make Delay, t _{OPEN} | | 25 | 10 | 20 | - | 10 | 20 | - | ns |
| Enable Delay (ON), t _{ON(EN)} | | 25 | - | 120 | 175 | - | 120 | 175 | ns |
| Enable Delay (OFF), t _{OFF(EN)} | | 25 | - | 140 | 175 | - | 140 | 175 | ns |
| Settling Time | | | | | | | | | |
| | 0.1% | 25 | - | 250 | - | - | 250 | - | ns |
| 0.01% | 25 | - | 800 | - | - | 800 | - | ns | |
| Charge Injection Error | Note 4 | 25 | - | - | 25 | - | - | 25 | mV |
| Off Isolation | Note 5 | 25 | 45 | - | - | 45 | - | - | dB |
| Channel Input Capacitance, C _{S(OFF)} | | 25 | - | - | 5 | - | - | 5 | pF |
| Channel Output Capacitance, C _{D(OFF)} | | 25 | - | - | 10 | - | - | 10 | pF |
| Digital Input Capacitance, C _A | | 25 | - | - | 5 | - | - | 5 | pF |
| Input to Output Capacitance, C _{DS(OFF)} | | 25 | - | 0.02 | | - | 0.02 | - | pF |
| DIGITAL INPUT CHARACTERISTICS | | | | | | | | | |
| Input Low Threshold, V _{AL} (TTL) | | Full | - | - | 0.8 | - | - | 0.8 | V |
| Input High Threshold, V _{AH} (TTL) | | Full | 2.4 | - | - | 2.4 | - | - | V |
| Input Low Threshold, V _{AL} (CMOS) | | Full | - | - | 0.3V _{DD} | - | - | 0.3V _{DD} | V |
| Input High Threshold, V _{AH} (CMOS) | | Full | 0.7V _{DD} | - | - | 0.7V _{DD} | - | - | V |

HI-518

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; $V_{DD}/LLS = GND$ (Note 1), Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | HI-518-2, -8 | | | HI-518-5 | | | UNITS |
|--|-----------------|-----------|--------------|-------|-------|----------|-------|-------|----------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input Leakage Current, I_{AH} (High) | | Full | - | - | 1 | - | - | 1 | μA |
| Input Leakage Current, I_{AL} (Low) | | Full | - | - | 20 | - | - | 20 | μA |
| ANALOG CHANNEL CHARACTERISTICS | | | | | | | | | |
| Analog Signal Range, V_{IN} | Note 2 | Full | -14 | | +14 | -15 | - | +15 | V |
| On Resistance, r_{ON} | Note 3 | 25 | - | 480 | 750 | - | 480 | 750 | Ω |
| | | Full | - | - | 1,000 | - | - | 1,000 | Ω |
| Off Input Leakage Current, $I_{S(OFF)}$ | | 25 | - | 0.01 | - | - | 0.01 | - | nA |
| | | Full | - | - | 50 | - | - | 50 | nA |
| Off Output Leakage Current, $I_{D(OFF)}$ | | 25 | - | 0.015 | - | - | 0.015 | - | nA |
| | | Full | - | - | 50 | - | - | 50 | nA |
| On Channel Leakage Current, $I_{D(ON)}$ | | 25 | - | 0.015 | - | - | 0.015 | - | nA |
| | | Full | - | - | 50 | - | - | 50 | nA |
| POWER SUPPLY CHARACTERISTICS | | | | | | | | | |
| Power Dissipation, P_D | | Full | - | - | 450 | - | - | 540 | mW |
| I_+ , Current | Note 6 | Full | - | - | 15 | - | - | 18 | mA |
| I_- , Current | Note 6 | Full | - | - | 15 | - | - | 18 | mA |

NOTES:

- V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
- At temperatures above 90°C, care must be taken to assure V_{IN} remains at least 1.0V below the V_{SUPPLY} for proper operation.
- $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$.
- $V_{IN} = 0V$, $C_L = 100pF$, enable input pulse = 3V, $f = 500kHz$.
- $C_L = 40pF$, $R_L = 1K$. Due to the pin to pin capacitance between IN 8/4B and OUT B, channel 8/4B exhibits 60dB of OFF isolation under the above test conditions.
- $V_{EN} = +2.4V$.

TRUTH TABLE HI-518 Used as an 8-Channel Multiplexer or 4-Channel Differential Multiplexer

| USE A_2 AS DIGITAL ADDRESS INPUT | | | | ON CHANNEL TO | |
|------------------------------------|-------|-------|-------|---------------|-------|
| ENABLE | A_2 | A_1 | A_0 | OUT A | OUT B |
| L | X | X | X | None | None |
| H | L | L | L | 1A | None |
| H | L | L | H | 2A | None |
| H | L | H | L | 3A | None |
| H | L | H | H | 4A | None |
| H | H | L | L | None | 1B |
| H | H | L | H | None | 2B |
| H | H | H | L | None | 3B |
| H | H | H | H | None | 4B |

TRUTH TABLE HI-518 Used as a Differential 4-Channel Multiplexer

| A_2 CONNECT TO V-SUPPLY | | | ON CHANNEL TO | |
|---------------------------|-------|-------|---------------|-------|
| ENABLE | A_1 | A_0 | OUT A | OUT B |
| L | X | X | None | None |
| H | L | L | 1A | 1B |
| H | L | H | 2A | 2B |
| H | H | L | 3A | 3B |
| H | H | H | 4A | 4B |

Test Circuits and Waveforms

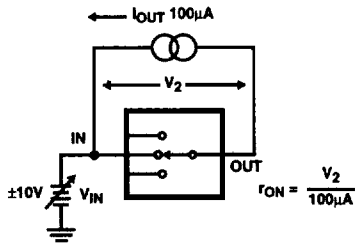


FIGURE 1. ON RESISTANCE vs INPUT SIGNAL LEVEL

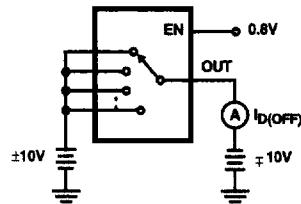


FIGURE 2. $I_{D(OFF)}$ (NOTE 1)

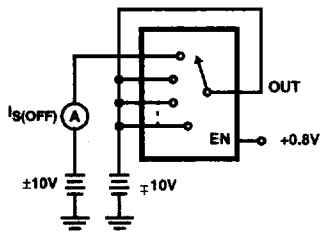


FIGURE 3. $I_{S(OFF)}$ (NOTE 1)

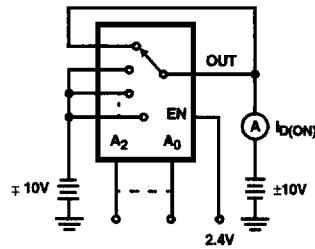


FIGURE 4. $I_{D(ON)}$ (NOTE 1)

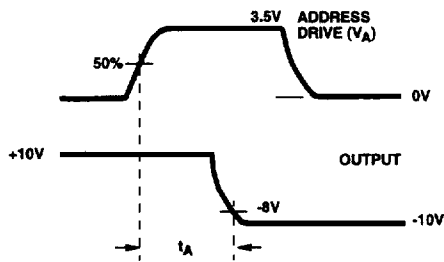


FIGURE 5A.

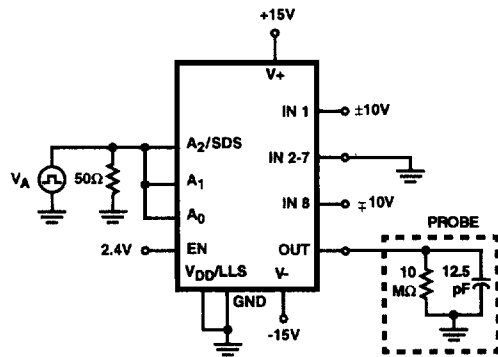


FIGURE 5B.

FIGURE 5. ACCESS TIME

NOTE:

- Two measurements per channel: $\pm 10V$ and $\mp 10V$. (Two measurements per device for $I_{D(OFF)}$ $\pm 10V$ and $\mp 10V$.)

Test Circuits and Waveforms (Continued)

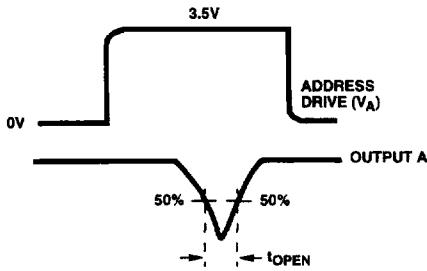


FIGURE 6A.

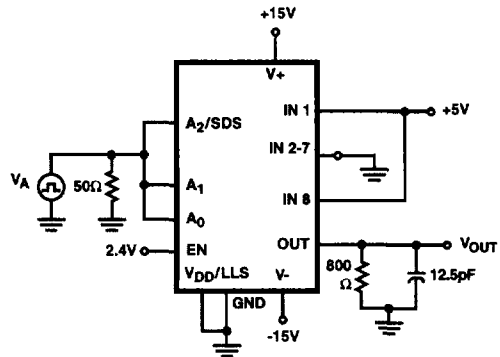


FIGURE 6B.

FIGURE 6. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

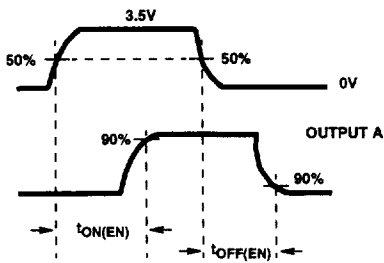


FIGURE 7A.

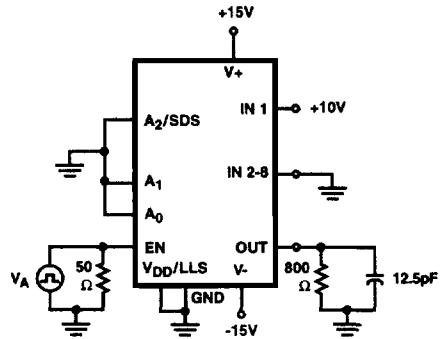


FIGURE 7B.

FIGURE 7. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

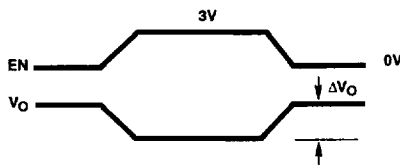


FIGURE 8A.

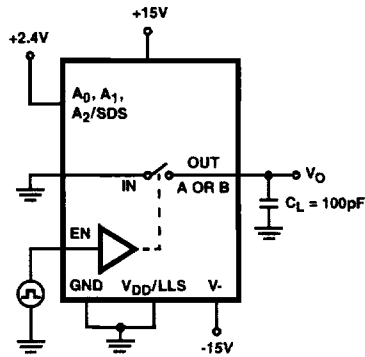


FIGURE 8B.

ΔV_O is the measured voltage error due to charge injection. The error voltage in coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 8. CHARGE INJECTION TEST CIRCUIT

HI-518

Die Characteristics

DIE DIMENSIONS:

89 mils x 93 mils

METALLIZATION:

Type: AlCu
Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

SUBSTRATE POTENTIAL (NOTE):

$-V_{\text{SUPPLY}}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: $3.5\text{k}\text{\AA} \pm 1.0\text{k}\text{\AA}$
Silox Thickness: $12\text{k}\text{\AA} \pm 2.0\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

$1.43 \times 10^5 \text{ A/cm}^2$

TRANSISTOR COUNT:

356

PROCESS:

CMOS-DI

NOTE: The substrate appears resistive to the $-V_{\text{SUPPLY}}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{\text{SUPPLY}}$ potential.

Metallization Mask Layout

