

August 1997

Quad CMOS Analog Switches

Features

- Switches Greater Than 20V_{p-p} Signals with ±15V Supplies
- Quiescent Current <10μA
- Break-Before-Make Switching
 - t_{OFF} (Typ)..... 500ns
 - t_{ON} (Typ)..... 1000ns
- TTL, CMOS Compatible
- IH5052 4 Normally Closed Switches
- IH5053 4 Normally Open Switches
- Low r_{DS(ON)} (Typ) 80Ω

Ordering Information

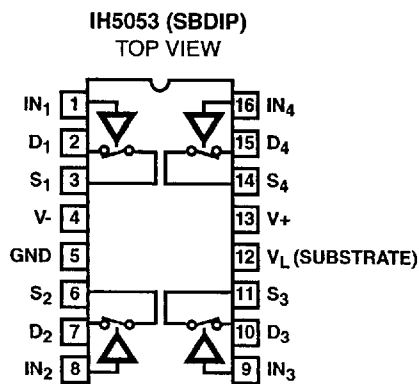
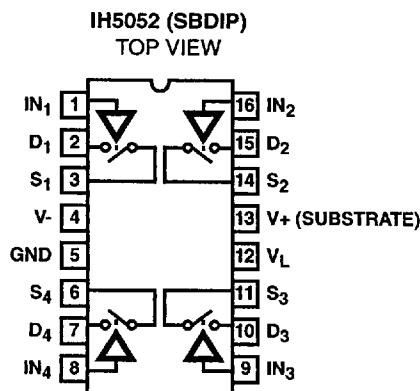
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
IH5052CDE	-0 to 70	16 Ld SBDIP	D16.3
IH5052MDE	-55 to 125	16 Ld SBDIP	D16.3
IH5053CDE	-0 to 70	16 Ld SBDIP	D16.3
IH5053MDE	-55 to 125	16 Ld SBDIP	D16.3

Description

The IH5052, IH5053 analog switches use an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Key performance advantages are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10μA.

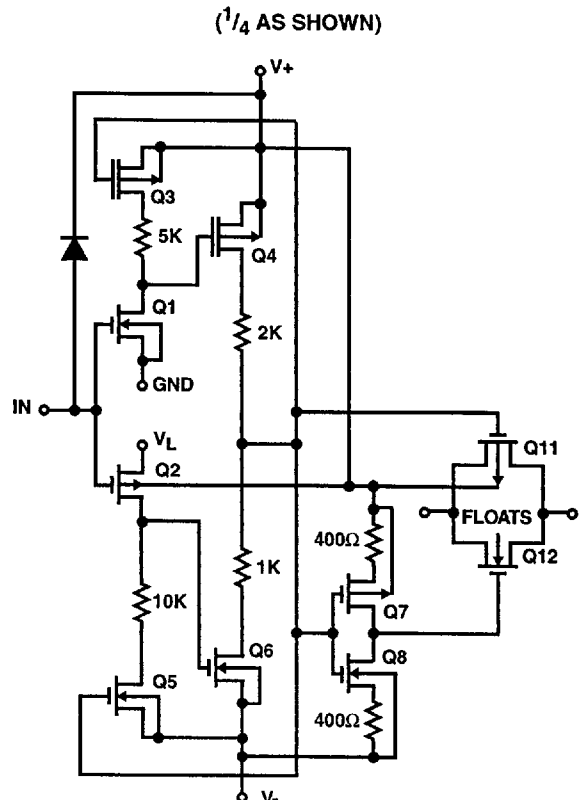
The IH5052, IH5053 also guarantees Break-Before-Make switching. This is accomplished by extending the t_{ON} time (1000ns) such that it exceeds t_{OFF} time (500ns). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel shorting during switching. With a logic "0" (0.8V or less) at its control inputs, the IH5052 switches are closed, while the IH5053 switches are closed with a logic "1" (2.4V or more) at its control inputs.

Pinouts



Switch states shown for logic "1" input

Functional Diagram



IH5052, IH5053

Absolute Maximum Ratings

V+ to V-	<36V
V+ to V _D	<30V
V _D to V-	<30V
V _D to V _S	±22V
V _L to V-	<33V
V _L to V _{IN}	<30V
V _L to GND	<20V
V _{IN} to GND	<20V
Continuous Current (S-D)	30mA
Peak Current (S-D)	70mA
(Pulsed at 1ms, 10% Duty Cycle, Max)	

Thermal Information

Maximum Junction Temperature (Ceramic Package)	175°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Operating Conditions

Temperature Ranges

M Suffix	-55°C to 125°C
C Suffix	0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^\circ\text{C}$, V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETER	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNITS
		-55°C	25°C	125°C	0°C	25°C	70°C	
Input Logic Current, I _{IN(ON)}	V _{IN} = 2.4V (IH5053) = 0.8V (IH5052)	10	±1	10	-	±10	-	μA
Input Logic Current, I _{IN(OFF)}	V _{IN} = 0.8V (IH5053) = 2.4V (IH5052)	10	±1	10	-	±10	-	μA
Drain Source On Resistance, r _{DS(ON)}	I _S = 10mA, V _{ANALOG} = -10V to +10V	75	75	100	80	80	100	Ω
Channel to Channel, r _{DS(ON)} Match	(Note 2)	-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V _{ANALOG}	(Note 2)	-	±11 (Typ)	-	-	±10 (Typ)	-	V
Switch OFF Leakage Current, I _{D(OFF)} , I _{S(OFF)}	V _{ANALOG} = -10V to +10V	-	±1	100	-	±5	100	nA
Switch On Leakage Current, I _{D(ON)} + I _{S(ON)}	V _D = V _S = -10V to +10V	-	±2	200	-	±10	100	nA
Switch "ON" Time, t _{ON}	R _L = 1kΩ, V _{ANALOG} = -10V to +10V See Figure 7	-	500	-	-	1000	-	ns
Switch "OFF" Time, t _{OFF}	R _L = 1kΩ, V _{ANALOG} = -10V to +10V See Figure 7	-	250	-	-	500	-	ns
Charge Injection, Q(INJ)	See Figure 8 (Note 2)	-	15 (Typ)	-	-	20 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio OIRR	f = 1MHz, R _L = 100Ω, C _L ≤ 5pF See Figure 4 (Note 2)	-	54 (Typ)	-	-	50 (Typ)	-	dB
+ Power Supply Quiescent Current, I ₊	V+ = +15V, V- = -15V, V _L = +5V	10	10	100	10	10	100	μA
- Power Supply Quiescent Current, I ₋	V+ = +15V, V- = -15V, V _L = +5V	10	10	100	10	10	100	μA
+5V Supply Quiescent Current, I _{V_L}	V+ = +15V, V- = -15V, V _L = +5V	10	10	100	10	10	100	μA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTE:

2. Typical values are for Design Aid only, not guaranteed nor production tested.

Typical Performance Curves

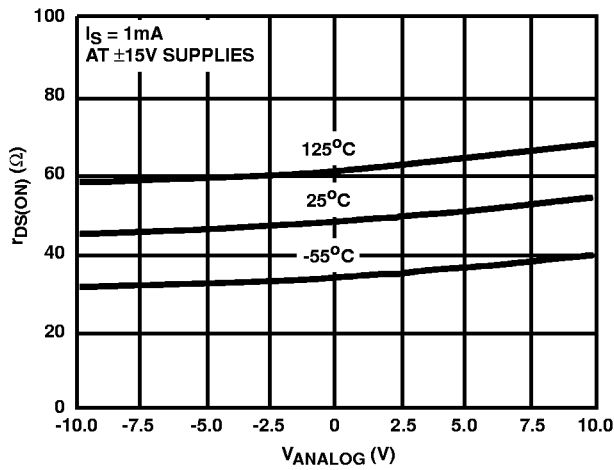


FIGURE 1. $r_{DS(ON)}$ vs V_{ANALOG}

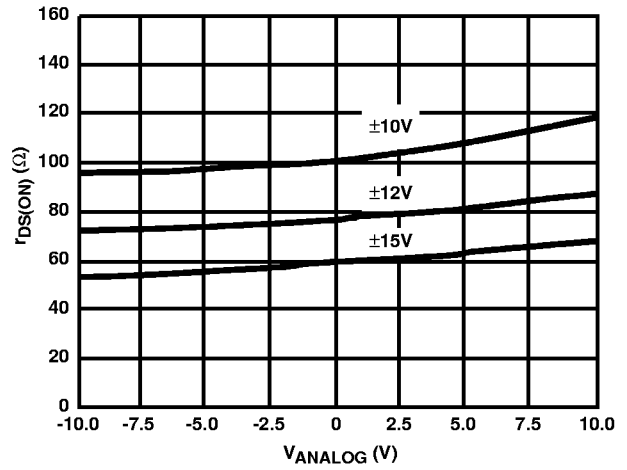


FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY VOLTAGE

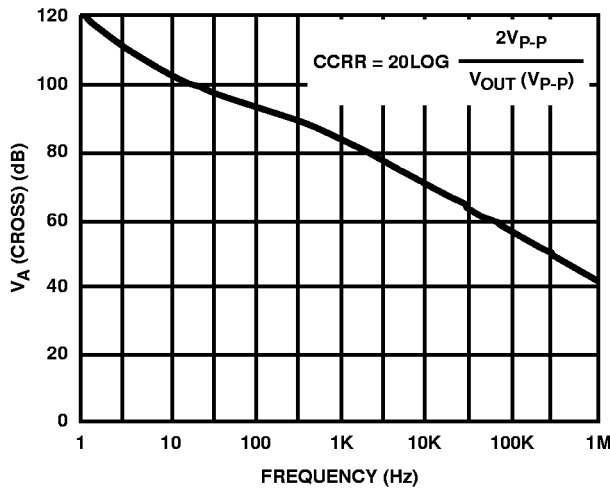


FIGURE 3A.

FIGURE 3. CROSS COUPLING REJECTION vs FREQUENCY

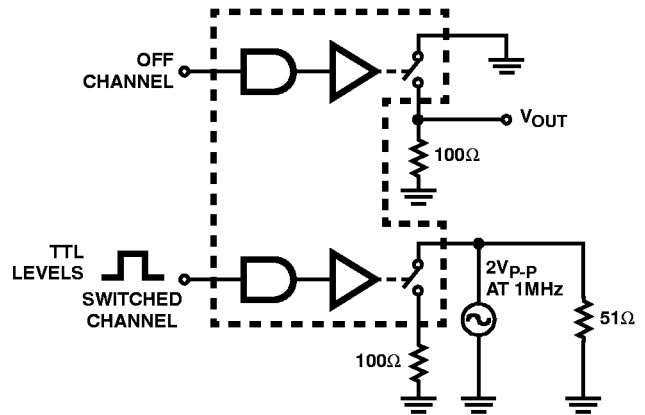


FIGURE 3B.

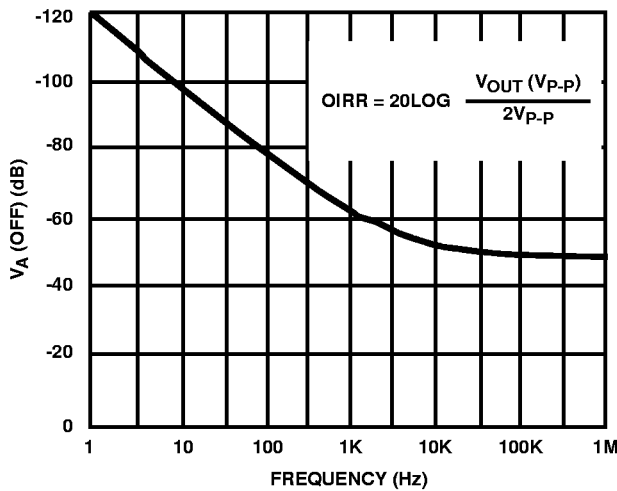


FIGURE 4A.

FIGURE 4. OFF ISOLATION vs FREQUENCY

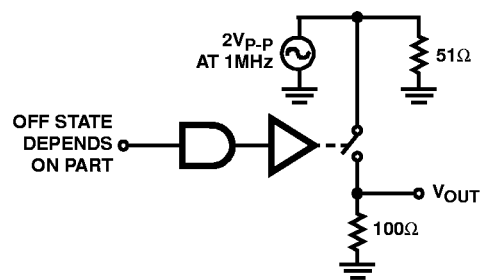


FIGURE 4B.

Typical Performance Curves (Continued)

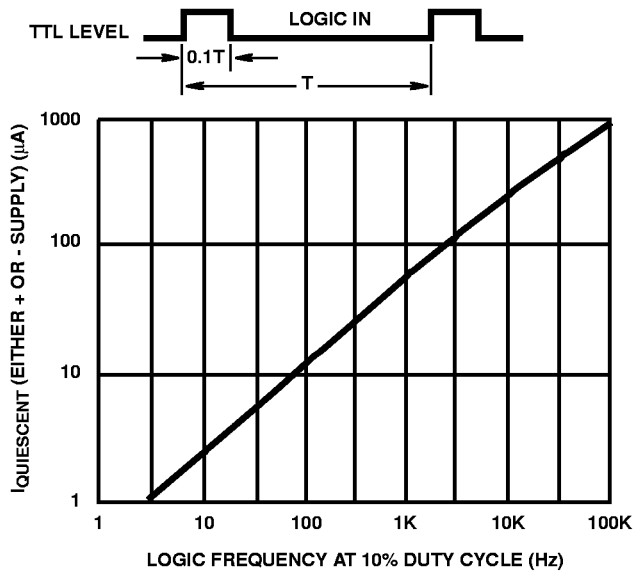


FIGURE 5. POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

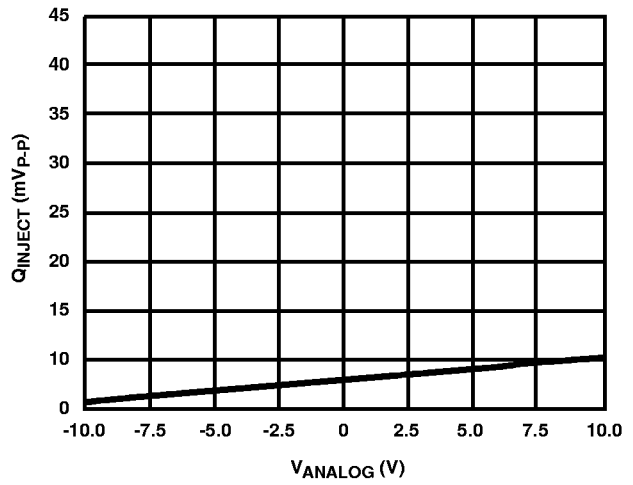


FIGURE 6. CHARGE INJECTION vs V_{ANALOG} (SEE FIGURE 8)
 $C_L = 10,000pF$

Test Circuits

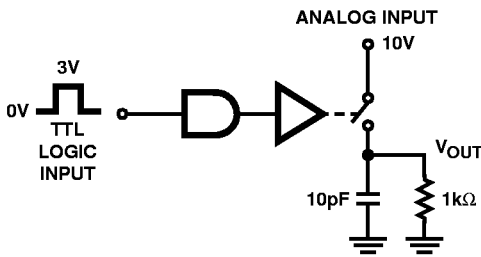


FIGURE 7.

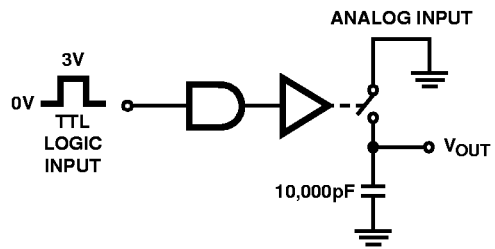


FIGURE 8.

Typical Applications

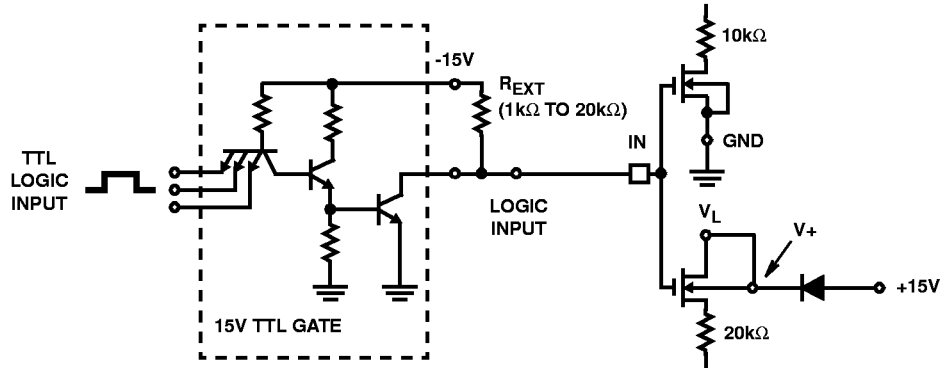


FIGURE 9. +15V OPEN COLLECTOR TTL INTERFACE TO IH5052/IH5053

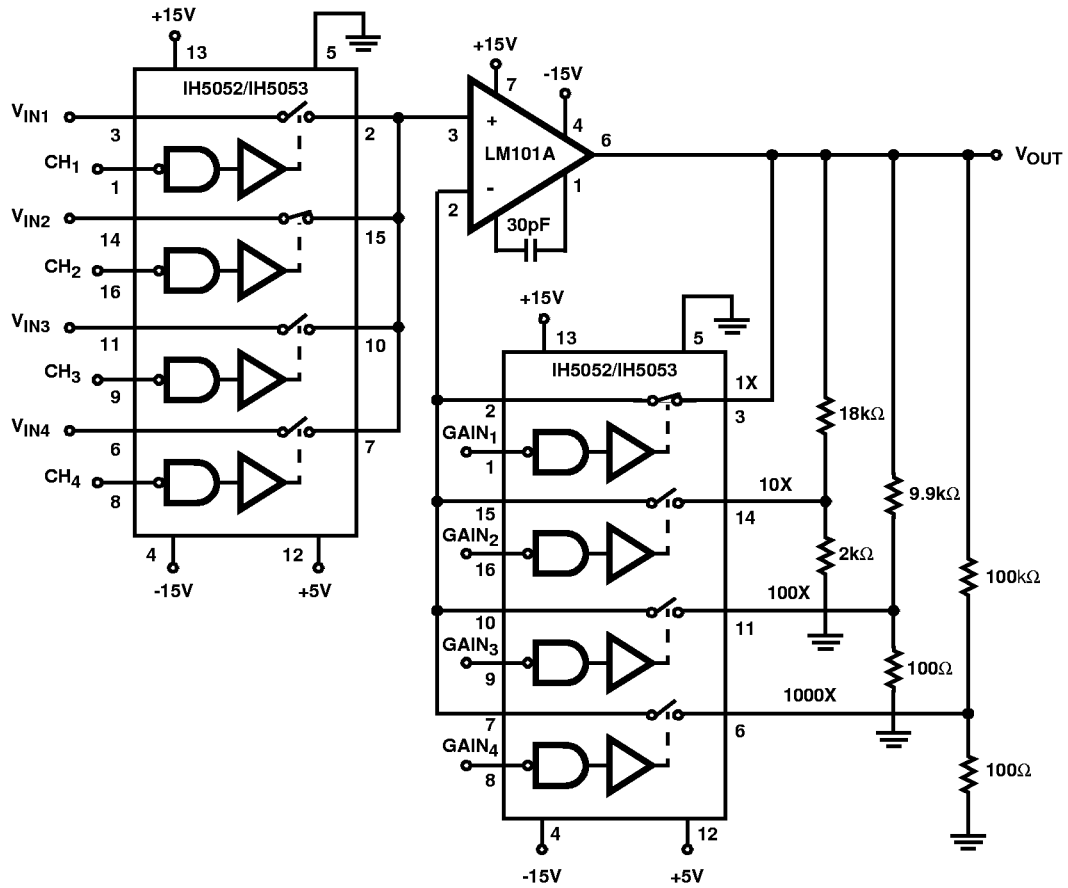


FIGURE 10. ACTIVE LOW PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY

