HARRIS HI-506A/507A

Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant..... >4,000V
- 44V Maximum Power Supply
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

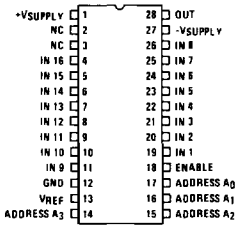
The HI-506A and HI-507A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-506A and HI-507A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-506A is a 16 channel device and the HI-507A is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

Each device is available in a 28 pin Plastic or Ceramic DIP and a 28 pad Ceramic LCC package.

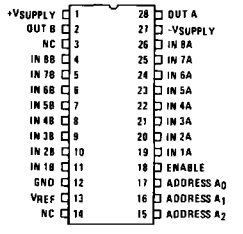
The HI-506A/507A are offered in both commercial and military grades. Additional Hi-Rel screening including 160 hour burn-in is specified by the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-546/883 or HI-547/883 data sheets.

Pinouts

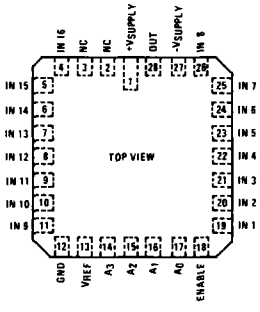
HI1-506A (CERAMIC DIP)
HI3-506A (PLASTIC DIP)
TOP VIEW



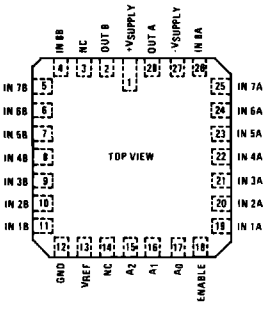
HI1-507A (CERAMIC DIP)
HI3-507A (PLASTIC DIP)
TOP VIEW



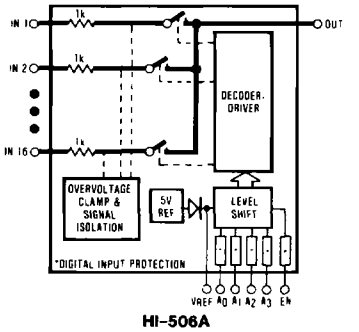
HI4-506A (CERAMIC LCC)
TOP VIEW



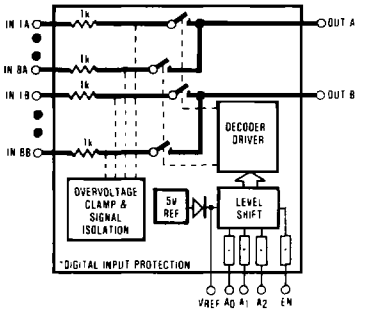
HI4-507A (CERAMIC LCC)
TOP VIEW



Functional Diagrams



HI-506A



HI-507A

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V

Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-506A/507A-2, -8 ..... -55°C to +125°C
HI-506A/507A-4 ..... -25°C to +85°C
HI-506A/507A-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{REF} pin = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-506A/HI-507A -2, -8 MIN.	TYP.	MAX.	HI-506A/507A -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
*I_D (OFF), with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-507A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
*V_{AH}, Input High Threshold (Note 8)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 9)	+25°C			0.8			0.8	V
V_{AH} MOS Drive (Note 9)	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), *Enable Delay (ON)*	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"Off Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I_+, Current Pin 1 (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I_-, Current Pin 27 (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100 μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
6. V_{EN} = 0.8 V, R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz
7. V_{EN}, V_A = 0 V or 4.0 V.
8. To drive from DTL/TTL Circuits, 1 kΩ pull-up resistors to +5.0 V supply are recommended.
9. V_{REF} = +10 V.

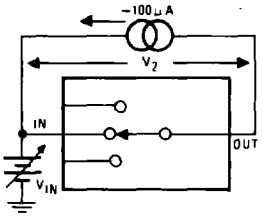
Performance Characteristics and Test Circuits

Unless Otherwise Specified: T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V And V_{Ref} = Open.

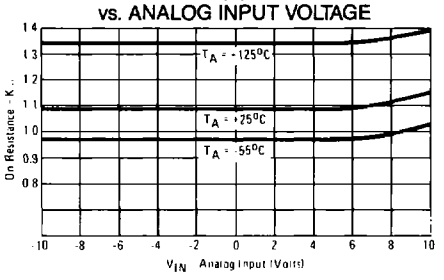
ON RESISTANCE vs.
INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

$R_{ON} = \frac{V_2}{100\mu A}$

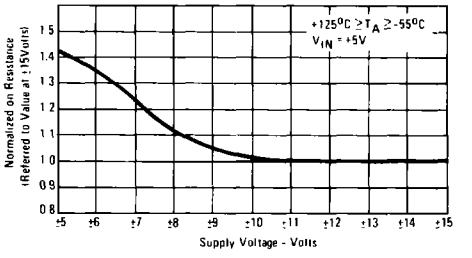
TEST CIRCUIT NO. 1



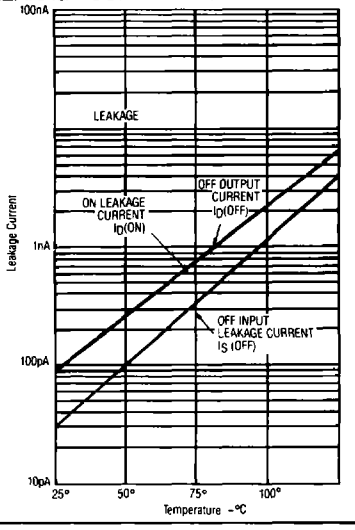
ON RESISTANCE
vs. ANALOG INPUT VOLTAGE



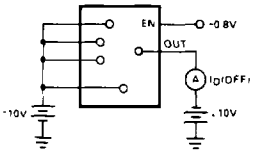
NORMALIZED ON RESISTANCE
vs. SUPPLY VOLTAGE



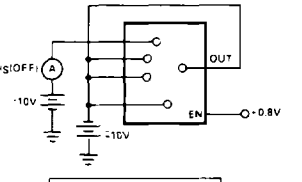
LEAKAGE CURRENT VS. TEMPERATURE



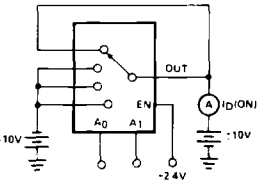
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

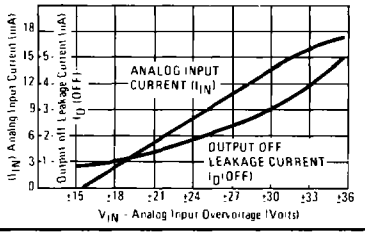


TEST CIRCUIT NO. 4*



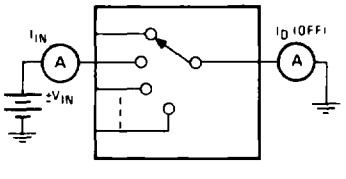
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



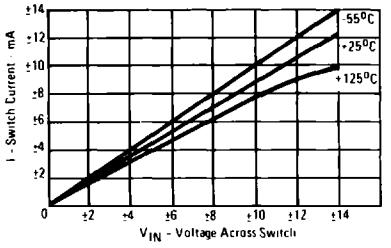
TEST CIRCUIT NO. 5

ANALOG INPUT
OVERVOLTAGE CHARACTERISTICS



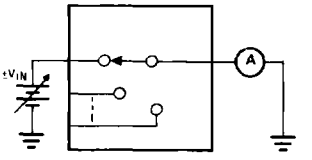
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

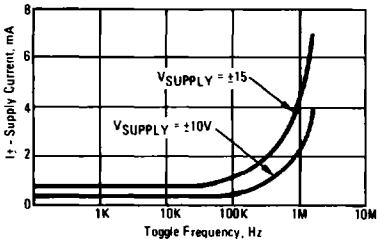


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

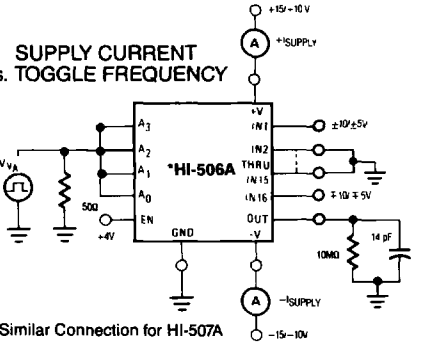


SUPPLY CURRENT vs. TOGGLE FREQUENCY



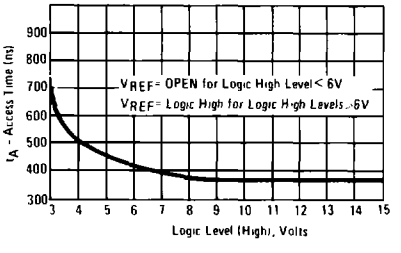
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



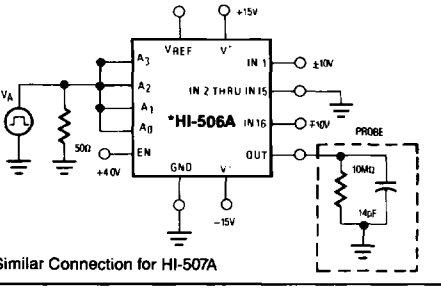
*Similar Connection for HI-507A

ACCESS TIME VS. LOGIC LEVEL (HIGH)



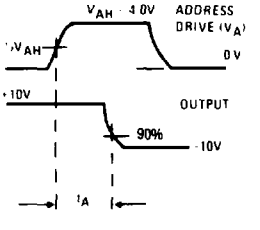
TEST CIRCUIT NO. 8

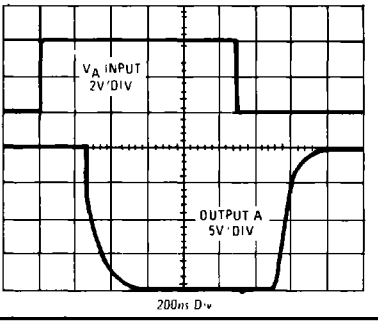
ACCESS TIME vs. LOGIC LEVEL (HIGH)



*Similar Connection for HI-507A

Switching Waveforms

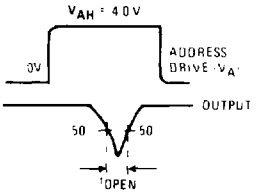


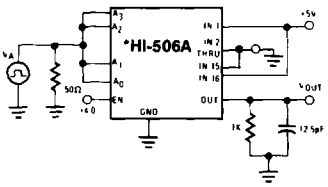


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

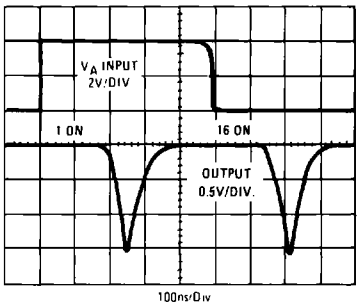
BREAK-BEFORE-MAKE DELAY (tOPEN)





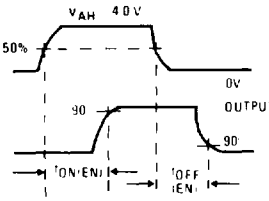
*Similar Connection for HI-507A

BREAK-BEFORE-MAKE DELAY(tOPEN)

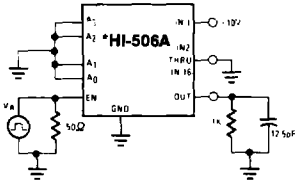


TEST CIRCUIT NO. 10

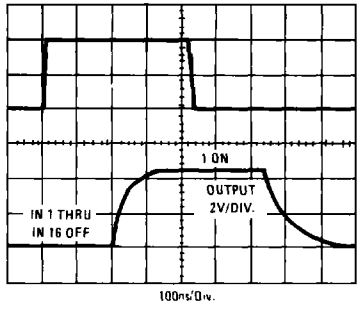
ENABLE DRIVE



ENABLE DELAY (tON(EN),tOFF(EN))

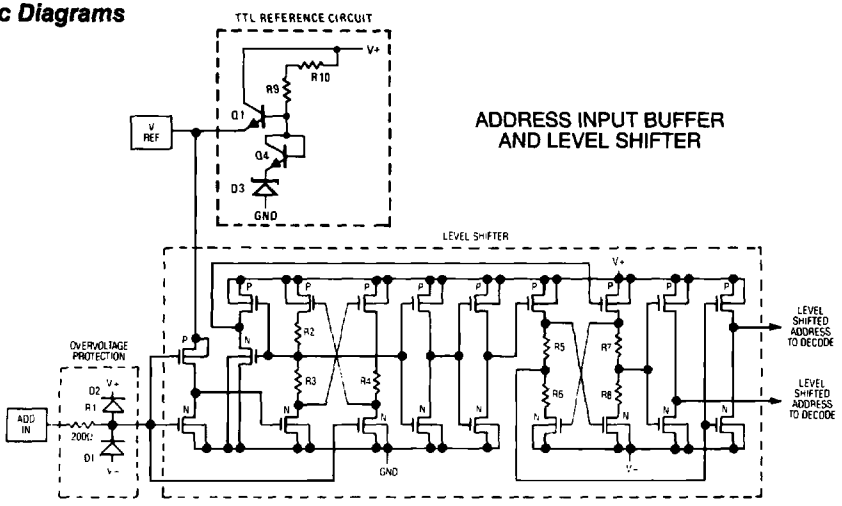


ENABLE DELAY (tON(EN),tOFF(EN))

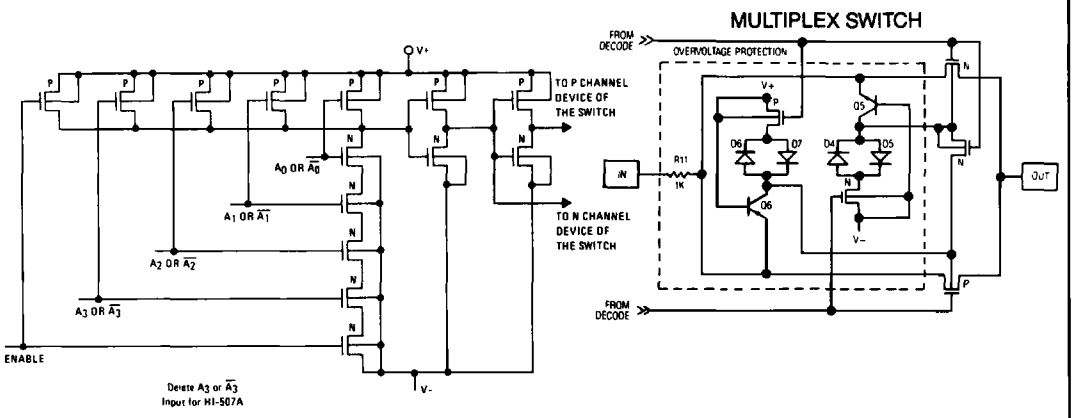


*Similar Connection for HI-507A

Schematic Diagrams



Schematic Diagrams (continued)



Die Characteristics

Transistor Count	485
Die Dimensions	159 x 84 mils
Substrate Potential*	$-V_{SUPPLY}$
Process	CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	50	18
Ceramic LCC	81	40

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

8