RAA227063

4.5V to 60V 3-Phase Smart Gate Driver

The RAA227063 is a smart gate driver IC for 3-phase Brushless DC (BLDC) motor applications. It integrates three half-bridge smart gate drivers that are capable of driving up to three N-channel MOSFET bridges and supports bridge voltages from 4.5V to 60V. Each gate driver supports up to 1A source and 2A sink peak drive current with programmable drive strength control. Adjustable and adaptive dead-times are implemented to ensure robustness and flexibility. The active gate holding mechanism prevents a Miller effect-induced cross-conduction and further enhances robustness.

The device integrates power supplies that power internal analog and logic circuitry, high-side and low-side drivers, and a dedicated supply for powering external microcontrollers. The device also features a low-power Sleep mode that consumes only 20µA to maximize battery life in portable applications.

The driver control inputs can be configured to either 3-phase LI/HI or 3-phase PWM modes. Three accurate differential amplifiers with adjustable gain are integrated to support ground-side shunt current sensing or low-side $r_{DS(ON)}$ current sensing for each bridge. The device can also support sensorless operation using back EMF in brushless DC motors.

The device can be configured to use either a hardware interface or SPI interface. For hardware interface configuration, key driver operating parameters can be set using resistor pin-straps. For SPI configuration, all the parameters can be set through the SPI Bus, which allows better monitoring.

Extensive protection functions include bridge voltage UV protection, buck-boost OV/UV/OC protection, charge pump UV protection, MOSFET drain-to-source voltage OC protection, current sense overcurrent protection, thermal warning, and shutdown. Fault conditions are indicated on a dedicated nFAULT pin and in SPI status registers.

Applications

- Power tools, fans, pumps, E-bikes
- Industrial automation, robotics, drones

Features

- Wide V_{IN} range: 4.5V to 60V (65V abs max)
- Switching frequency range up to 200kHz
- 3-Phase drive for BLDC application
  - Peak 1A/2A source/sink current with programmable drive strength
  - Supports 8 adjustable levels of drive strength through hardware interface and 16 adjustable levels of drive strength through SPI interface
- Adaptive and adjustable dead time
- Fully integrated power supply architecture
  - Two VCC LDOs allow for Sleep mode low I_Q
  - 500mA buck-boost switching regulator generates drive voltage (5V to 15V adjustable)
  - 200mA adjustable output LDO for MCU supplies
- Flexible configuration
  - 3-phase HI/LI mode and 3-phase PWM mode
  - Support half-bridge, full-bridge configuration
- Three current sense amplifiers
  - Four levels of sense gain setting
  - Supports DC offset calibration during power-up and on-the-fly
  - Supports both ground-side shunt sense or low-side MOSFET $r_{DS(ON)}$ sense
- Back-EMF sensing for BLDC sensorless operation
- Features both hardware interface and SPI interface
- Extensive fault protection functions (VCC UV, VM/VBRIDGE UV, charge pump UV, MOSFET VDS OCP, current sense OCP, thermal warning/shutdown, buck-boost current limiting, buck-boost OCP, buck-boost UV/OV)
- Supports reverse battery protection by additional external circuitry
- 7mm x 7mm 48 Ld QFN package (0.5mm pitch)

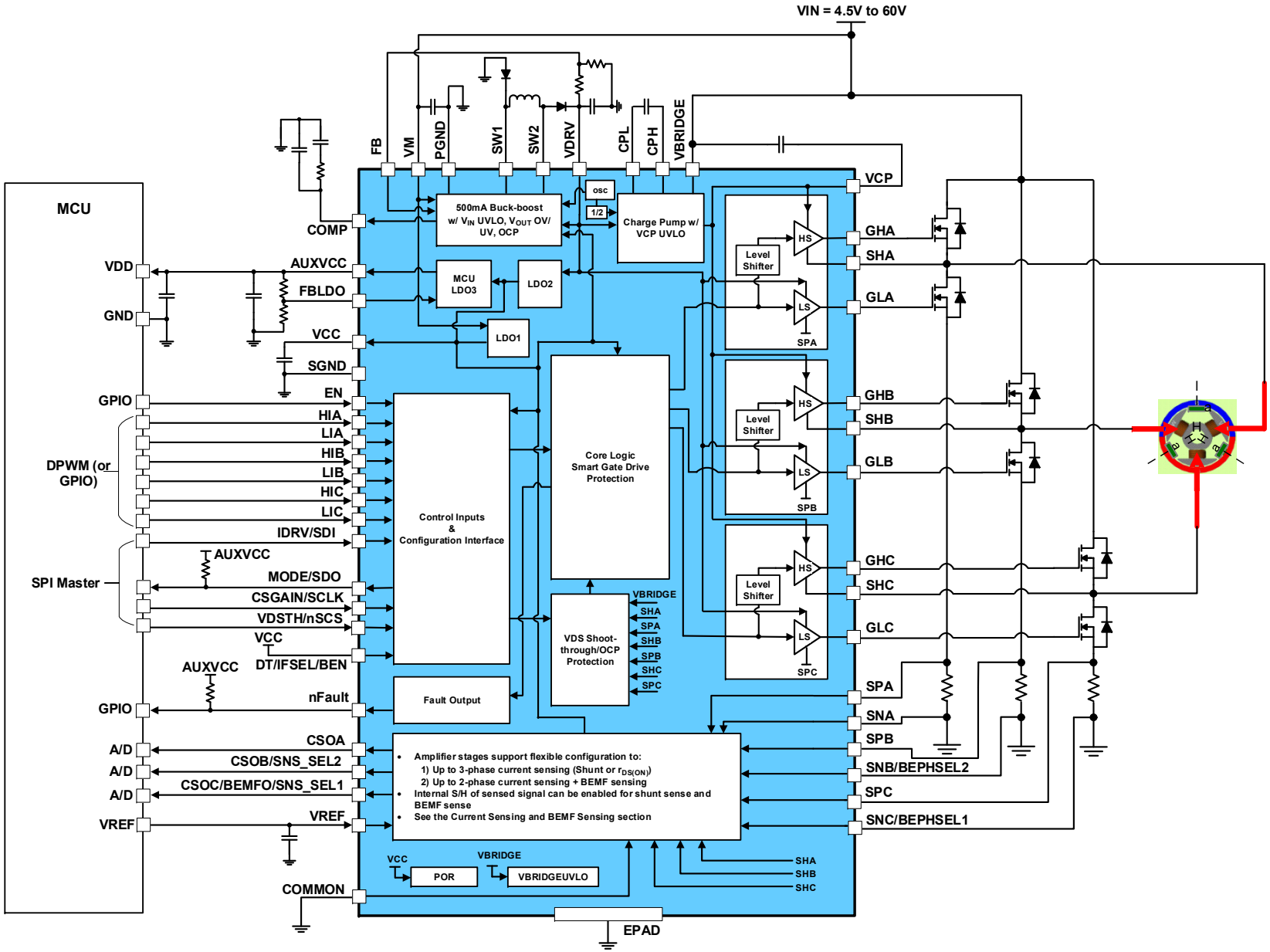


Figure 1. Typical Application Diagram

Contents

1. Overview

1.1 Typical Application Circuits

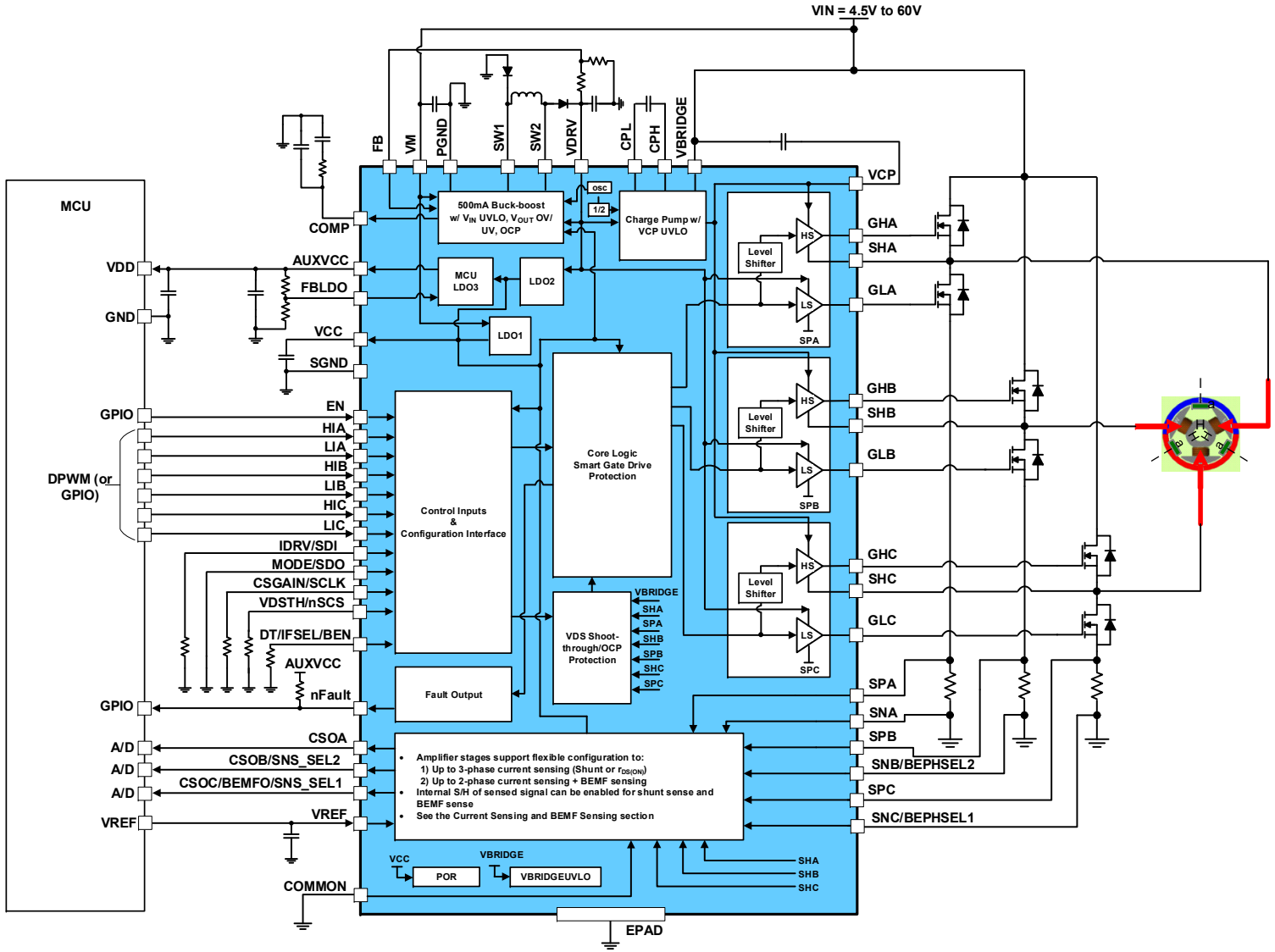


Figure 2. RAA227063 Simplified Diagram and Application – Hardware Interface Operation, BEMF Sensing Disabled, No S/H for Current Sense

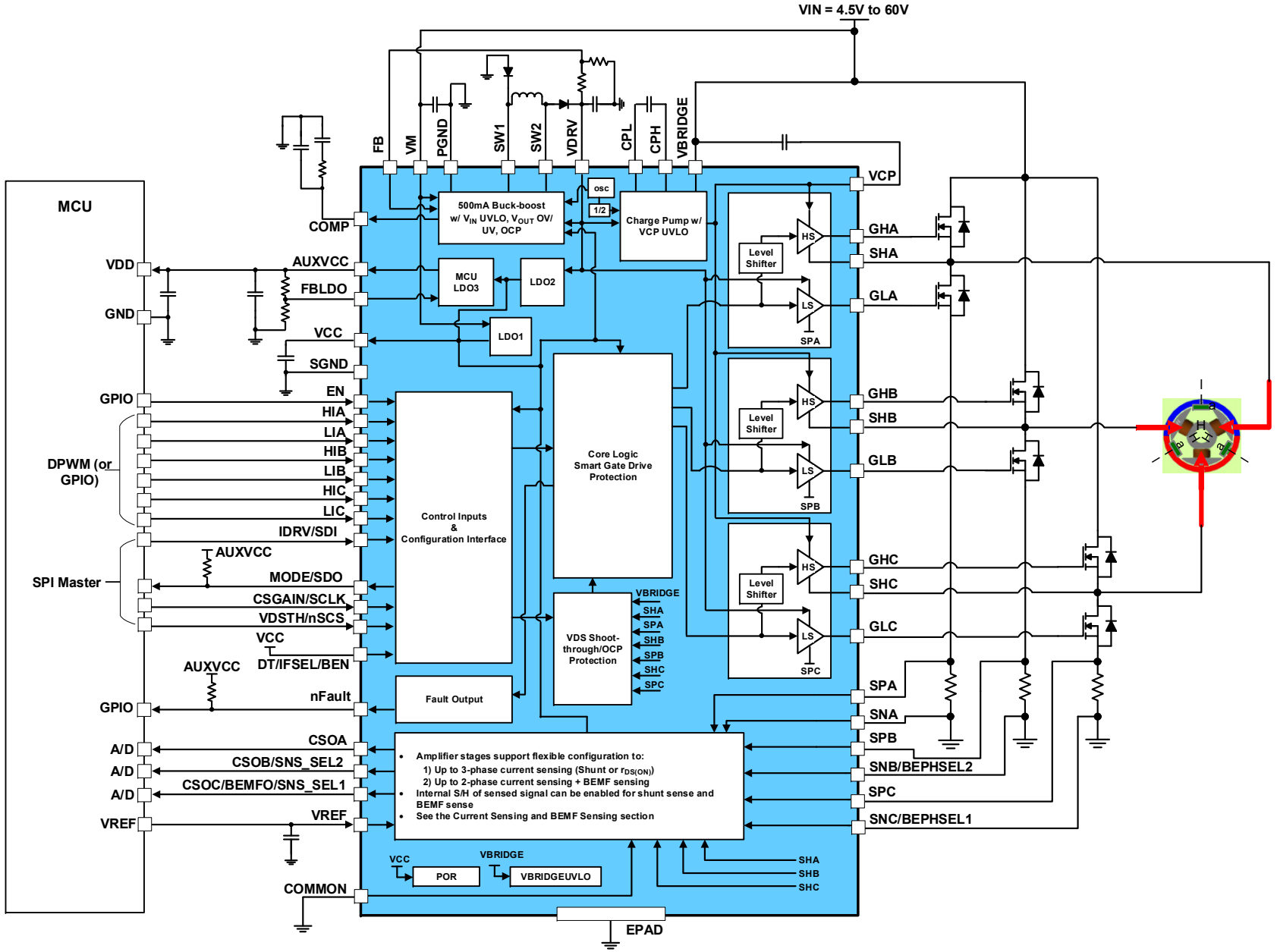


Figure 3. RAA227063 Simplified Diagram and Application – SPI Interface Operation, BEMF Sensing Disabled, No S/H for Current Sense

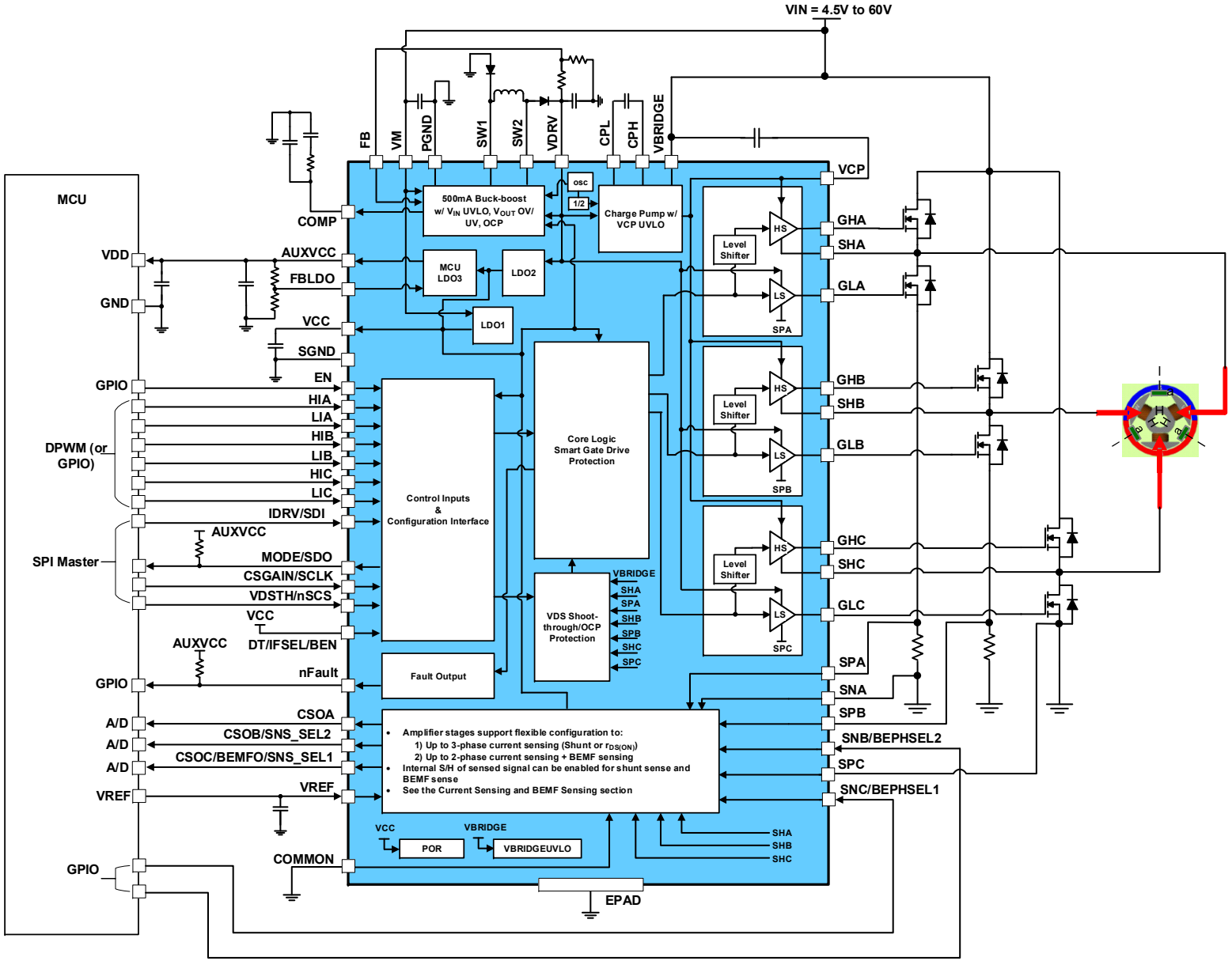


Figure 4. RAA227063 Simplified Diagram and Application – SPI Interface Operation, BEMF Sensing Enabled Using Internal Virtual Common Signal, No S/H for Current Sense or BEMF Sense

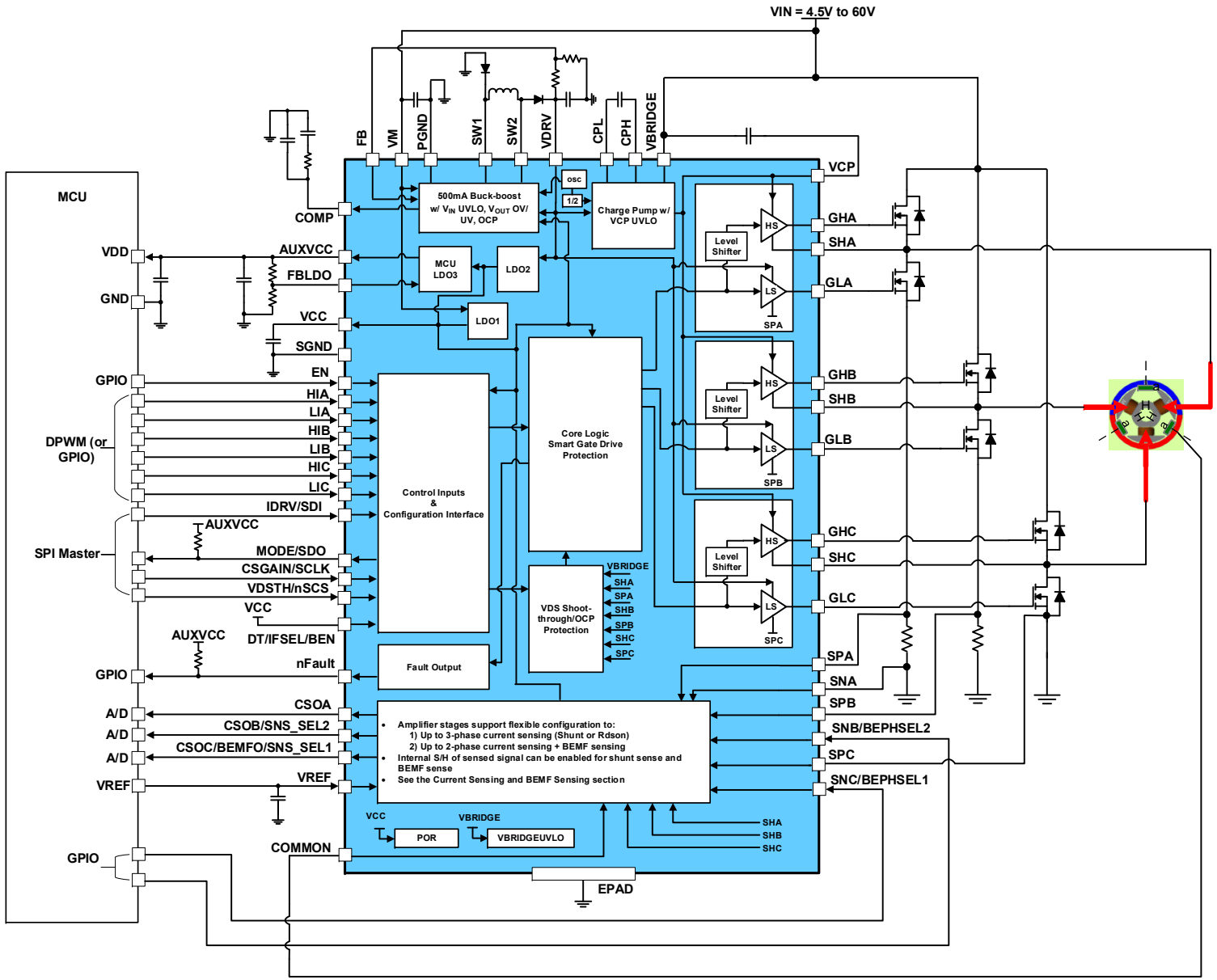


Figure 5. RAA227063 Simplified Diagram and Application – SPI Interface Operation, BEMF Sensing Enabled Using External Direct Motor Common (center tap) Connection, No S/H for Either Current Sensing or BEMF Sensing

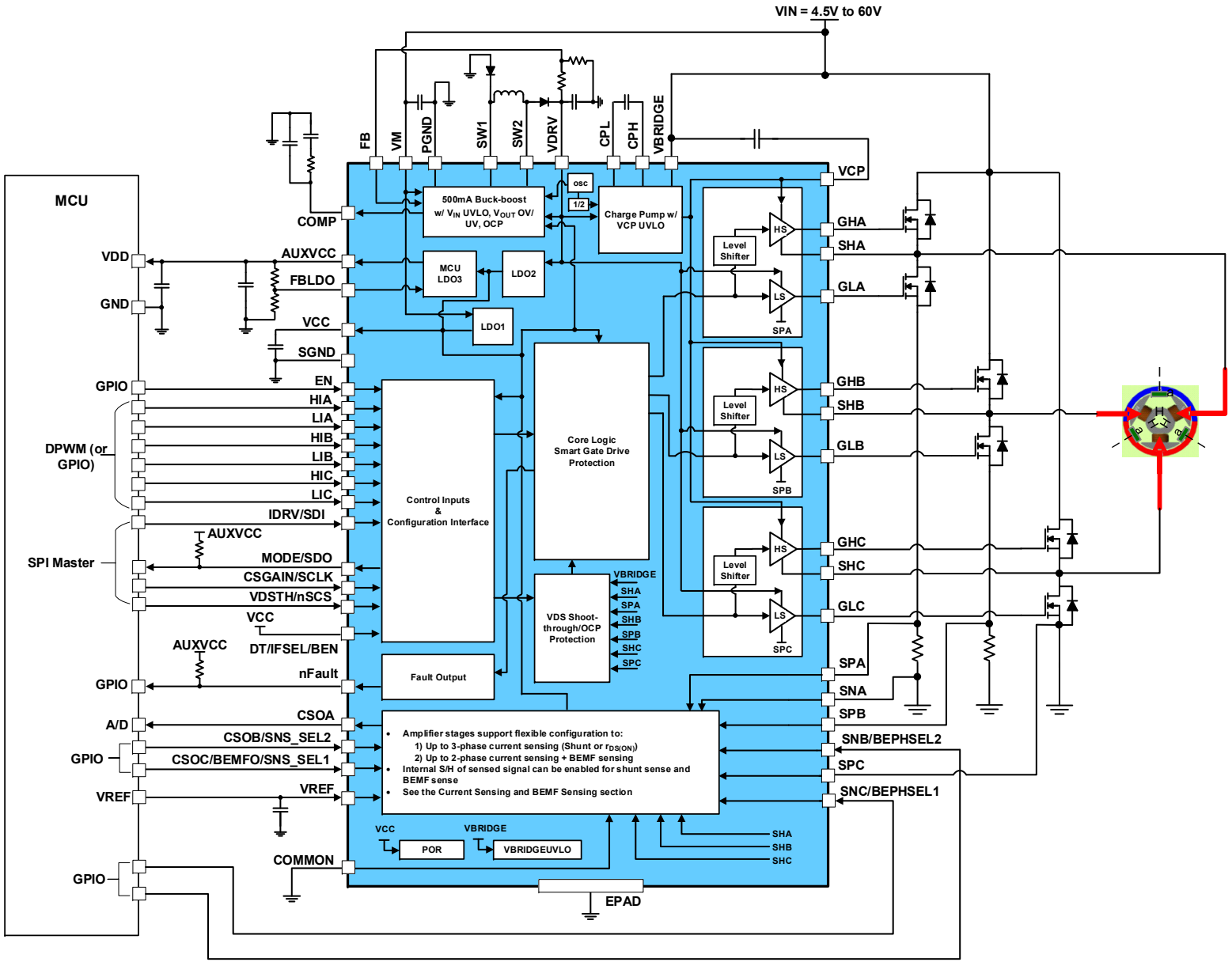
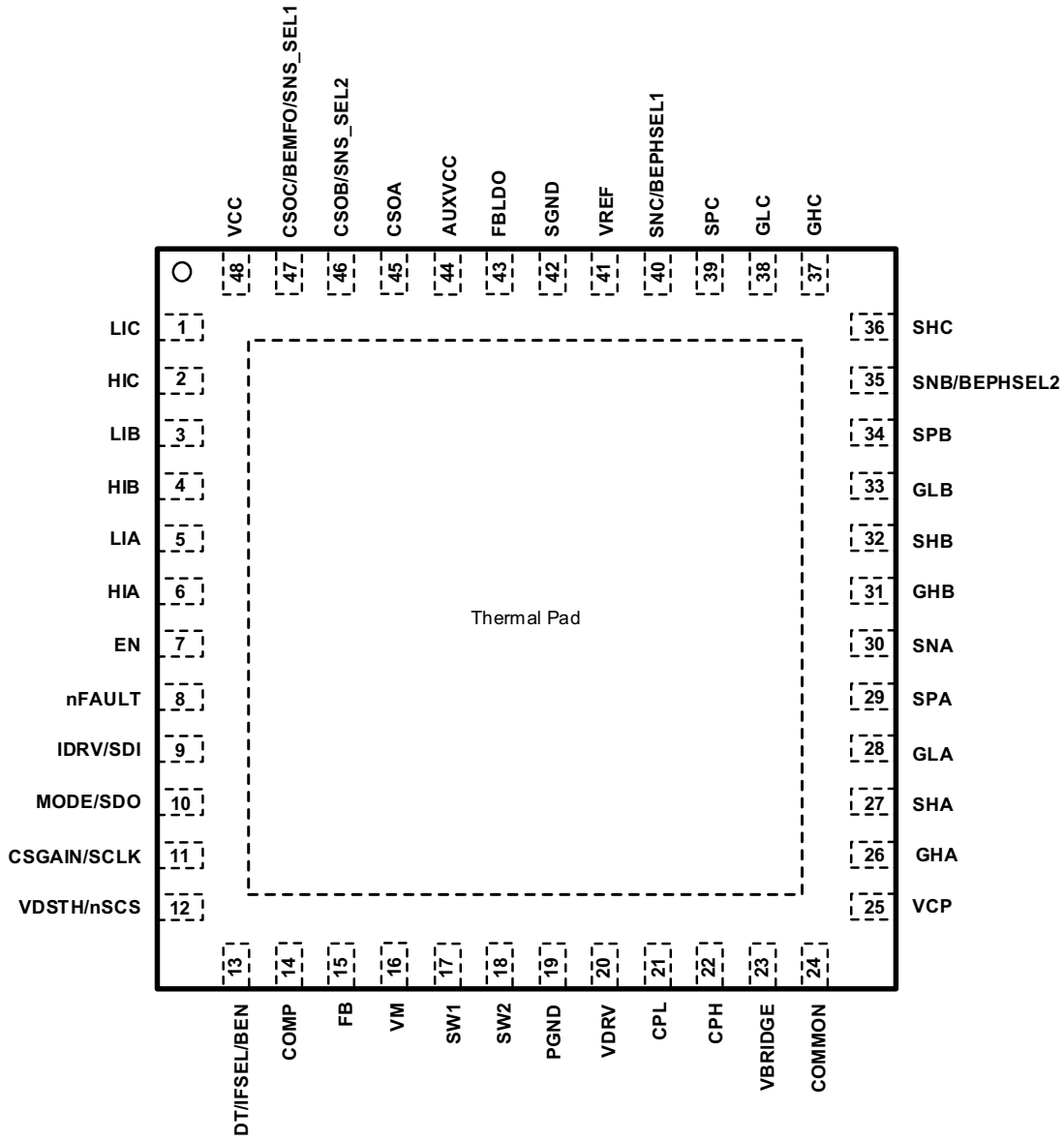


Figure 6. RAA227063 Simplified Diagram and Application –
SPI Interface Operation, BEMF Sensing Enabled Using Internal Virtual Common Signal, Internal S/H Enabled for Both Current Sensing or BEMF Sensing

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin #	Pin Name	Description
1	LIC	Phase C low-side driver control input.
2	HIC	Phase C high-side driver control input.
3	LIB	Phase B low-side driver control input.
4	HIB	Phase B high-side driver control input.
5	LIA	Phase A low-side driver control input.
6	HIA	Phase A high-side driver control input.

Pin #	Pin Name	Description
7	EN	IC normal operation mode enable pin. Pulling high puts the IC into normal operating mode; pulling low or being left floating puts the IC into low power Sleep mode.
8	nFAULT	Fault indicator pin. This is an open-drain output pin that requires an external pull-up resistor. If not being set to take no action through the SPI interface, this pin is pulled low if any fault occurs, and released if all fault conditions are removed and all necessary power rails are up. **Note:** This pin is only in valid state 5µs after EN goes high. In shutdown mode, the internal pull-down device is disabled to lower the shutdown current.
9	IDRV/SDI	Dual function pin. ▪ If the device is Eight as a hardware interface, this pin serves as the driver peak source current setting pin. Eight levels of source current settings are supported through resistor on this pin. The setting is detected and latched up after the device is put into operating mode and all the power rail soft-starts are done. ▪ If the device is configured as an SPI interface, this pin serves as the SPI data input pin.
10	MODE/SDO	Dual function pin. ▪ If the device is configured as a hardware interface, this pin serves as the mode setting pin that sets PWM mode and current sensing mode. • If tied to VCC directly, the device works in 3-phase PWM mode, using ground-side shunt resistor for current sensing. • If tied to SGND through a 60.4kΩ resistor, the device works in 3-phase PWM mode and uses low-side $r_{DS(ON)}$ for current sensing. • If tied to SGND through a 25kΩ resistor, the device works in 3-phase HI/LI mode and uses low-side $r_{DS(ON)}$ for current sensing. • If tied to SGND directly, the device works in 3-phase HI/LI mode and uses ground-side shunt resistors for current sensing. The setting is detected and latched after the device is put into operating mode and all the power rail soft-starts are done. ▪ If the device is configured as an SPI interface, this pin serves as the SPI data output pin.
11	CSGAIN/SCLK	Dual function pin. ▪ If the device is configured as a hardware interface, this pin serves as the shunt amplifier sensing gain setting pin. Four levels of gain (5V/V, 10V/V, 20V/V, 40V/V) settings are supported through resistors on this pin. The setting is detected and latched up after the device is put into operating mode and all the power rail soft-starts are done. ▪ If the device is configured as an SPI interface, this pin serves as the SPI clock input pin.
12	VDSTH/nSCS	Dual function pin. ▪ If the device is configured as a hardware interface, this pin serves as the VDS OCP threshold setting pin. Eight levels of settings are supported through resistor on this pin. The setting is detected and latched after the device is put into operating mode and all the power rail soft-starts are done. ▪ If the device is configured as an SPI interface, this pin serves as the SPI chip select pin.

Pin #	Pin Name	Description
13	DT/IFSEL/BEN	Configuration pin for dead time, interface selection, and BEMF sensing. Five levels of different settings are supported. ▪ If tied to VCC directly, the device is set to use SPI interface. Default dead time 150ns. BEMF sensing is disabled by default. **Note:** The dead time setting and BEMF sensing related functionalities can be modified through the SPI interface after the device is put into operating mode when all power rail soft-starts are done. ▪ If tied to SGND through a 120kΩ resistor, the device is set to use hardware interface, 450ns dead time, BEMF sensing feature disabled. ▪ If tied to SGND through a 60.4kΩ resistor, the device is set to use hardware interface, 250ns dead time, BEMF sensing feature disabled. ▪ If tied to SGND through a 25kΩ resistor, the device is set to use hardware interface, 150ns dead time, BEMF sensing feature is enabled with gain set to 0.5 and using the COMMON pin as the motor center tap input. ▪ If tied to SGND directly, the device is set to use hardware interface, 150ns dead time, BEMF sensing feature is enabled with gain set to 0.5 and using internal virtual center tap. The setting is detected first during device power-up (entering operating mode) because the interface selection determines other configuration pin settings. Settings are latched after the device is put into operating mode and all the power rail soft-starts are done.
14	COMP	Compensation pin. Place a type 2 compensation network from this pin to SGND.
15	FB	FB pin of buck-boost regulator. Internal reference voltage is 0.8V.
16	VM	Supply input for device internal power chains. It is the input for the buck-boost regulator and main 60mA LDO. VM and VBRIDGE are shorted inside the IC.
17	SW1	Buck-boost switch node (Buck side)
18	SW2	Buck-boost switch node (Boost side)
19	PGND	Device power ground.
20	VDRV	Output of the buck-boost switching regulator. It is the low-side driver supply and also supplies 200mA VCC LDO in Operating mode.
21	CPL	Charge pump low-side switch node.
22	CPH	Charge pump high-side switch node.
23	VBRIDGE	Bridge voltage input pin and charge pump output reference. It also senses the high-side MOSFET drain voltage. Route a trace from this pin directly to the area as close as possible to the high-side MOSFET drain pad. VM and VBRIDGE are shorted inside the IC.
24	COMMON	External motor center tap connection for BEMF sensing. If the device is configured to use the internal virtual common signal for BEMF sensing, or BEMF sensing is disabled, tie this pin directly to SGND.
25	VCP	Charge pump output. It is the high-side driver supply. Place a minimum 1µF 25V MLCC capacitor from this pin to the VBRIDGE pin.
26	GHA	Phase A high-side driver output.
27	SHA	Phase A high-side driver output return. It is also the Phase A switch node voltage sense for the purposes of VDS OCP and BEMF sense.
28	GLA	Phase A low-side driver output.
29	SPA	Phase A low-side driver output return. It is also the current sense Amplifier A positive input and the Phase A low-side MOSFET source sense for VDS OCP and adaptive dead time.
30	SNA	Negative input of current sense amplifier A. **Note:** If BEMF sensing is enabled, the Phase A and B current sense amplifier negative inputs are both connected to the SNA pin internally.
31	GHB	Phase B high-side driver output.
32	SHB	Phase B high-side driver output return. It is also the Phase B switch node voltage sense, for the purposes of VDS OCP and BEMF sense.

Pin #	Pin Name	Description
33	GLB	Phase B low-side driver output.
34	SPB	Phase B low-side driver output return. It is also the current sense Amplifier B positive input and the Phase B low-side MOSFET source sense for VDS OCP and adaptive dead time.
35	SNB/BEPHSEL2	Dual function pin: ▪ If the BEMF function is disabled, it is the negative input of current sense Amplifier B. ▪ If the BEMF function is enabled, it is the BEMF sensing phase selection control signal input 2.
36	SHC	Phase C high-side driver output return. It is also the Phase C switch node voltage sense, for the purposes of VDS OCP and BEMF sense
37	GHC	Phase C high-side driver output.
38	GLC	Phase C low-side driver output.
39	SPC	Phase C low-side driver output return. It is also the current sense Amplifier C positive input. It is also the Phase C low-side MOSFET source sense for VDS OCP and adaptive dead time
40	SNC/BEPHSEL1	Dual function pin: ▪ If the BEMF function is disabled, it is the negative input of current sense Amplifier C. ▪ If the BEMF function is enabled, it is the BEMF sensing phase selection control signal input 1.
41	VREF	Current sense amplifier reference voltage input. It is divided down to ½ to supply actual amplifier reference voltage.
42	SGND	IC signal ground
43	FBLDO	Auxiliary LDO output voltage feedback pin. AUXVCC output voltage can be adjusted by changing resistor divider ratio. **Note:** The internal reference voltage is 1.2V nominal.
44	AUXVCC	Auxiliary LDO supply for MCU and peripheral. **Note:** Its voltage can be adjusted through the FBLDO pin. The input to this LDO is VCC, which is 5V. Therefore, if the MCU needs 5V supply, tie directly to VCC instead of AUXVCC.
45	CSOA	If internal S/H is disabled, this pin is current sense amplifier A output. If S/H is enabled for either current sense, BEMF sensing or both, this pin is the buffered output of an internal analog multiplexer that selects from the S/H output of CSA, CSB, and CSC.
46	CSOB/SNS_SEL2	Dual function pin. ▪ If internal S/H is disabled, this pin is a current-sense amplifier B output. ▪ If internal S/H is enabled for either current sense, BEMF sensing, or both, this pin is the control signal 2 input for an internal analog multiplexer that selects from the S/H output of CSA, CSB, and CSC.
47	CSOC/BEMFO/SNS_SEL1	Multiple function pin. If internal S/H is disabled: ▪ If the Back-EMF sensing function is enabled, Amplifier C is used to sense the motor back-emf. This pin is the sensed motor back-EMF output. ▪ If the Back-EMF sensing function is disabled, Amplifier C is used to sense voltage across external shunt or $r_{DS(ON)}$. This pin is the sensed voltage output. If internal S/H is enabled for either current sense, BEMF sensing or both, this pin is the control signal 1 input for internal analog multiplexer that selects from the S/H output of CSA, CSB, and CSC.
48	VCC	Internal LDO output that supplies IC analog and logic bias. At start up, before IC is enabled, VCC is powered by LDO1 from VM. When the IC is enabled and the buck-boost regulator is running, VCC is obtained from LDO2 fed by VDRV. A value of 10µF MLCC decoupling capacitor is recommended to be placed as close as possible between this pin and SGND.
-	EPAD	Thermal and GND pad. Connect it to the system ground plane on the board level to achieve low thermal impedance.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter		Minimum	Maximum	Unit
VBRIDGE to GND, VM to GND		-0.3	65	V
VCC to GND		-0.3	5.5	V
GHx to SHx (x = A, B, C)		-0.3	16	V
VDRV to GND		-0.3	16	V
VCP to GND, VCP to SHx (x = A, B, C), CPH to GND		-0.3	VBRIDGE + 16	V
SHx (x = A, B, C) to GND, COMMON to GND		-5	VBRIDGE + 5	V
SPx (x = A, B, C) to GND, SNA to GND, SNB/BEPHSEL2 to GND, SNC/BEPHSEL1 to GND		DC: -0.3 Transient (< 200ns): -1	VCC + 0.3	V
GHx (x = A, B, C) to GND		-5	VCP + 0.3	V
GLx (x = A, B, C) to GND		-1	VDRV + 0.3	V
CPL to GND		-0.3	VDRV + 0.3	V
SW2 to GND		-0.3	VDRV + 2	V
SW1 to GND		-0.3	VM + 0.3	V
All Other Pins		-0.3	VCC + 0.3	V
ESD Rating		**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)		1.5		kV
Charged Device Model (Tested per JS-002-2018)		750		V
Latch-Up (Tested per JESD78E; Class 2, Level B, 125°C)	GHA, GHB, GHC, SHA, SHB, SHC	90		mA
	All other pins	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
48 Ld 7x7 QFN Package	25	1.2

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature, T_J	-55	+150	°C
Operating Temperature, T_A	-40	+125	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VBRIDGE to GND, VM to GND	4.5	60	V
VCC to GND	0	5.25	V
VDRV to GND	5	14	V
EN, VDSTH/nSCS, DT/IFSEL/BEN, HIx (x = A, B, C), LIx (x = A, B, C), IDRV/SDI, FBLDO, AUXVCC, MODE/SDO, CSGAIN/SCLK, nFAULT, CSOA, CSOB/SNS_SEL2, CSOC/BEMFO/SNS_SEL1, VREF	0	5.25	V
Operating Ambient Temperature Range, T_A	-40	125	°C
Operating Junction Temperature Range, T_J	-40	150	°C

3.4 Electrical Specifications

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Bridge Supply						
Operating Supply Current (VM and VBRIDGE combined)	I_{DDO}	VM = VBRIDGE = 48V, EN = 3.3V, HIx/LIx = 0V, COMP = 0, VDRV = 0, Charge Pump and Buck-boost regulator not switching VREF = 0		2.4		mA
VM Sleep Mode Supply Current	$I_{VMsleep}$	EN = 0V, VM = 48V, T_A = 25°C, no load on AUXVCC		23	40	µA
Sleep Mode Entry Time Delay	t_{sleep}	Transition time from EN = 0V to Sleep mode		0.5		ms
Wake-Up Delay from Sleep Mode	t_{wake}	VCC > VCC_POR, EN goes from 0V to 3.3V to all power rails startup ready, with recommended 2.2µF and 0.22µF capacitors between VM-VCP and CPH-CPL, respectively		6.5		ms
Internal Main 5V LDO1						
Output Voltage	VCC1	VM = 60V, EN = 0V, load = 0mA		5		V
		VM = 4.5V, EN = 0V, load = 10mA	4.0	4.4		V
		VM = 8V, EN = 0V, load = 10mA		5		V
Current Limit		VM = 12V, EN = 0V		39		mA
		VM = 12V, EN = 3.3V, LDO2 is off		128		mA
AUXVCC LDO3						
Output Voltage	AUXVCC	EN = 3.3V, VDRV = 5V, AUXVCC set to 3.3V, load = 0mA	3.05	3.30	3.60	V
Operating Mode Current Limit		EN = 3.3V, VDRV = 12V, AUXVCC set to 3.3V		220		mA
Sleep Mode Output Voltage		EN = 0V, load = 1mA, VM = 24V		3.5		V

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Internal 5V LDO2						
Output Voltage	VCC2	EN = 3.3V, VDRV = 8V, load = 0mA	4.65	5.00	5.45	V
		EN = 3.3V, VDRV = 15V, load = 0mA	4.65	5.00	5.45	V
Current Limit		EN = 3.3V, VDRV = 12V		220		mA
Buck-Boost Supply						
Output Voltage Adjustment Range	VDRV		5		15	V
Reference Voltage	V_{REF_BB}			0.8		V
Operating Source Current	I_{DDO_BB}			5		mA
FB Pin Source Current			-50		50	nA
Transconductance Amplifier Gain	gm			200		µS
Transconductance Amplifier Output Capability				±18		µA
Transconductance Amplifier Maximum Output		FB = 0.7V		3.95		V
Transconductance Amplifier Minimum Output		FB = 1V		0.02		V
Ramp Offset				870		mV
Oscillator Frequency	f_{SWBB}		410	500	590	kHz
Minimum On-Time	t_{min_on}			130		ns
Minimum Off-Time	t_{min_off}			142		ns
Soft-Start Time	t_{ss}			5.5		ms
Cycle-By-Cycle Current Limit	I_{oc_1}			1.4		A
Hiccup Current Limit Threshold	I_{oc_2}			1.6		A
Buck to Buck-Boost Transition Threshold	VM - VDRV	VM = 10V and ramp VDRV voltage		1.9		V
Buck-Boost to Buck Transition Hysteresis				1.6		V
Charge Pump Supply						
Charge Pump Voltage to VBRIDGE	VCP - VBRIDGE	VM = VBRIDGE = 4.5V, VDRV = 5V, I_{VCP} = 0mA		4.93		V
		VM = VBRIDGE = 24V, VDRV = 12V, I_{VCP} = 25mA		10.75		V
		VM = VBRIDGE = 48V, VDRV = 12V, I_{VCP} = 25mA		10.58		V

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
EN Logic Level						
EN Rise Threshold	V_{RS_TH}			1.1		V
EN Fall Threshold	V_{FL_TH}			0.92		V
EN Threshold Hysteresis	V_{EN_HYS}			160		mV
Logic Level Input Signals (LIx, HIx, IDRV/SDI, CSGAIN/SCLK, VDSTH/nSCS, SNB/BEPHSEL2, SNC/BEPHSEL1, CSOB/SNS_SEL2, CSOC/BEMFO/SNS_SEL1)						
Logic-Low Voltage Level Threshold	V_IL			1.21		V
Logic-High Voltage Level Threshold	V_IH			1.57		V
Logic Level Hysteresis	V_HYS			350		mV
Logic-Low Current	I_IL	Voltage level = 0V		15		nA
Logic-High Current	I_IH	Voltage level = 5V, EN = 3.3V		14		µA
		Voltage level = 3.3V, EN = 3.3V		9		µA
Internal Pull-Down Resistance	R_IPD			380		kΩ
Logic Level Output Signals (nFault, MODE/SDO)						
Logic-Low Voltage Level	V_OL	I_O = 2mA sinking		0.24		V
High Impedance Output Leakage	I_OHLk	V_O = 5V		50		nA
Gate Drivers						
Gate Driver Strength						
Peak Source Current	I_{src} (HW I/F selected)	IDRV/SDI tied to SGND		70		mA
		IDRV/SDI 25kΩ to SGND		160		mA
		IDRV/SDI 62kΩ to SGND		220		mA
		IDRV/SDI 133kΩ to SGND		310		mA
		IDRV/SDI 91kΩ to VCC		400		mA
		IDRV/SDI 50kΩ to VCC		500		mA
		IDRV/SDI 25kΩ to VCC		700		mA
		IDRV/SDI tied to VCC		1100		mA

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Peak Source Current (Cont.)	I_{src} (SPI I/F selected)	I_SRC_HS[3:0] = 0000b		50		mA
		I_SRC_HS[3:0] = 0001b		70		mA
		I_SRC_HS[3:0] = 0010b		120		mA
		I_SRC_HS[3:0] = 0011b		160		mA
		I_SRC_HS[3:0] = 0100b		200		mA
		I_SRC_HS[3:0] = 0101b		220		mA
		I_SRC_HS[3:0] = 0110b		250		mA
		I_SRC_HS[3:0] = 0111b		310		mA
		I_SRC_HS[3:0] = 1000b		350		mA
		I_SRC_HS[3:0] = 1001b		400		mA
		I_SRC_HS[3:0] = 1010b		440		mA
		I_SRC_HS[3:0] = 1011b		500		mA
		I_SRC_HS[3:0] = 1100b		580		mA
		I_SRC_HS[3:0] = 1101b		700		mA
		I_SRC_HS[3:0] = 1110b		900		mA
		I_SRC_HS[3:0] = 1111b		1100		mA
Peak Sink Current	I_{snk} (HW I/F selected)	IDRV/SDI tied to SGND		180		mA
		IDRV/SDI 25kΩ to SGND		350		mA
		IDRV/SDI 62kΩ to SGND		500		mA
		IDRV/SDI 133kΩ to SGND		650		mA
		IDRV/SDI 91kΩ to VCC		800		mA
		IDRV/SDI 50kΩ to VCC		1000		mA
		IDRV/SDI 25kΩ to VCC		1400		mA
		IDRV/SDI Tied to VCC		2400		mA

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Peak Sink Current (Cont.)	I_{snk} (SPI I/F selected)	I_SRC_HS[3:0] = 0000b		130		mA
		I_SRC_HS[3:0] = 0001b		180		mA
		I_SRC_HS[3:0] = 0010b		280		mA
		I_SRC_HS[3:0] = 0011b		350		mA
		I_SRC_HS[3:0] = 0100b		420		mA
		I_SRC_HS[3:0] = 0101b		500		mA
		I_SRC_HS[3:0] = 0110b		560		mA
		I_SRC_HS[3:0] = 0111b		650		mA
		I_SRC_HS[3:0] = 1000b		700		mA
		I_SRC_HS[3:0] = 1001b		800		mA
		I_SRC_HS[3:0] = 1010b		880		mA
		I_SRC_HS[3:0] = 1011b		1000		mA
		I_SRC_HS[3:0] = 1100b		1200		mA
		I_SRC_HS[3:0] = 1101b		1400		mA
		I_SRC_HS[3:0] = 1110b		1800		mA
		I_SRC_HS[3:0] = 1111b		2400		mA
Strong Sink Current	I_{snk_strg}			2500		mA
Pull-Up Source Current	I_{pu}			40		mA
Pull-Down Sink Current	I_{pd}			100		mA
Gate Pull-Down Resistor	R_{pd}			90		kΩ
High-Side Gate Clamp	VGH_CLAMP	I_{pu} = 40mA	13.3	14.3	15.3	V
High-Side Gate Driver High-Level Output Voltage	VGSHH	1mA load, VDRV = 10V, SHx = VBRIDGE = 12V, differential voltage between GHx and SHx		9.7		V
High-Side Gate Driver Low-Level Output Voltage	VGSHL	-1mA load, VDRV = 10V, SHx = VBRIDGE = 12V, differential voltage between GHx and SHx		3.0		mV
Low-Side Gate Driver High-Level Output Voltage	VGSLH	1mA load, VDRV = 10V, SHx = VBRIDGE = 12V, differential voltage between GLx and SPx		10.0		V
Low-Side Gate Driver Low-Level Output Voltage	VGSLL	-1mA load, VDRV = 10V, SHx = VBRIDGE = 12V, differential voltage between GLx and SPx		2.5		mV
Dead-Time and Maximum Gate Transition Time						
Adaptive Dead Time VGS Falling Threshold				1		V
Adaptive Dead Time VGS Threshold Hysteresis				2		V

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Gate Drive Default Dead Time	t_{dt} (HW I/F is selected)	DT/IFSEL/BEN tied to SGND		150		ns
		DT/IFSEL/BEN 25kΩ to SGND		150		ns
		DT/IFSEL/BEN 60.4kΩ to SGND		250		ns
		DT/IFSEL/BEN 120kΩ to SGND		450		ns
	t_{dt} (SPI I/F is selected)	DT/IFSEL/BEN tied to VCC, DEAD_TIME[1:0] = 00b		100		ns
		DT/IFSEL/BEN tied to VCC, DEAD_TIME[1:0] = 01b		150		ns
		DT/IFSEL/BEN tied to VCC, DEAD_TIME[1:0] = 10b		250		ns
		DT/IFSEL/BEN tied to VCC, DEAD_TIME[1:0] = 11b		450		ns
Max Gate Transition Time	t_{gt_max} (SPI I/F selected)	DT/IFSEL/BEN tied to VCC, T_GT[1:0] = 00b		0.5		µs
		DT/IFSEL/BEN tied to VCC, T_GT[1:0] = 01b		1.0		µs
		DT/IFSEL/BEN tied to VCC, T_GT[1:0] = 10b		2.0		µs
		DT/IFSEL/BEN tied to VCC, T_GT[1:0] = 11b		4.0		µs
3-phase HI/LI Mode Propagation Delay						
HIX Turn-On Delay	t_{rh}	LIX = L, HIX = L to H to VGHX-VSHX starts to rise		40		ns
HIX Turn-Off Delay	t_{fh}	LIX = L, HIX = H to L to VGHX-VSHX starts to fall		40		ns
LIX Turn-On Delay	t_{rl}	HIX = L, LIX = L to H to VGLX starts to rise		40		ns
LIX turn-Off Delay	t_{fl}	HIX = L, LIX = H to L to VGLX starts to fall		40		ns
Gate Drive Off Delay when HIX and LIX Turning High	$t_{goff\_LI\_HI}$	HIX = H, LIX = L to H to VGHX-VSHX starts to fall		40		ns
		LIX = H, HIX = L to H to VGLX starts to fall		40		ns
Gate Drive On Delay when HIX and LIX Recover from Both High Conditions	$t_{gon\_LI\_HI}$	HIX = H, LIX = H to L to VGHX-VSHX starts to rise		40		ns
		LIX = H, HIX = H to L to VGLX starts to rise		40		ns
3-phase PWM Mode Propagation Delay						
PWM GHX Turn-Off Delay	t_{GHxpwm}	LIX = H, HIX = H to L to VGHX – VSHX falling		40		ns
PWM GLX Turn-Off Delay	t_{GLxpwm}	LIX = H, HIX = HIX = L to H to GLX = H to L		40		ns
Gate Drive Off Delay when LIX Turning Low	t_{goff_pwm}	LIX = H to L to VGHX-VSHX/GLX falling		40		ns

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Gate Drive On Delay when LIX Turning High	t_{gon_pwm}	LIX = L to H to VGHX-VSHX/GLX rising		40		ns
Current Sense Amplifier						
Amplifier Gain (Shunt sense)	G_{cs} (HW I/F selected)	CSGAIN/SCLK tied to SGND	4.5	5	5.2	V/V
		CSGAIN/SCLK 25kΩ to SGND	9.1	10	10.4	V/V
		CSGAIN/SCLK 60.4kΩ to SGND	18.3	20	20.7	V/V
		CSGAIN/SCLK 120kΩ to SGND	35.8	40	41.2	V/V
	G_{cs} (SPI I/F selected)	CS_GAIN[1:0] = 00b	4.5	5	5.2	V/V
		CS_GAIN[1:0] = 01b	9.1	10	10.4	V/V
		CS_GAIN[1:0] = 10b	18.3	20	20.7	V/V
		CS_GAIN[1:0] = 11b	35.8	40	41.2	V/V
Amplifier Gain Error (Shunt sense)		Input differential >0.025V	-11		4.5	%
Amplifier Gain ($r_{DS(ON)}$ sense)	G_{cs} (HW I/F selected)	CSGAIN/SCLK tied to SGND	4.1	5	5.4	V/V
		CSGAIN/SCLK 25kΩ to SGND	8.5	10	10.8	V/V
		CSGAIN/SCLK 60.4kΩ to SGND	17.0	20	21.5	V/V
		CSGAIN/SCLK 120kΩ to SGND	33.0	40	42.5	V/V
	G_{cs} (SPI I/F selected)	CS_GAIN[1:0] = 00b	4.1	5	5.4	V/V
		CS_GAIN[1:0] = 01b	8.5	10	10.8	V/V
		CS_GAIN[1:0] = 10b	16.5	20	21.5	V/V
		CS_GAIN[1:0] = 11b	33.0	40	42.5	V/V
Amplifier Gain Error ($r_{DS(ON)}$ sense)		Input differential >0.025V	-19		9	%
Settling Time to ±1%		G_{cs} = 5 V/V, output step = 0.5V, C_{load} = 60pF		150		ns
		G_{cs} = 10 V/V, output step = 0.5V, C_{load} = 60pF		250		ns
		G_{cs} = 20 V/V, output step = 0.5V, C_{load} = 60pF		400		ns
		G_{cs} = 40 V/V, output step = 0.5V, C_{load} = 60pF		1000		ns
Common Mode Input Voltage Range with G_{cs} = 5			-0.15		0.15	V
Differential Mode Input Voltage Range with G_{cs} = 5			-0.3		0.3	V
DC Input Offset			-4		4	mV
Amplifier Output Linear Range			0.25		V_{REF}-0.25	V
Amplifier Output Voltage Bias				V_{REF}/2		V

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Reference Buffer Error			-3%		3%	
VREF Input Current		V_{REF} = 5V, all amplifiers are running		1.7	3	mA
Unity Gain Bandwidth		60 load		5		MHz
Open loop Gain				80		dB
BEMF Sense Amplifier						
Amplifier Gain (BEMF sense)	G_{BEMF} (HW I/F selected)	CSGAIN/SCLK tied to SGND		0.5		V/V
	G_{BEMF} (SPI I/F selected)	BEMF_GAIN[1:0] = 00b	0.215	0.25	0.255	V/V
		BEMF_GAIN[1:0] = 01b	0.430	0.5	0.530	V/V
		BEMF_GAIN[1:0] = 10b	0.850	1	1.080	V/V
		BEMF_GAIN[1:0] = 11b	1.700	2	2.100	V/V
Settling Time to ±1%		G_{BEMF} = 0.25V/V, output step = 0.5V, C_{load} = 60pF		200		ns
		G_{BEMF} = 0.5V/V, output step = 0.5V, C_{load} = 60pF		300		ns
		G_{BEMF} = 1V/V, output step = 0.5V, C_{load} = 60pF		500		ns
		G_{BEMF} = 2V/V, output step = 0.5V, C_{load} = 60pF		1200		ns
DC Input Offset				40		mV
Amplifier Output Linear Range			0.25		V_{REF} - 0.25	V
Amplifier Output Voltage				V_{REF}/2		V
Reference Buffer Error			-3		3	%
Fault Management						
V_{CC} Power-On Reset Rising	VCC_POR			4.0		V
V_{CC} Power-On Reset Falling				3.6		V
VM UVLO	VM_UVLO	VM rising	3.8	4.2	4.5	V
		VM falling	3.6	3.9	4.1	V
VM UVLO Hysteresis				0.3		V
Charge Pump Undervoltage with Respect to VM	VCP_UV	VCP - VM falling		0.55 * VDRV (6.60V if VDRV = 12V)		V
Charge Pump Undervoltage Hysteresis				VCP_UV * 0.12		V

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
MOSFET VDS OCP Threshold	VDS_TH/nSCS (HW I/F selected)	VDS_TH/nSCS tied to SGND	32	75	115	mV
		VDS_TH/nSCS 25kΩ to SGND	150	240	320	mV
		VDS_TH/nSCS 62kΩ to SGND	290	400	490	mV
		VDS_TH/nSCS 133kΩ to SGND	490	645	805	mV
		VDS_TH/nSCS 91kΩ to VCC	510	710	872	mV
		VDS_TH/nSCS 50kΩ to VCC	936	1200	1510	mV
		VDS_TH/nSCS 25kΩ to VCC	1255	1600	1960	mV
		VDS_TH/nSCS tied to VCC	1710	2150	2630	mV
	VDS_TH/nSCS (SPI I/F selected)	VDS_TH[3:0] = 0000b	10	35	57	mV
		VDS_TH[3:0] = 0001b	32	75	115	mV
		VDS_TH[3:0] = 0010b	93	160	206	mV
		VDS_TH[3:0] = 0011b	150	240	320	mV
		VDS_TH[3:0] = 0100b	223	320	397	mV
		VDS_TH[3:0] = 0101b	290	400	490	mV
		VDS_TH[3:0] = 0110b	405	520	690	mV
		VDS_TH[3:0] = 0111b	490	645	805	mV
		VDS_TH[3:0] = 1000b	505	670	839	mV
		VDS_TH[3:0] = 1001b	510	710	872	mV
		VDS_TH[3:0] = 1010b	675	880	1140	mV
		VDS_TH[3:0] = 1011b	936	1200	1510	mV
		VDS_TH[3:0] = 1100b	1070	1400	1700	mV
		VDS_TH[3:0] = 1101b	1255	1600	1960	mV
		VDS_TH[3:0] = 1110b	1375	1800	2160	mV
		VDS_TH[3:0] = 1111b	1710	2150	2630	mV
VDS OCP Retry Delay Time	$t_{rtry\_delay\_VDSOCP}$ (HW I/F selected)			4000		µs
	$t_{rtry\_delay\_VDSOCP}$ (SPI I/F selected)	RETRY_DELAY_VDSOCP[0] = 0b		4000		µs
		RETRY_DELAY_VDSOCP[0] = 1b		70		µs
Shunt Current Sense OCP Threshold	CSOCP_TH (HW I/F selected)			1000		mV
	CSOCP_TH (SPI I/F selected)	CSOCP_TH[2:0] = 000b	32	50	61	mV
		CSOCP_TH[2:0] = 001b	76	100	123	mV
		CSOCP_TH[2:0] = 010b	118	150	173	mV
		CSOCP_TH[2:0] = 011b	163	200	240	mV
		CSOCP_TH[2:0] = 100b	191	250	302	mV
		CSOCP_TH[2:0] = 101b	408	500	564	mV
		CSOCP_TH[2:0] = 110b	616	750	847	mV
		CSOCP_TH[2:0] = 111b	818	1000	1124	mV

VM = 48V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Shunt Current Sense OCP Retry Delay Time	$t_{rtry\_delay\_CSOCP}$ (HW I/F selected)			4000		µs
	$t_{rtry\_delay\_CSOCP}$ (SPI I/F selected)	RETRY_DELAY_CSOCP[0] = 0b		4000		µs
		RETRY_DELAY_CSOCP[0] = 1b		70		µs
VDS OCP and Shunt Current Sense OCP Deglitch Time	t_{deg_OCP} (HW I/F selected)			3.2		µs
	t_{deg_OCP} (SPI I/F selected)	DEG_TIME[1:0] = 00b		1.4		µs
		DEG_TIME[1:0] = 01b		2.2		µs
		DEG_TIME[1:0] = 10b		3.2		µs
		DEG_TIME[1:0] = 11b		5.4		µs
Thermal Warning Threshold				140		°C
Thermal Shutdown Threshold				160		°C
Thermal Hysteresis				15		°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Typical Performance Curves

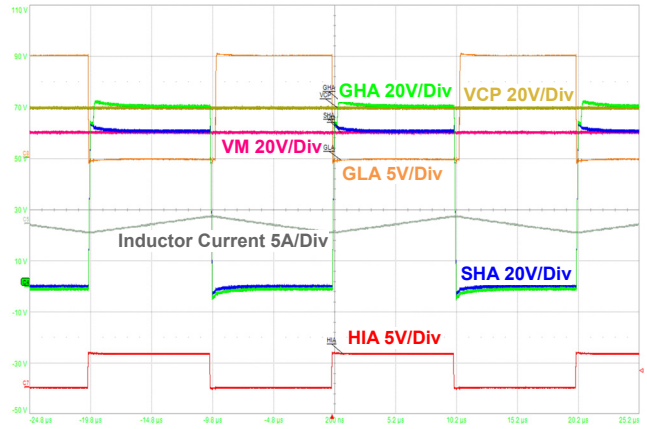


Figure 7. Phase A Driver Switching - No Load, PWM Mode

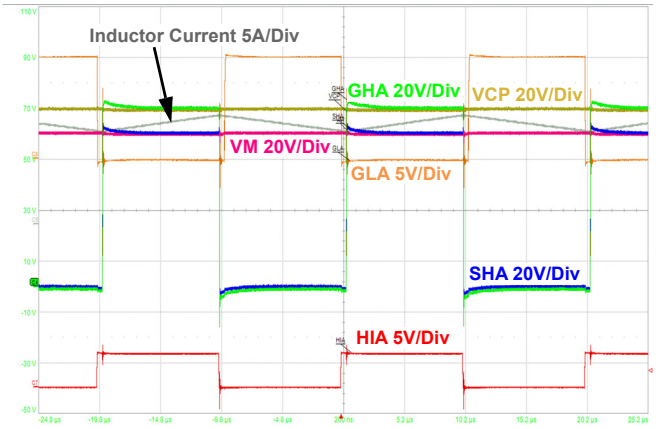


Figure 8. Phase A Driver Switching - 10A Load PWM Mode

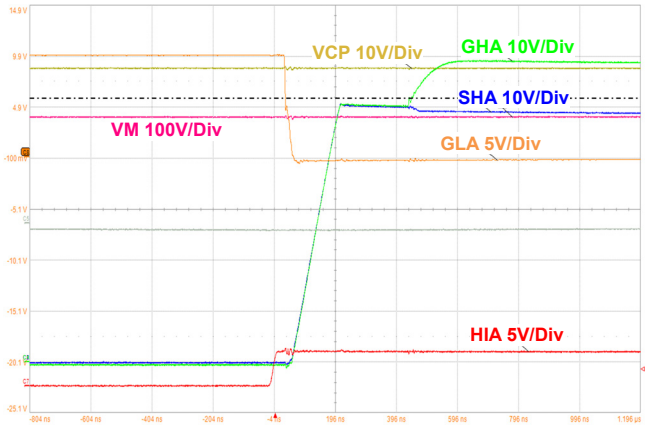


Figure 9. Phase A Driver - No Load HS Turn ON

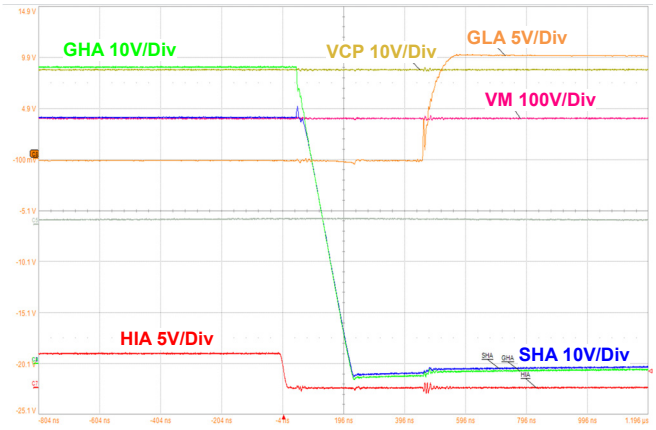


Figure 10. Phase A Driver - No Load HS Turn OFF

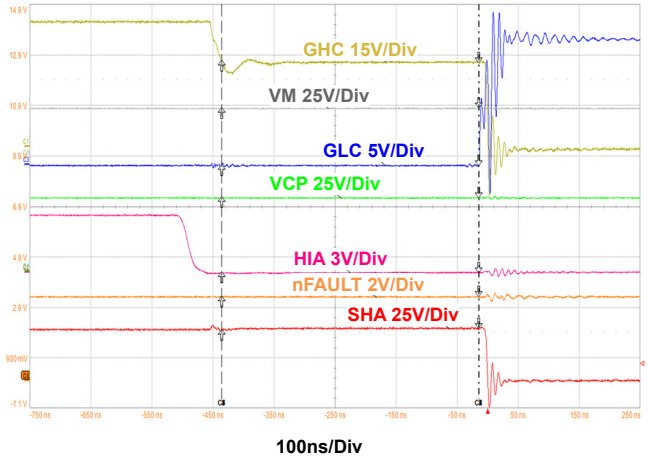


Figure 11. Phase C Driver 421ns Dead Time

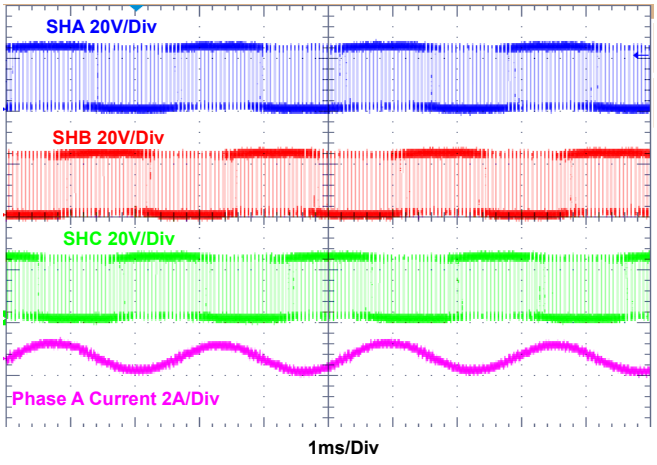


Figure 12. BLDC Motor Commutation with FOC, VM = 24V

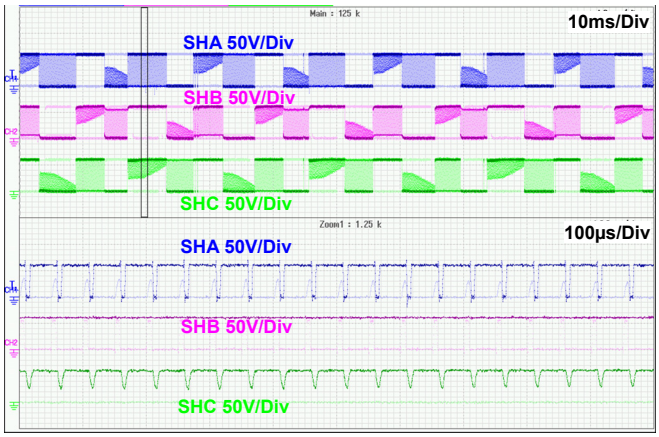


Figure 13. BLDC Motor Commutation with 120° Driving, VM = 60V

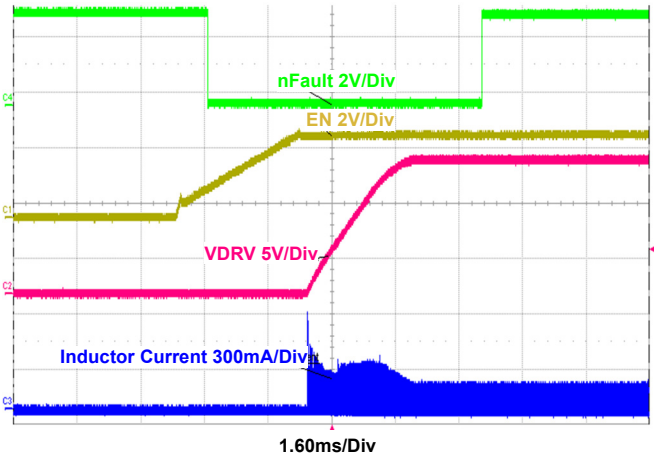


Figure 14. Buck-Boost Regulator Start-Up without Load, VM = 36V

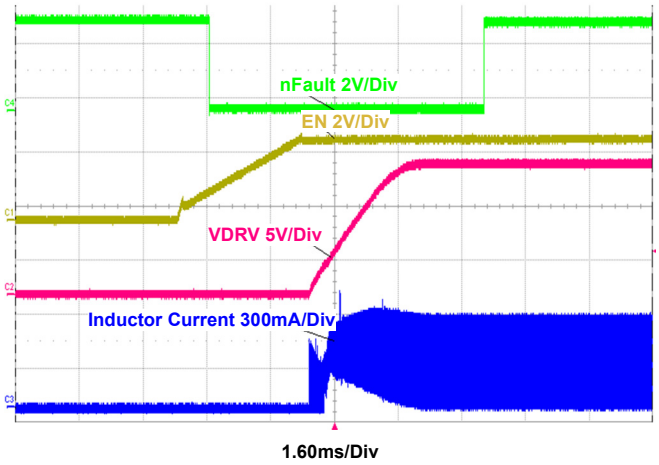


Figure 15. Buck-Boost Regulator Start-Up with 250mA Load, VM = 36V

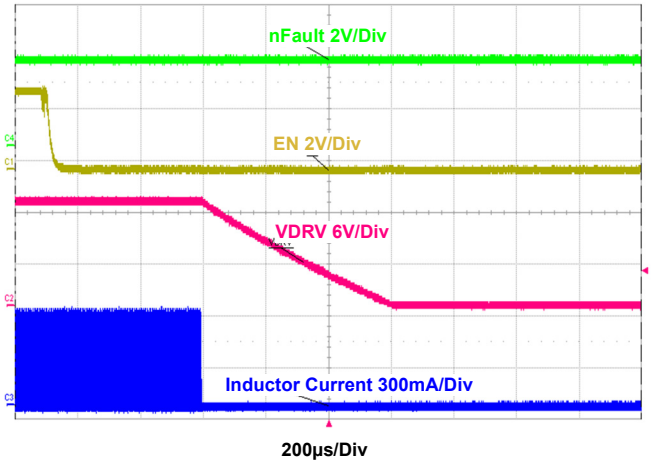


Figure 16. Buck-Boost Regulator Shutdown at 250mA Load, VM = 60V

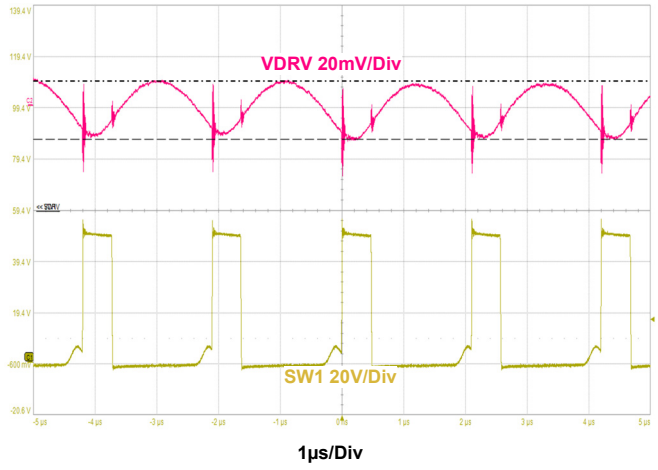


Figure 17. Buck-Boost Regulator Ripple with 200mA Load, VM = 48V

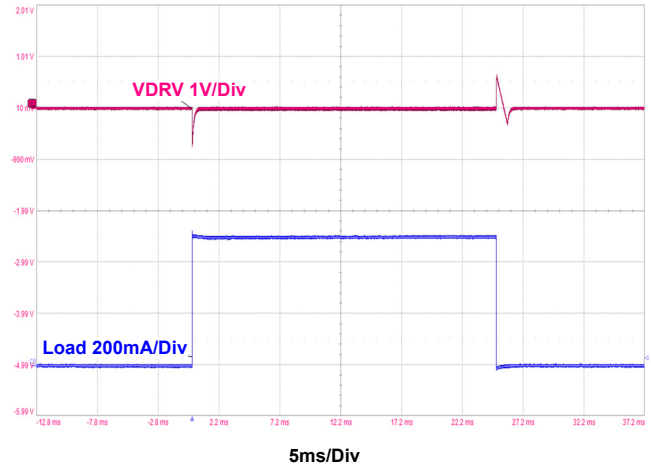


Figure 18. Buck-Boost Regulator 500mA Load Transient, VM = 48V

5. Functional Description

5.1 Modes of Operation and Power-On Sequence

The device contains four modes of operation:

- Shutdown mode
- Sleep mode
- Operating mode
- Fault Management mode

5.1.1 Definitions of State of Different Modes

- **Shutdown mode:** This mode represents the state where VCC voltage is below the POR falling threshold (typical 3.6V). In this state, all other internal functional blocks are disabled except for LDO1. LDO1 keeps powering the VCC rail until VM drops further below 1.2V. 200mA LDO3 is Off but a clamp circuit supplies AUXVCC directly sourced from VCC.
- **Sleep mode:** The RAA227063 is in low-power Sleep mode when VCC is above the POR rising threshold VCC_POR (typical 4.0V) and EN is low. In this mode, the driver output is disabled and ignores any control input on LI/HI pins. The power chain associated with the buck-boost regulator (buck-boost, charge pump, LDO2) is disabled. LDO1 and LDO3 (if FBLDO is connected normally) are kept alive. This minimizes the IC power consumption in Sleep mode.
- **Operating mode:** This mode represents the state when VCC is above the POR rising threshold VCC_POR (typical 4.0V) and EN is pulled high. The RAA227063 is put into normal operation, high-efficiency buck-boost regulator power chain (Buck-boost, charge pump, LDO2) is enabled, and LDO1 is disabled. Driver output is enabled in response to control inputs on the LI/HI pins. No occurrence of any fault is required in this mode.
- **Fault Management mode:** This mode represents the state after any fault occurs. The Smart driver reacts to fault conditions (see Fault Management for detailed responses) and reports the fault status to the MCU using the nFault pin and through the SPI interface. In this mode, the functioning of blocks depends on the fault source.

5.1.2 Mode Transition

The mode transition conditions (A to J) are summarized in Table 1.

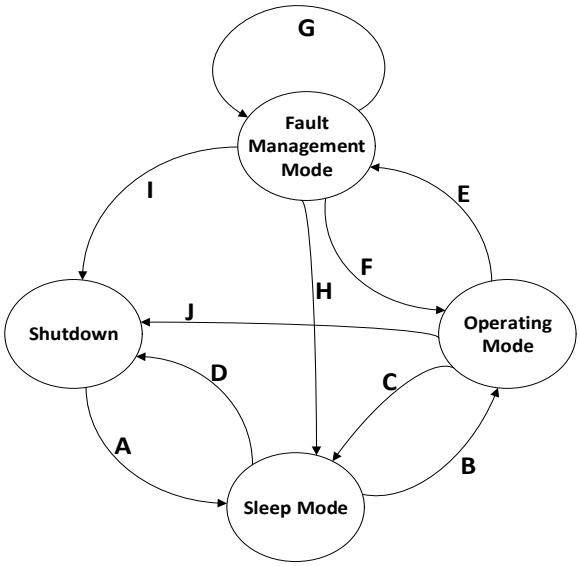


Figure 19. Mode Transition State Machine

Table 1. Mode Transition Conditions

Transition	Exiting Mode	Entering Mode	Conditions	Actions
A	Shutdown	Sleep	VM Rising and VCC goes above VCC_POR (VCC > VCC_POR)	Entering sleep mode after device startup delay. Most of the function blocks are disabled except for main LDO1 and AUXVCC LDO3
B	Sleep	Operating	EN goes high and stays	Enable all function blocks. Device enters normal operation after wake up delay (t_{wake})
C	Operating	Sleep	EN goes low and stays	Disable most of the function blocks except for main LDO1 and AUXVCC LDO3 in low power mode. Device enters sleep mode after sleep entry delay (t_{sleep})
D	Sleep	Shutdown	VM falling and VCC goes below VCC_POR - hys	Disable most of the function blocks except for main LDO1 and AUXVCC LDO3 in low power mode. Enter shutdown mode after shutdown delay.
E	Operating	Fault Management	Any fault condition occurs	Respond based on fault management matrix
F	Fault Management	Operating	Fault condition clears and operating recovers based on fault management matrix	Enable all function blocks. Device enters normal operation after fault recovery delay (t_{ftrcvr})
G	Fault Management	Fault Management	Any other fault condition occurs	Respond based on fault management matrix; each function block disabling signal (active low) from multiple fault sources are ANDed together
H	Fault Management	Sleep	EN is low	Disable most of the function blocks except for main LDO1 and AUXVCC LDO3. Device enters sleep mode after fault recovery delay (t_{ftrcvr})
I	Fault Management	Shutdown	VM falling and VCC goes below VCC_POR - hys	Disable most of the function blocks except for main LDO1 and AUXVCC LDO3 in low power mode. Enter shutdown mode after shutdown delay (t_{shdn})
J	Operating	Shutdown	VM falling and VCC goes below VCC_POR - hys	Disable most of the function blocks except for main LDO1 and AUXVCC LDO3 in low power mode

5.1.3 Modes of Operation

5.1.3.1 Gate Driver Control Modes

When the device is put into Operating mode, the gate driver sets its output state based on the control signal present on HIx and LIx pins. Two gate driver control modes are available:

- 3-phase HI/LI modes
- 3-phase PWM modes

Detailed descriptions and logic truth tables are listed in the following 3-phase HI/LI Mode and 3-phase PWM Mode sections.

5.1.3.2 3-phase HI/LI Mode

In this mode, HIx and LIx inputs serve as control inputs for each individual driver output, logic active high. This mode is enabled by pulling MODE/SDO pin to SGND. For each phase, the HI input signal controls the high-side driver output GHx directly, while the LI input signal controls the low-side driver output GLx directly. See Table 2.

Table 2. 3-phase HI/LI Mode Truth Table

HIx	LIx	GHx - SHx	GLx	SHx
0	0	Low	Low	Hi-Z
0	1	Low	High	Low
1	0	High	Low	High
1	1	Low	Low	Hi-Z

5.1.3.3 3-phase PWM Mode

This mode is enabled by pulling the MODE/SDO pin to VCC or logic high level. In this mode, LIx serves as the enable (logic high)/disable (logic low) of the driver output of each bridge. HIx serves as control input for each bridge. See Table 3.

Table 3. 3-phase PWM Mode Truth Table

HIx	LIx	GHx - SHx	GLx	SHx
X	0	Low	Low	Hi-Z
0	1	Low	High	Low
1	1	High	Low	High

5.1.4 Gate Driver Structure and Feature

5.1.4.1 Driver Structure

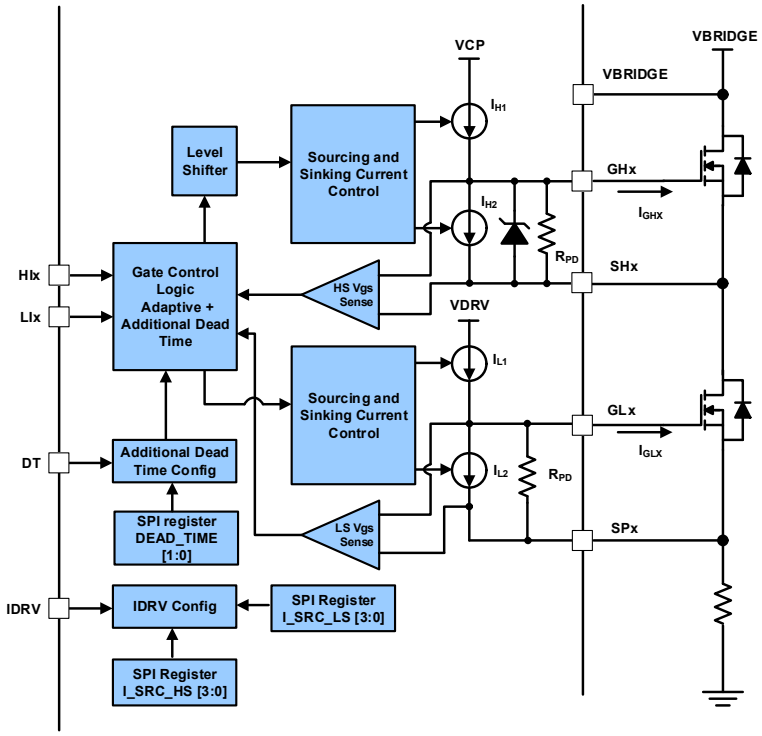


Figure 20. Driver Structure

5.1.4.2 Adjustable Slew-Rate

The smart gate driver architecture allows for the accurate setting of the gate drive source (I_{src}) and sink current (I_{snk}). It is helpful to more accurately control and adjust the slew-rate of switch node voltage, which is beneficial for radiated emission optimization, controlling the reverse recovery of the body diode, and avoiding dV/dt induced shoot-through. For all gate driver outputs, 8 levels of sourcing/sinking current can be supported through the IDRV pin if hardware interface is used, or 16 levels can be supported through the SPI interface. The configurable range is from 50mA to 1.1A for sourcing and 130mA to 2.4A for sinking. **Important:** Pay attention to phase node negative voltage spikes during gate switching. Select a slew rate that keeps the SHx pin negative voltage peak within the specification (-5V). An external protection circuit such as diode resistor clamp between the SHx pin and the motor phase is strongly recommended for reducing negative spikes. **Note:** Configuring using the hardware interface (IDRV pin) sets the source current for both high-side and low-side drivers to be the same value. However, if configuring using the SPI interface, the device can set the source current of high-side and low-side drivers separately. In both configuration cases, the driver sink current is automatically set to be double the source current.

The maximum duration of driver peak source/sink current (gate transition time (t_{gt})), can also be configured to ensure the MOSFET turns on fully. This gate transition time is 1µs by default (for both hardware and SPI interfaces) and can be configured to four levels of options (0.5µs, 1µs, 2µs, 4µs) only through the SPI interface.

5.1.4.3 Driver Robustness Enhancement

Strong sinking current to avoid CdV/dt induced cross-conduction

Additionally, within the same bridge phase, whenever one of the gate drivers is during gate transition of turning on or turning off the corresponding external MOSFET, the complementary gate driver performs a strong sinking current (I_{snk_strg}) to avoid dV/dt induced cross-conduction. The maximum duration of the strong sinking current is also equal to gate transition time (t_{gt}).

Active pull-up/pull-down current to hold gate state

Out of gate transition periods, the driver actively imposes weaker current to hold the gate state. A pull-up current (I_{pu}) is sourced out of the driver to maintain a high output voltage, whereas a pull-down sinking current (I_{pd}) is imposed to maintain nearly zero output voltage.

Adaptive dead time control plus configurable additional dead time

Adaptive dead time control is implemented by actively monitoring the gate of the MOSFET that is turning off first during the transition. The complementary MOSFET is allowed to start turning on only after it drops below the threshold (1V typical). In additional to adaptive dead time, you can add extra dead time (t_{dt}) by setting either through DT/IFSEL/BEN pin in hardware interface mode or through SPI interface DEAD_TIME[0:1] bits.

Note: The t_{gt} value is defined as maximum gate transition time because in real applications, actual gate transition must be shorter than the t_{gt} setting in order to properly drive the MOSFETs. Therefore, the duration of driver peak source/sink current can get terminated before reaching the full t_{gt} duration. For example, during the turn off transition, after V_{gs} drops below the adaptive dead time threshold, peak sink current and the complementary MOSFET gate strong sinking current are terminated, which is earlier than the elapse of t_{gt}. For the turning-on transition, because there is no detection of V_{gs} reaching high level, peak source current and complementary MOSFET gate strong sinking current sustain a full t_{gt} duration, assuming it is sufficiently long on time. Other instances involve the short on-time or off-time.

5.1.4.4 Gate Drive Diagram

Gate drive scheme in 3-phase PWM mode (Figure 21): The MODE/SDO pins need to be tied to logic high to enable this mode. The MODE/SDO state is latched during the internal logic initialization after VCC POR. LIx serves as enable/disable of the driver output of each phase.

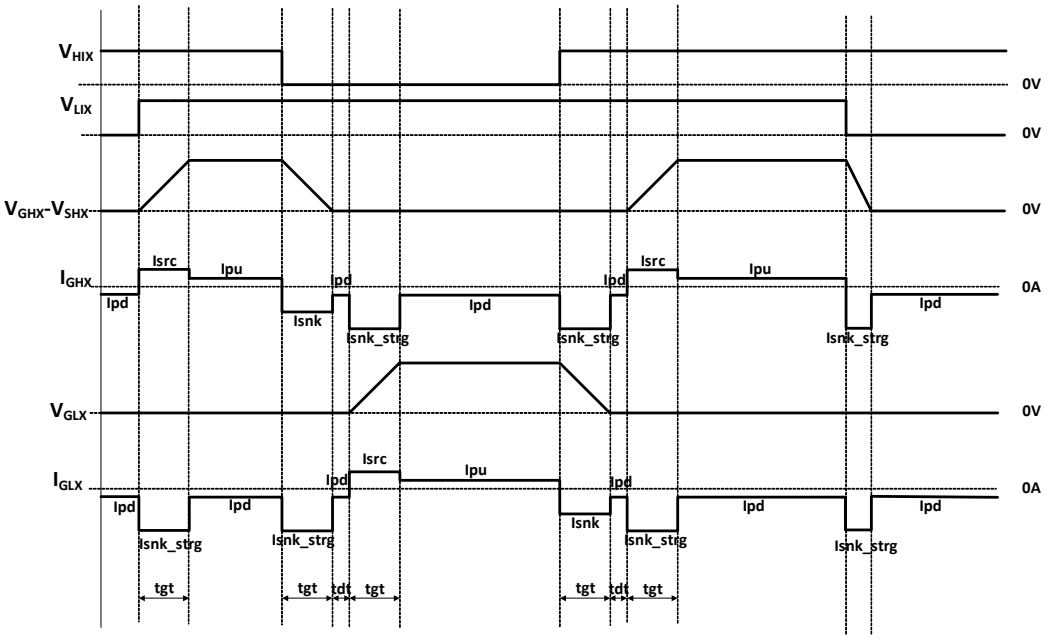


Figure 21. Gate Drive Timing in 3-phase PWM Mode

5.1.4.5 Gate Drive Scheme in 3-phase HI/LI Mode

If HI/LI inserted dead time is relatively short (shorter than the gate transition time plus dead time set):

- During high-side MOSFET turn-off/low-side MOSFET turn-on transition, if LIx asserts high before the GHx-SHx high-to-low transition time (t_{gt}) and dead time (t_{dt}, based on DT pin setting) ends.
- During low-side MOSFET turn-off / high-side MOSFET turn-on transition, if HIx asserts high before the GLx high-to-low transition time (t_{gt}) and dead time (t_{dt}, based on DT pin setting) ends.
- Total effective dead time is adaptive dead time plus dead time setting (see Figure 22).

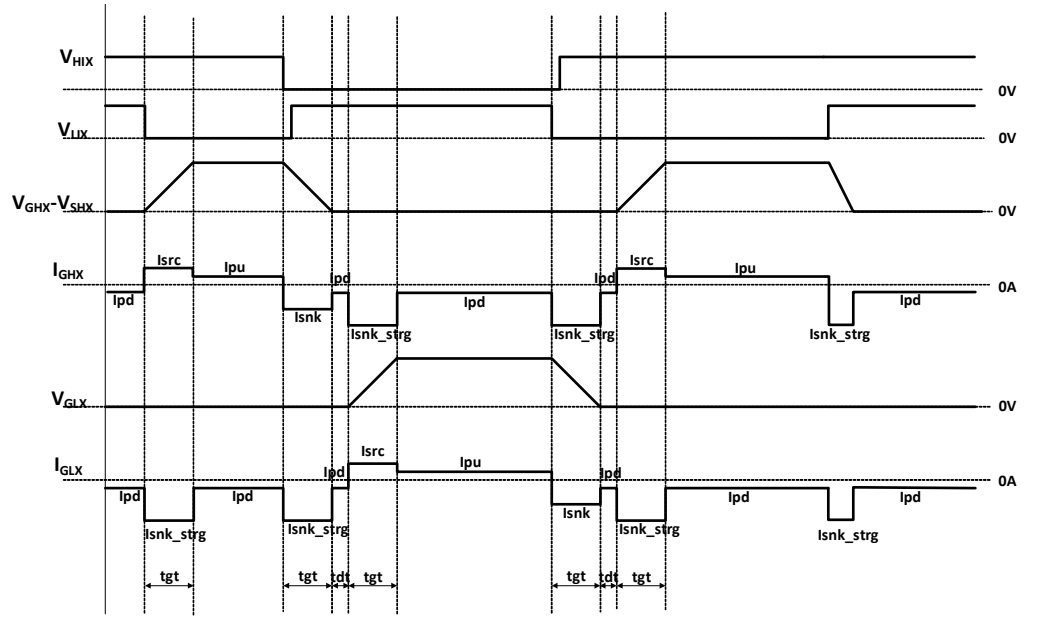


Figure 22. Gate Drive Timing in 3-phase HI/LI Mode with Short HI/LI Inserted Dead Time

If the HI/LI inserted dead time is relatively long (longer than gate transition time plus dead time set), that is:

- During high-side MOSFET turn-off/low-side MOSFET turn-on transition, if LIx asserts high after the GHx-SHx high-to-low transition time (t_{gt}) and dead time (t_{dt}, based on DT pin setting) ends.
- During low-side MOSFET turn-off/high-side MOSFET turn-on transition, if HIx asserts high after the GLx high-to-low transition time (t_{gt}) and dead time (t_{dt}, based on DT pin setting) ends.
- Total effective dead time is equal to the dead time introduced by the HI/LI signal (see Figure 23).

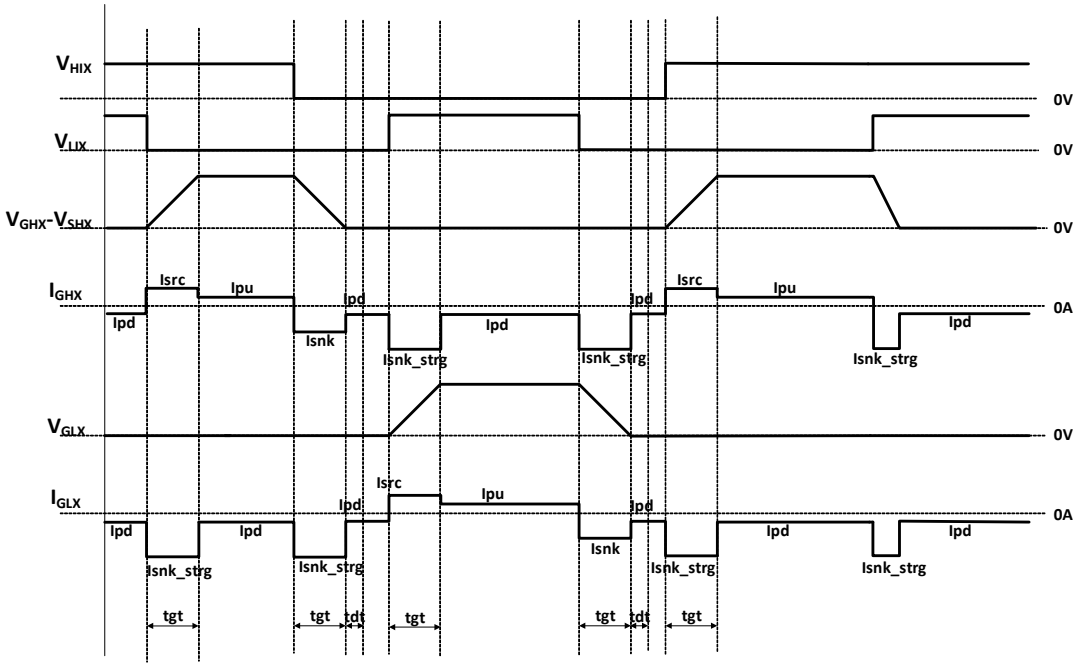
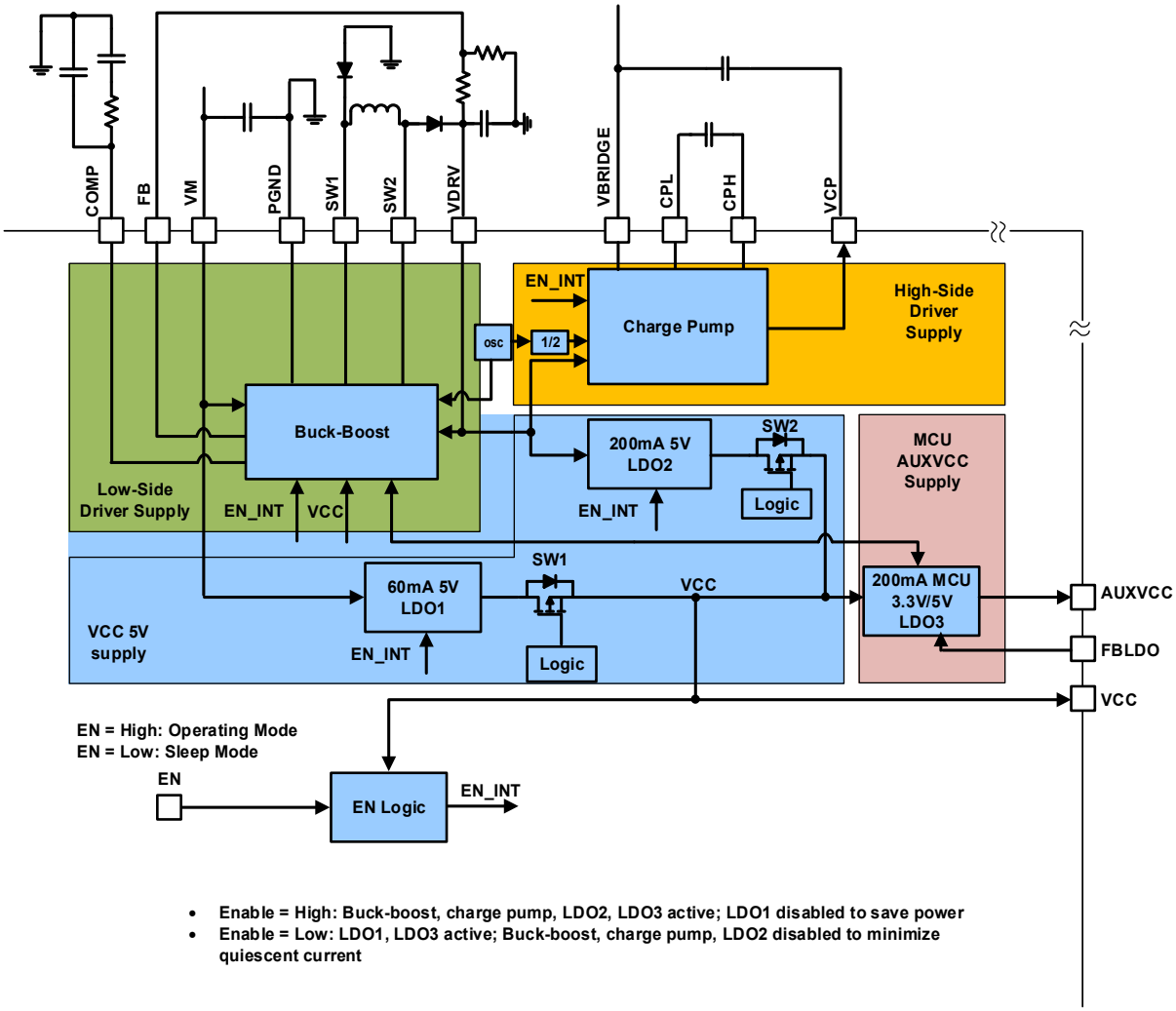


Figure 23. Gate Drive Timing in 3-phase HI/LI Mode with Long HI/LI Inserted Dead Time

5.1.5 Power Architecture

5.1.5.1 Power Architecture Overview



Note: VM and VBRIDGE are shorted inside the IC. VM and VBRIDGE sourcing current at device power-up without any load includes Operating Supply Current I_{DDO}, VREF input current, and Buck-Boost regulator Operating Source Current I_{DDO_BB}.

Figure 24. Power Architecture

Table 4. Power Block Status at Different Modes

Mode	Buck-Boost	Charge Pump	60mA 5V LDO1	200mA 5V LDO2	200mA MCU LDO3
Shutdown[1]	Off	Off	On	Off	Off
Sleep	Off	Off	On	Off	On but in Low Power mode
Operating	On	On	Off	On	On
Fault Management	Reaction based on fault management response				

1. In Shutdown mode, 200mA LDO3 is off but a clamp circuit supplies AUXVCC directly sourced from VCC with clamp voltage at 3.5V.

5.1.5.2 Low-Side Driver Supply (VDRV)

Low-side driver supply (VDRV) is generated by a 500mA buck-boost switching regulator fed from VM. VDRV adjustable range is from 5V to 15V. The buck-boost regulator integrates a 900mΩ high voltage (65V) PMOS as a buck-side control switch, a 600mΩ low voltage (25V) NMOS as a boost-side control switch, and the corresponding gate driver. It also integrates all the control circuitry and logic to achieve a peak current mode control scheme. Both buck-side and boost-side freewheeling diodes and inductor need to be placed externally. Regulator switching frequency is 500kHz, with a two-level peak current limit at 1.4A (cycle-by-cycle current limit) and 1.6A (peak OCP threshold). The regulator output is monitored and protected from OV and UV conditions. Under medium or high load conditions, the regulator runs in CCM mode. However, under light-load conditions, it can run in DCM mode because of the nature of asynchronous rectification. Moreover, in the case of high VM low VDRV operation in light load, it can run in Pulse Skipping mode because of the minimum on-time limitation.

To further improve the efficiency at high VM, the regulator is designed to work in Buck mode only when VM-VDRV > ~2V. When VM-VDRV < ~2V-hysteresis, the regulator enters Buck-Boost mode by starting the boost switch, where the on-time undergoes a soft-start process: starting from minimum on-time, increasing over ~70µs, and eventually matching the buck switch phase and duty. Similarly, exiting from Buck-Boost mode to Buck mode when VM-VDRV goes back above 2V involves a soft-off process for the boost switch over 1ms. These ensure smooth transitions.

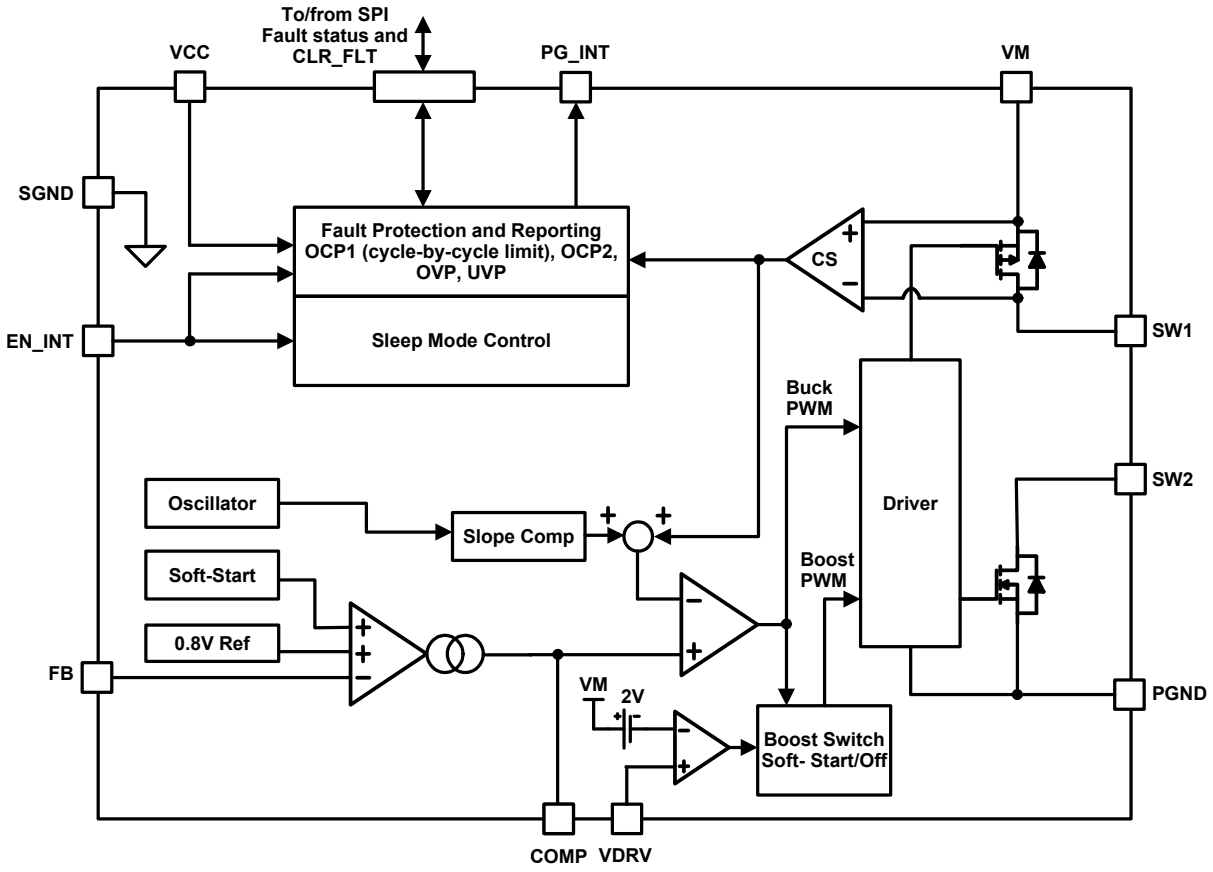


Figure 25. Buck-Boost Regulator Block Diagram

5.1.5.3 Charge Pump

This high voltage charge pump generates a steady high-side driver supply rail at the level VBRIDGE+VDRV. The CPL pin switches between VDRV and PGND by complementary switches Q_1 and Q_2. The CPH pin switches between VBRIDGE and VBRIDGE+VDRV by complementary switches Q_3 and Q_4. Q_1 and Q_4 are turned on and off at the same time, while Q_2 and Q_3 are turned on and off at the same time. In this way, during on-time of Q_2 and Q_3 (off-time of Q_1 and Q_4), the flying capacitor across CPH and CPL C_1 gets charged by VBRIDGE. During on-time of Q_1 and Q_4 (off-time of Q_2 and Q_3), C_2 gets charged up towards VBRIDGE+VDRV by VDRV. From its operation, it can be seen that this charge pump always runs in full mode with minimal power dissipation. The complementary switches operate at 250kHz, which is ½ the internal oscillator frequency used by the buck-boost regulator, and the duty cycle is 50%. The maximum loading target is < 50mA. The charge pump output is monitored and undervoltage protection is implemented.

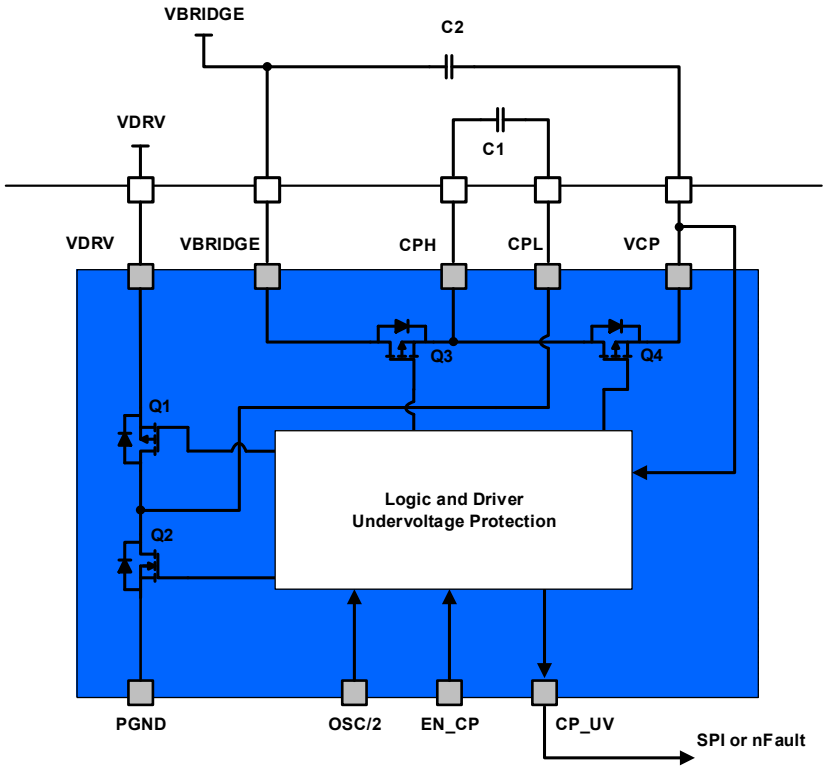


Figure 26. Charge Pump Block Diagram

5.1.5.4 VCC Supply

VCC supply consists of two LDOs:

- **60mA 5V LDO1**: This LDO is a high voltage LDO fed from VM. It is enabled to generate VCC power during device power-up (VCC reaches above rising POR VCC_POR) before buck-boost soft-start is completed during Sleep mode when the buck-boost power chain is disabled. Whenever LDO1 is enabled, SW_1 is also turned on.
  Note: The bandgap reference used in LDO1 is untrimmed.
- **200mA 5V LDO2**: This LDO is a low voltage LDO fed from the buck-boost output. It supplies VCC only in Operating mode after buck-boost soft-up is done. SW2 is on when LDO2 is used.
  Note: The bandgap reference used in LDO2 is trimmed, to achieve better VCC accuracy in Operating mode.

5.1.5.5 MCU AUXVCC Supply

AUXVCC LDO is a 200mA low voltage LDO3 fed from VCC, designed to power the MCU and peripherals in applications as required. It has a dedicated feedback pin (FBLDO) that allows for fine adjustment of output voltage, ranging from 1.2V to VCC (slightly lower). The internal reference is 1.2V. The output voltage is tightly regulated during normal Operating mode. During device Sleep mode, LDO3 also enters a low-power mode with its output voltage set to 3.5V and with not-so-tight regulation. Larger feedback resistance (R_1 plus R_2) leads to smaller Sleep mode current, but generally should stay below 1.5MΩ. One option for minimizing Sleep mode current is to use a circuit to disconnect the R_2 in sleep mode.

When the MCU is operating at low AUXVCC configuration below 2V, pay attention to the signal level communicating to the device. Use an external pull-up circuit if necessary to ensure meeting the logic level requirement of the device.

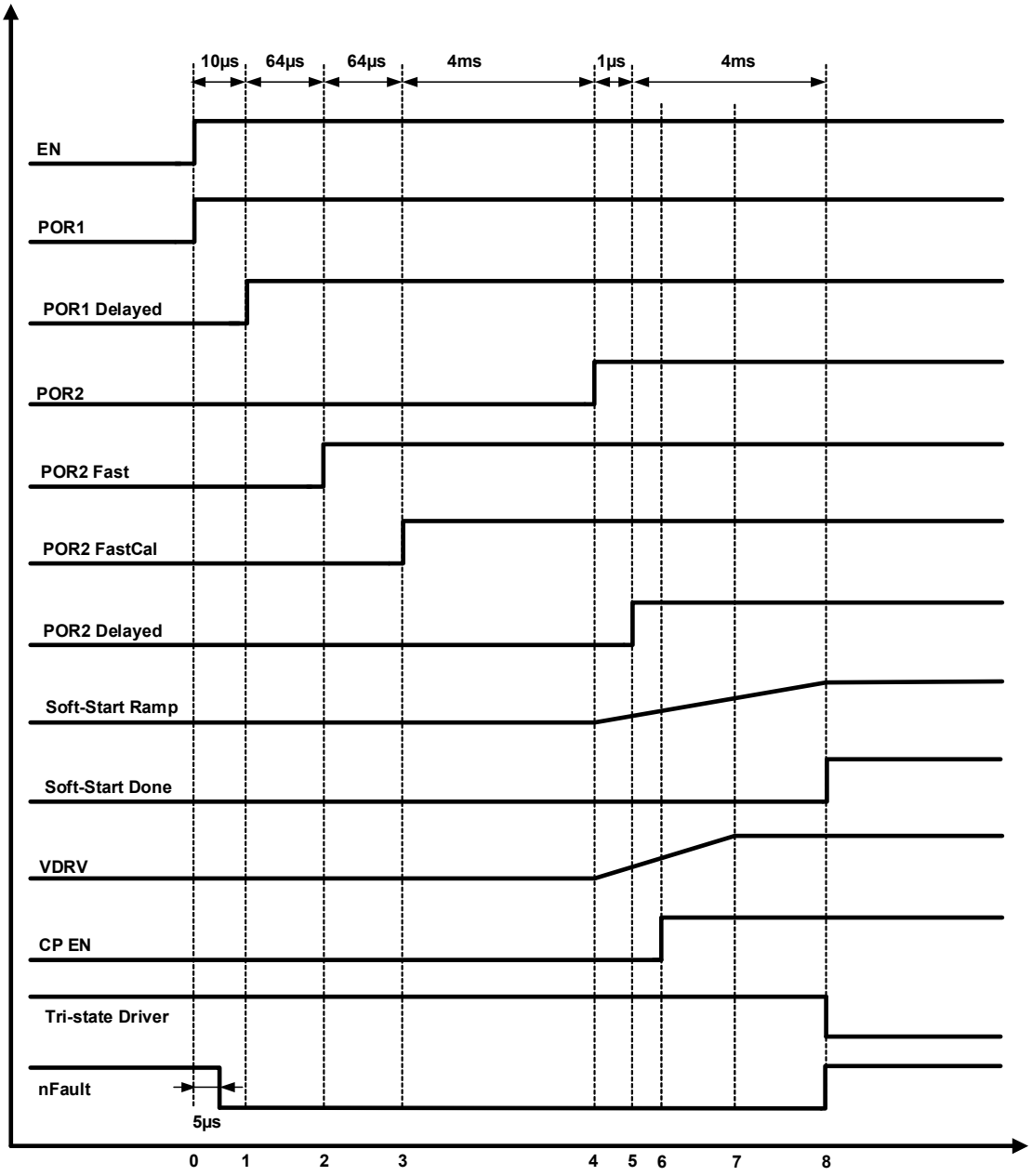
(EQ. 1) $$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right)$$

where:

- V_{REF} = 1.2V
- R_1 = High-side resistor divider
- R_2 = Low-side resistor connected from FBLDO to SGN

5.1.6 Power-On Sequence

The VCC and AUXVCC of the IC are turned on automatically when VM is applied, even before EN goes high. See VCC Supply and MCU AUXVCC Supply for details about VCC and AUXVCC. After EN goes high, the IC internally goes through POR1, POR2, and soft-start process to charge pump enable, VDRV and driver output ready. Figure 27 shows the internal power-on enabling sequence of the IC.



1. POR1 Delayed:
   - Start the oscillator
2. POR2 Fast:
   - Start sensing the levels from HW pins
   - Detect SPI_EN mode
3. POR2 FastCal:
   - Start sense Amp Calibration
4. POR2:
   - Latch the HW sense levels
   - Start Soft-Start Ramp
5. POR2 Delayed:
   - Turn off HW sense blocks
6. CP EN:
   - Enable Charge Pump when VDRV reaches threshold (4.6V if operating VDRV is 10V)
7. VDRV Ramp Done:
   - Regulate VDRV at operating voltage when Soft-Start Ramp reaches 0.8V
8. Soft-Start Done:
   - End tri-stating driver output when Soft-Start Ramp reaches 1.5V
   - Ensure VM, VBRIDGE, VDRV, and CP are settled without fault and start operating the driver
   - nFault goes high if there's no fault condition

* Timing label not in scale for better illustration

Figure 27. Power-On Sequence

5.2 Fault Management

5.2.1 Fault Conditions Types

The following are the fault conditions/sources supported by the device:

- VCC undervoltage
- VM/VBRIDGE undervoltage
- Charge pump undervoltage
- MOSFET VDS overcurrent
- Shunt current sense overcurrent
- Thermal warning
- Thermal shutdown
- Buck-boost overcurrent limiting (OC1)
- Buck-boost overcurrent protection (OC2)
- Buck-boost undervoltage
- Buck-boost overvoltage

Table 5. Fault Management Matrix[1][2][3]

Fault Type	Condition	Default & Program Options	Exit Mode	Enter Mode	Driver CTRL Input	Driver Outputs	60mA 5V LDO1	Buck-Boost Reg.	Charge Pump	200mA 5V LDO2	200mA MCU LDO3	Core Logic	nFault Pin	SPI STTS Bit	Recovery Condition	Recovery Action (Table 6)
VCC UV	VCC < VCC_ POR - hys (3.6V)	Default	Sleep; Fault Mgmt.; operating	SHDN	BLKD	Keep all driver output low	EN	Dis	Dis	Dis	EN in low power mode (if FBLDO is tied to divider)	Dis	N/A	N/A	VCC rises above VCC_POR (typ. 4.0V)	Device resumes operation Auto. Device exits SHDN mode, entering sleep mode.
VM UV	VM < VM_ UVLO (typ. 3.9V)	Default	Oprt Fault Mgmt.	Fault Mgmt.	BLKD	Keep all driver output low	EN	Dis	Dis	Dis	EN (if FBLDO is tied to divider)	EN	Pull low	Set	VM rises above UVLO + hys (typ. 4.2V)	A1

Table 5. Fault Management Matrix[1][2][3] (Cont.)

Fault Type	Condition	Default & Program Options	Exit Mode	Enter Mode	Driver CTRL Input	Driver Outputs	60mA 5V LDO1	Buck-Boost Reg.	Charge Pump	200mA 5V LDO2	200mA MCU LDO3	Core Logic	nFault Pin	SPI STTS Bit	Recovery Condition	Recovery Action (Table 6)
Charge pump UV	VCP - VBRIDGE < VCP_UV (0.55* VDRV)	Default	Oprt Fault Mgmt.	Fault Mgmt.	BLKD	Keep all driver output low	Dis	EN	EN	EN	EN (if FBLDO is tied to divider)	EN	Pull low	Set	VCP - VBRIDGE rises above VCP_UV+ hys (0.55*VDRV)	A2
		Option: report status only	Oprt Fault Mgmt.	Stays in Orgnl mode	Keep behavior in Orgnl mode	Keep behavior in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	EN	Pull low	Set	VCP- VBRIDGE rises above VCP_UV + hys (0.55*VDRV)	D
MOSFET VDS OCP	VDS > VDS_TH	Default	Oprt	Fault Mgmt.	BLKD	Keep all driver output low	Dis	EN	EN	EN	EN (if FBLDO is tied to divider)	EN	Pull low	Set	N/A	B
		Option#1: Auto retry	Oprt	Fault Mgmt.	BLKD	Keep all driver output low	Dis	EN	EN	EN	EN (if FBLDO is tied to divider)	EN	Pull low	Set	Retry after RETRY_DELAY_ VDSOCP	C
		Option#2: report status only	Oprt	Fault Mgmt.	Keep behavior in Orgnl mode	Keep behavior in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	EN	Pull low	Set	VDS < VDS_TH	D
		Option#3: no action	Oprt	Oprt	Keep behavior in Orgnl mode	Keep behavior in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	EN	Keep state in Orgnl mode	Set	N/A	N/A

Table 5. Fault Management Matrix[1][2][3] (Cont.)

Fault Type	Condition	Default & Program Options	Exit Mode	Enter Mode	Driver CTRL Input	Driver Outputs	60mA 5V LDO1	Buck-Boost Reg.	Charge Pump	200mA 5V LDO2	200mA MCU LDO3	Core Logic	nFault Pin	SPI STTS Bit	Recovery Condition	Recovery Action (Table 6)
Shunt OCP	SPx -SNx > CSOCP _TH	Default	Oprt	Fault Mgmt.	BLKD	Keep all driver output low	Dis	EN	EN	EN	EN (if FBLDO is tied to divider)	EN	Pull low	Set	N/A	B
		Option#1: Auto retry	Oprt	Fault Mgmt.	BLKD	Keep all driver output low	Dis	EN	EN	EN	EN (if FBLDO is tied to divider)	EN	Pull low	Set	Retry after RETRY_DELAY_ CSOCP	C
		Option#2: report status only	Oprt	Fault Mgmt.	Keep behavior in Orgnl mode	Keep behavior in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	EN	Pull low	Set	SPx-SNx < CSOCP_ TH - hys	D
		Option#3: no action	Oprt	Oprt	Keep behavior in Orgnl mode	Keep behavior in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	EN	Keep state in Orgnl mode	Set	N/A	N/A
Thermal warning	Tj > T_{OTW}	Default	Oprt; Fault Mgmt.	Stays in Orgnl mode	Keep behavior in Orgnl mode	Keep behavior in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	EN	Pull low	Set	Tj < T_{OTW} - hys	E
		Option: only report through SPI status bit	Oprt; Fault Mgmt.	Stays in Orgnl mode	Keep behavior in Orgnl mode	Keep behavior in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	Keep state in Orgnl mode	EN	Keep state in Orgnl mode	Set	Tj < T_{OTW} - hys	F
Thermal SHDN	Tj > T_{OTP}	Default	Oprt; Fault Mgmt.	Fault Mgmt.	BLKD	Keep all driver output low	EN	Dis	Dis	Dis	EN (if FBLDO is tied to divider)	EN	Pull low	Set	Tj < T_{OTP} - hys	A2

Table 5. Fault Management Matrix[1][2][3] (Cont.)

Fault Type	Condition	Default & Program Options	Exit Mode	Enter Mode	Driver CTRL Input	Driver Outputs	60mA 5V LDO1	Buck-Boost Reg.	Charge Pump	200mA 5V LDO2	200mA MCU LDO3	Core Logic	nFault Pin	SPI STTS Bit	Recovery Condition	Recovery Action (Table 6)
Buck-boost OC1	$I_L > I_{OC1}$ (1.4A)	Default	Oprt; Fault Mgmt.	Fault Mgmt.	Keep behavior in Orgnl mode	Keep behavior in Orgnl mode	Dis	EN	EN	EN	EN (if FBLDO is tied to divider)	EN	Keep state in Orgnl mode	N/A	N/A	N/A
Buck-boost OC2	$I_L > I_{OC2}$ (1.6A)	Default	Oprt; Fault Mgmt.	Fault Mgmt.	BLKD	Keep all driver output low	EN	Hiccup	Dis	Dis	EN (if FBLDO is tied to divider)	EN	Pull low	Set	Buck-boost soft-start is done and $I_L < I_{OC2}$ (1.6A)	A2
Buck-boost UV	VDRV < 0.8 * $V_{out\_nominal}$ ($V_{FB} < 0.8*V_{REF}$)	Default	Oprt; Fault Mgmt.	Fault Mgmt.	BLKD	Keep all driver output low	EN	Hiccup	Dis	Dis	EN (if FBLDO is tied to divider)	EN	Pull low	Set	Buck-boost soft-start is done and VDRV > 0.8 * $V_{out\_nominal}$ + hys ($V_{FB} > 0.8*V_{REF}$ + hys)	A2
Buck-boost OV	VDRV>1.2 * $V_{out\_nominal}$ ($V_{FB} > 1.2*V_{REF}$)	Default	Oprt; fault Mgmt.	Fault Mgmt.	BLKD	Keep all driver output low	Dis	Dis	EN	EN	EN (if FBLDO is tied to divider)	EN	Pull low	Set	VDRV < 1.2 * $V_{out\_nominal}$ - hys ($V_{FB} < 1.2*V_{REF}$ - hys)	A2

1. Pulling EN low for longer than 1ms forces the device into sleep mode, which overrides all actions except for VCC UV.
2. ~2% hysteresis is applied to avoid chatter.
3. The following are abbreviations in the table. EN: Enabled, Dis: Disabled, Mgmt: Management, Orgnl: Original, Oprt: Operating, STTS: Status, BLKD: Blocked, CTRL: Control, Auto: automatically

Table 6. Recovery Actions[1]

A1	A2	B	C	D	E	F
Applies where nFault clears automatically, but driver input/outputs and status bit need to be recovered by EN low pulse or setting clear fault bit		**Applies to the case where nFault, driver input/outputs and status bit all need to be recovered by EN low pulse or setting clear fault bit**	**Applies to OCP automatically retry option**	**Applies to the cases where only report status in nFault and SPI is needed**	**Applies only thermal warning**	**Applies only thermal warning**
Device enters operating mode by going through necessary power rails soft-start firstly	Driver control inputs are still blocked and driver outputs are still kept low, until the rising edge of EN low pulse or SPI clear fault bit is set. The EN low pulse rising edge or setting SPI clear fault bit also reset the all fault status bits	Driver control inputs are still blocked and driver outputs are still kept low, until the rising edge of EN low pulse or SPI clear fault bit is set. The EN low pulse rising edge or setting SPI clear fault bit also reset the all fault status bits and nFault	Driver control inputs are still blocked and driver outputs are still kept low, until the expiration of retry delay period. The delay period expiration also releases nFault and reset fault status bit	nFault pin is latched. Requires a reset by CLR_FLT bit or an EN pin low pulse and fault condition clearance to be released high.	nFault pin is released high and SPI OTW status bit is reset automatically if power rails soft-start is done and there is no other fault present. Keep all other actions uninterrupted.	SPI OTW status bit is reset automatically if power rails soft-start is done and there is no other fault present. Keep all other actions uninterrupted.

1. EN low pulse width required for fault recovery is minimum10µs, typical 20µs, amd maximum 200µs.

5.2.2 nFAULT Indicator

The nFault pin (open-drain configuration) is the fault indicator. It is pulled low if any of the fault conditions occur. It is pulled high when all the fault conditions are removed and all chip power rail start-ups are done. nFault is latched only for VDS OCP and VSEN OCP. Toggling the EN signal, or setting CLR_FLT = 1 in control register 1 pulls the nFAULT high (if the fault is removed). There is about 1µs deglitch time on the nFAULT pin.

This signal notifies the MCU after any fault occurs, so the MCU can stop normal operation and enter the fault handling routine. It also informs the MCU when all fault conditions are removed and all necessary power rails are properly up, so the MCU can re-enter the normal operating routine.

5.3 Current Sensing and BEMF Sensing

5.3.1 Overview

The device supports both ground-side shunt current sense and low-side $r_{DS(ON)}$ current sense. There are three differential amplifiers (CSA, CSB, CSC) that can separately support current sensing up to three phases.
Important: In applications that current sensing is not used, it is necessary to short unused sensing signal inputs (SPx and SNx) to the low-side MOSFET power ground, and leave the outputs (CSOx) floating.

Regarding BEMF (Back Electromotive Force) sensing, the Phase C current sense amplifier (CSC) and another two dedicated amplifiers (A1, A2) form the BEMF sensing signal chain. The motor BEMF is the voltage induced on the stator coil when there is relative motion between the rotor permanent magnets and the stator coil. This voltage can detect rotor position without the need for an encoder or hall sensor cost savings. In a typical trapezoidal BLDC operation, only two-phase bridges are energized at a given time. The third phase is in high impedance state (both high-side and low-side MOSFETs are turned off). By sensing this phase node voltage and subtracting the motor center tap voltage from it, provides you the BEMF induced in this 3rd phase stator coil, which allows you to know/estimate the rotor position relative to this 3rd phase. The point of interest is the zero-crossing of the BEMF, which is approximately halfway through one commutation period if the motor is running at a constant speed with no phase advance.

The device has multiple amplifiers integrated to allow flexible configurations to support current sensing and BEMF sensing. Additionally, samples and holds of internally sensed signals can also be configured. However, there are limitations on different feature combinations; see Figure 28 and Table 7 for all the supported sensing configurations.

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Table 7. Current and BEMF Sensing Configurations

Config. Number	BEMF Sensing	Current Sensing	CS S/H	BEMF S/H	Descriptions	Configuration Setup
1	Enabled	Shunt Sense	Enabled	Enabled	Supports BEMF and up to two-phase current sensing. All these three signals are automatically S/H internally; MUXed out through one buffer	Can only be set if SPI is enabled; DT/IFSEL/BEN = tied to VCC; BEMF_EN = 1b; CS_MODE = 0b; CS_SH_EN = 1b; BEMF_SH_EN = 1b;
2	Enabled	Shunt Sense	Enabled	Disabled	Supports BEMF and up to two-phase current sensing. Only current sense signal is automatically S/H internally; BEMF and current sense is MUXed out through one buffer	Can only be set if SPI is enabled; DT/IFSEL/BEN = tied to VCC; BEMF_EN = 1b; CS_MODE = 0b; CS_SH_EN = 1b; BEMF_SH_EN = 0b

Table 7. Current and BEMF Sensing Configurations (Cont.)

Config. Number	BEMF Sensing	Current Sensing	CS S/H	BEMF S/H	Descriptions	Configuration Setup
3	Enabled	Shunt Sense	Disabled	Enabled	Supports BEMF and up to two-phase current sensing. Only BEMF sense signal automatically S/H internally; BEMF and current sense is MUXed out through one buffer	Can only be set if SPI is enabled; DT/IFSEL/BEN = tied to VCC; BEMF_EN = 1b; CS_MODE = 0b; CS_SH_EN = 0b; BEMF_SH_EN = 1b
4	Enabled	Shunt Sense	Disabled	Disabled	Supports BEMF and up to two-phase current sensing. No internal S/H, sensed signals are output continuously	Can be set through both HW and SPI I/F; HW I/F: Set through MODE/SDO and DT/IFSEL/BEN pins; SPI I/F: DT/IFSEL/BEN = tied to VCC BEMF_EN = 1b; CS_MODE = 0b CS_SH_EN = 0b BEMF_SH_EN = 0b
5	Disabled	Shunt Sense	Enabled	N/A	Supports up to 3-phase current sensing All current sense signals are automatically S/H internally and MUXed out through one buffer.	Can only be set if SPI is enabled; DT/IFSEL/BEN = tied to VCC BEMF_EN = 0b; CS_MODE = 0b CS_SH_EN = 1b
6	Disabled	Shunt Sense	Disabled	N/A	Supports up to 3-phase current sensing. No internal S/H, sensed signals are output continuously	Can be set through both HW and SPI I/F; HW I/F: Set through MODE/SDO and DT/IFSEL/BEN pins; SPI I/F: DT/IFSEL/BEN = tied to VCC BEMF_EN = 0b; CS_MODE = 0b CS_SH_EN = 0b
7	Disabled	$r_{DS(ON)}$ Sense	Disabled	N/A	Supports up to 3-phase low-side $r_{DS(ON)}$ sensing. Sensing only when corresponding low-side MOSFET is on No internal S/H, output signal is continuous	Can be set through both HW and SPI I/F; HW I/F: Set through MODE/SDO and DT/IFSEL/BEN pins; SPI I/F: DT/IFSEL/BEN = tied to VCC BEMF_EN = 0b; CS_MODE = 1b CS_SH_EN = 0b
8	Enabled	$r_{DS(ON)}$ Sense	Disabled	Disabled	Supports BEMF and up to two-phase current sensing. No internal S/H, sensed signals are output continuously	Can be set through both HW and SPI I/F; HW I/F: Set through MODE/SDO and DT/IFSEL/BEN pins; SPI I/F: DT/IFSEL/BEN = tied to VCC BEMF_EN = 1b; CS_MODE = 1b
9	Enabled	Shunt Sense	Enabled	Enabled	Supports BEMF sense and Phase A current sense. BEMF comparator, BEMF S/H signal and current sense S/H signal are output	Can be set through SPI. SPI I/F: DT/IFSEL/BEN = tied to VCC BEMF_CMP_MODE = HI

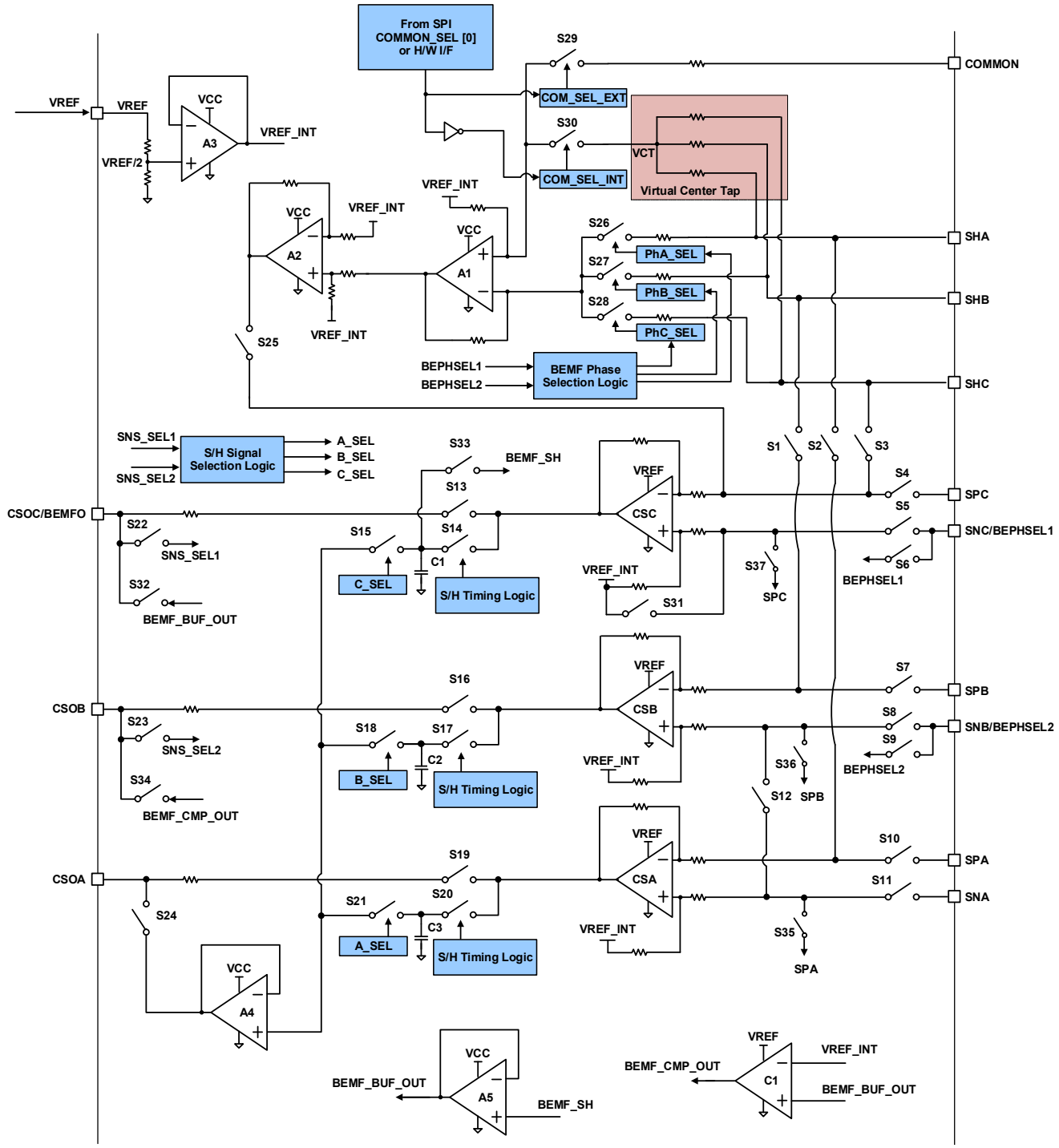


Figure 28. High Level Diagram

5.3.2 Details on Different Sensing Configurations

5.3.2.1 Configuration 1

See the high level diagram in Figure 29. In Configuration 1 (BEMF enabled, shunt current sensing, current sense S/H enabled, BEMF sense S/H enabled), the switches colored in red are on permanently, and the switches in black are off permanently. This allows amplifiers A1, A2, and CSC to sense BEMF, while CSA and CSB amplifiers sense Phase A and B current through shunts. **Note:** SNC/BEPHSEL1 and SNB/BEPHSEL2 pins are used as logic signal inputs for BEMF phase selection. The CSOC/BEMFO and CSOB pins are used as logic signal input pins to determines which S/H signal is to be buffered and output to the CSOA pin.

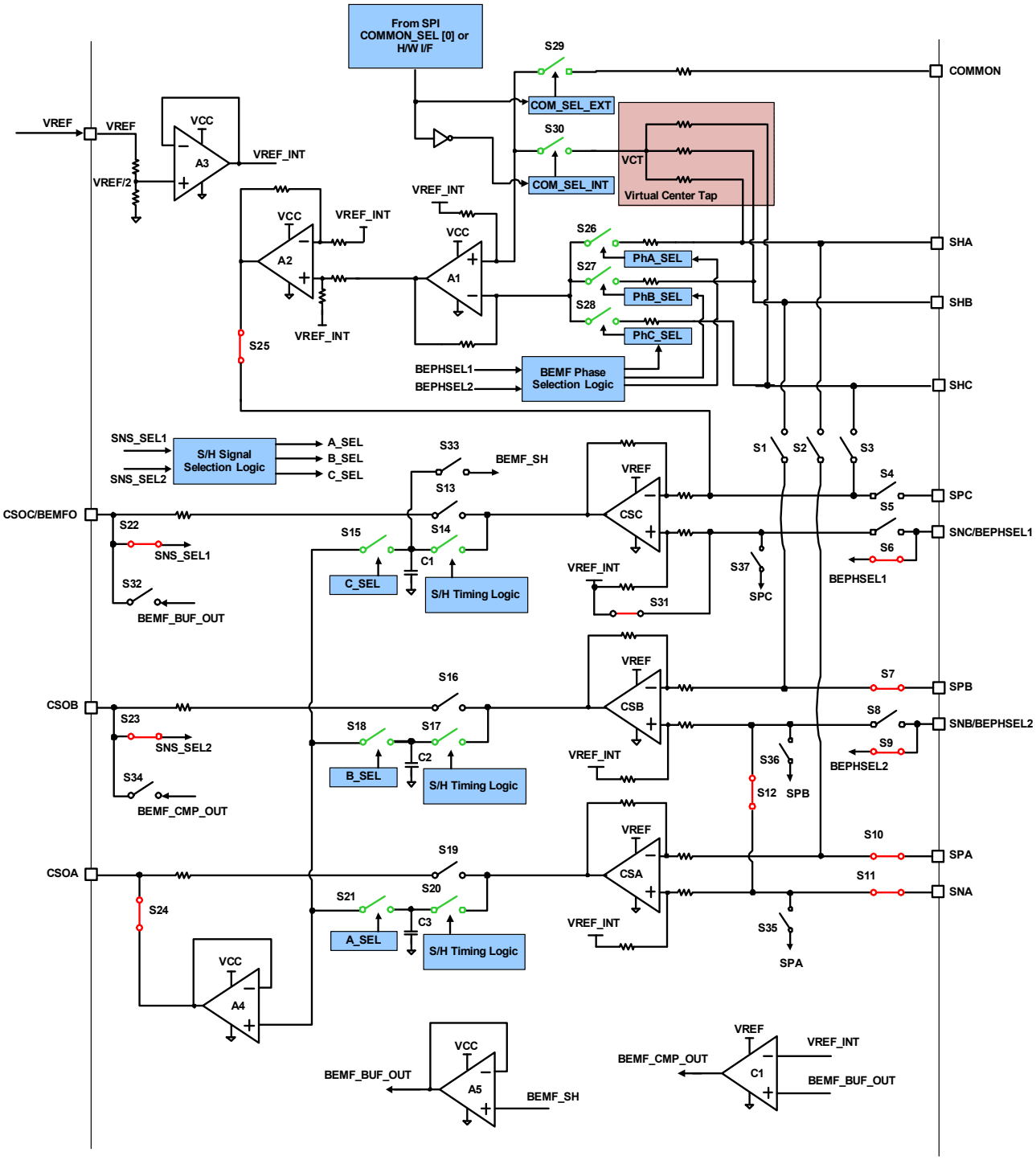


Figure 29. Configuration 1

The CSB amplifier negative input are connected to SNA. It may cause some current sensing error for CSB because of a non-ideal connection. This compensation is made because of limited pins available, if two phase currents need to be sensed in this configuration. If only one shunt current sense is needed, use CSA.

The switches colored in green are turning on and off based on the corresponding logic. For details, see Table 8.

Table 8. Configuration 1

Switch	Description
S29	On if configured to use external motor center tap connection
S30	On if configured to use internal virtual center tap connection
S26	On if BEMF sensing selection phase is Phase A
S27	On if BEMF sensing selection phase is Phase B
S28	On if BEMF sensing selection phase is Phase C
S15	On if selected to buffer the S/H BEMF signal and output to the CSOA pin
S18	On if selected to buffer the S/H sensed shunt voltage from CSB and output to the CSOA pin
S21	On if selected to buffer the S/H sensed shunt voltage from CSA and output to the CSOA pin
S14, S17, S20	These are the S/H switches; their On/Off timing is determined by internal timing logic

5.3.2.2 Configuration 2

See high level diagram in Figure 30. In Configuration 2 (BEMF enabled, shunt current sensing, current sense S/H enabled, BEMF sense S/H disabled), the switches colored in red are on permanently, and the switches in black are off permanently. This allows amplifiers A1, A2, and CSC to sense BEMF, while CSA and CSB amplifiers are used to sense Phase A and B current through shunts. **Note:** SNC/BEPHSEL1 and SNB/BEPHSEL2 pins are used as logic signal inputs for BEMF phase selection. The CSOC/BEMFO and CSOB pins are used as logic signal input pins to determine which sensed signal is to be buffered and output to the CSOA pin.

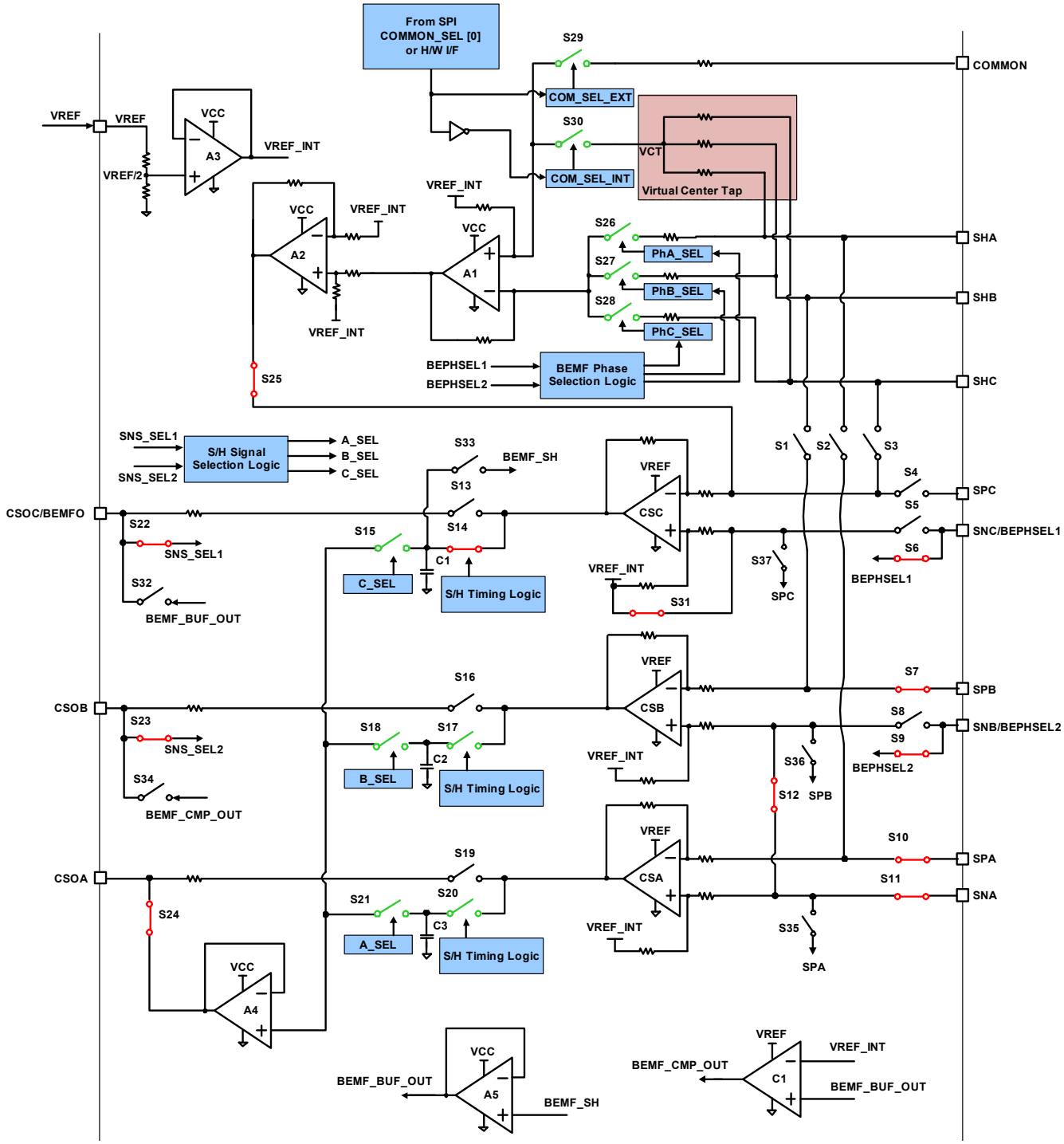


Figure 30. Configuration 2

The CSB amplifier negative input are connected to SNA. It may cause some current sensing error for CSB because of a non-ideal connection. This compensation is made because of limited pins available, if two phase currents need to be sensed in this configuration. If only one shunt current sense is required, use CSA.

The switches colored in green are turning on and off based on the corresponding logic. For details see Table 9.

Table 9. Configuration 2

Switch	Description
S29	On if configured to use external motor center tap connection
S30	On if configured to use internal virtual center tap connection
S26	On if BEMF sensing selection phase is Phase A
S27	On if BEMF sensing selection phase is Phase B
S28	On if BEMF sensing selection phase is Phase C
S15	On if selected to buffer the continuous BEMF signal and output to the CSOA pin
S18	On if selected to buffer the S/H sensed shunt voltage from CSB and output to the CSOA pin
S21	On if selected to buffer the S/H sensed shunt voltage from CSA and output to the CSOA pin
S17, S20	These are the S/H switches; their On/Off timing is determined by internal timing logic

5.3.2.3 Configuration 3

See the high level diagram in Figure 31. In Configuration 3 (BEMF enabled, shunt current sensing, current sense S/H disabled, BEMF sense S/H enabled), the switches colored in red are on permanently, and the switches in black are off permanently. This allows amplifiers A1, A2, and CSC to sense BEMF, while CSA and CSB amplifiers are used to sense Phase A and B current through shunts. **Note:** SNC/BEPHSEL1 and SNB/BEPHSEL2 pins are used as logic signal inputs for BEMF phase selection. The CSOC/BEMFO and CSOB pins are used as logic signal input pins to determine which sensed signal is to be buffered and output to the CSOA pin.

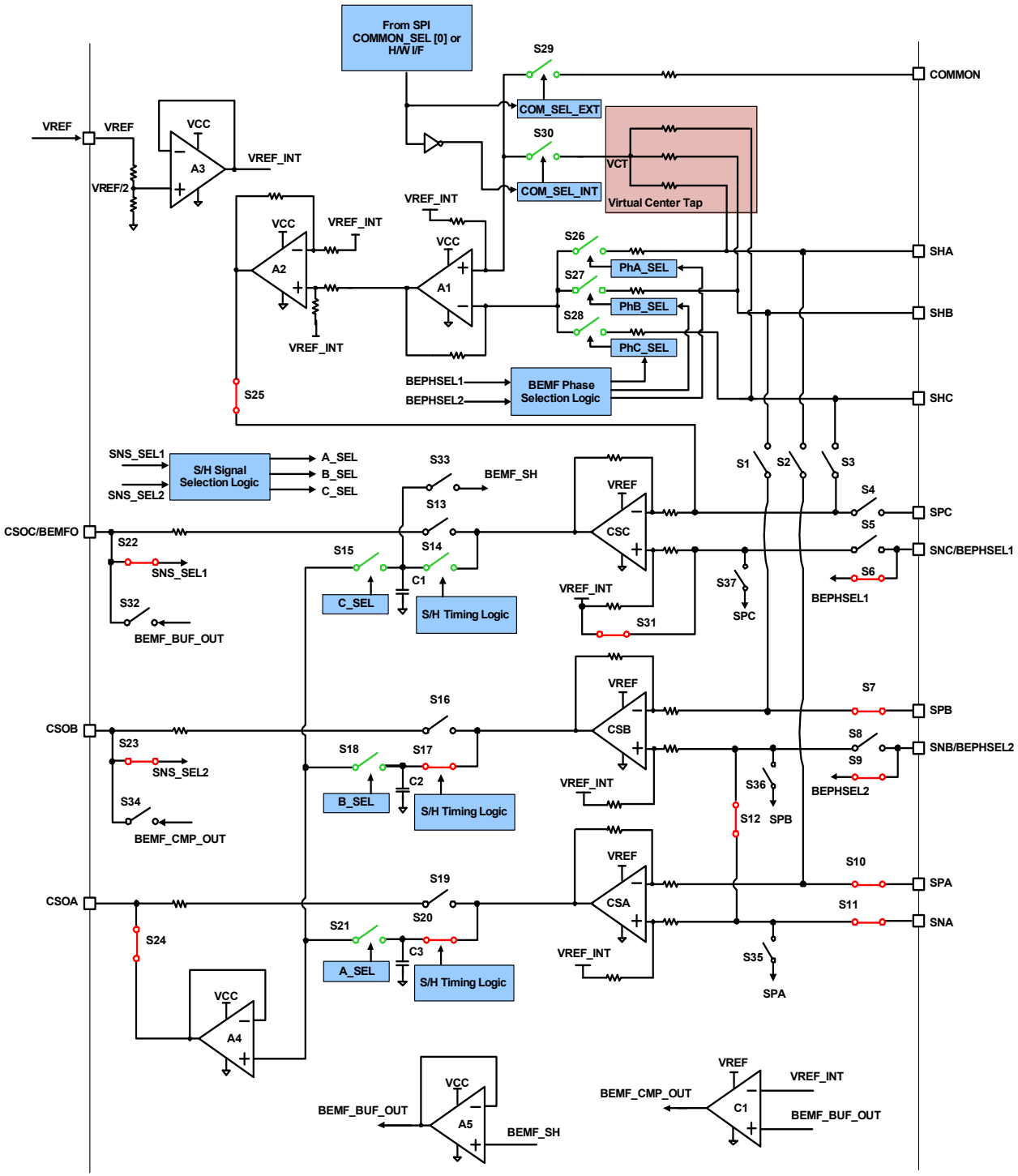


Figure 31. Configuration 3

The CSB amplifier negative input are connected to SNA. It can cause some current sensing error for CSB because of a non-ideal connection. This compensation is made because of limited pins available, if two phase currents need to be sensed in this configuration. If only one shunt current sense is required, use CSA.

The switches colored in green are turning on and off based on the corresponding logic. For details see Table 10

Table 10. Configuration 3

Switch	Description
S29	On if configured to use external motor center tap connection
S30	On if configured to use internal virtual center tap connection
S26	On if BEMF sensing selection phase is Phase A
S27	On if BEMF sensing selection phase is Phase B
S28	On if BEMF sensing selection phase is Phase C
S15	On if selected to buffer the S/H BEMF signal and output to the CSOA pin
S18	On if selected to buffer the continuous sensed shunt voltage from CSB and output to the CSOA pin
S21	On if selected to buffer the continuous sensed shunt voltage from CSA and output to the CSOA pin
S14	These are the S/H switches; their On/Off timing is determined by internal timing logic

5.3.2.4 Configuration 4

See the high level diagram in Figure 32. In Configuration 4 (BEMF enabled, shunt current sensing, current sense S/H disabled, BEMF sense S/H disabled), the switches colored in red are on permanently, and the switches in black are off permanently. This allows amplifiers A1, A2, and CSC to sense BEMF, while CSA and CSB amplifiers are used to sense Phase A and B current through shunts. **Note:** SNC/BEPHSEL1 and SNB/BEPHSEL2 pins are used as logic signal inputs for BEMF phase selection. There are no internal S/H functions in this configuration. Therefore, all three amplifier signal chains pass the sensed signals continuously.

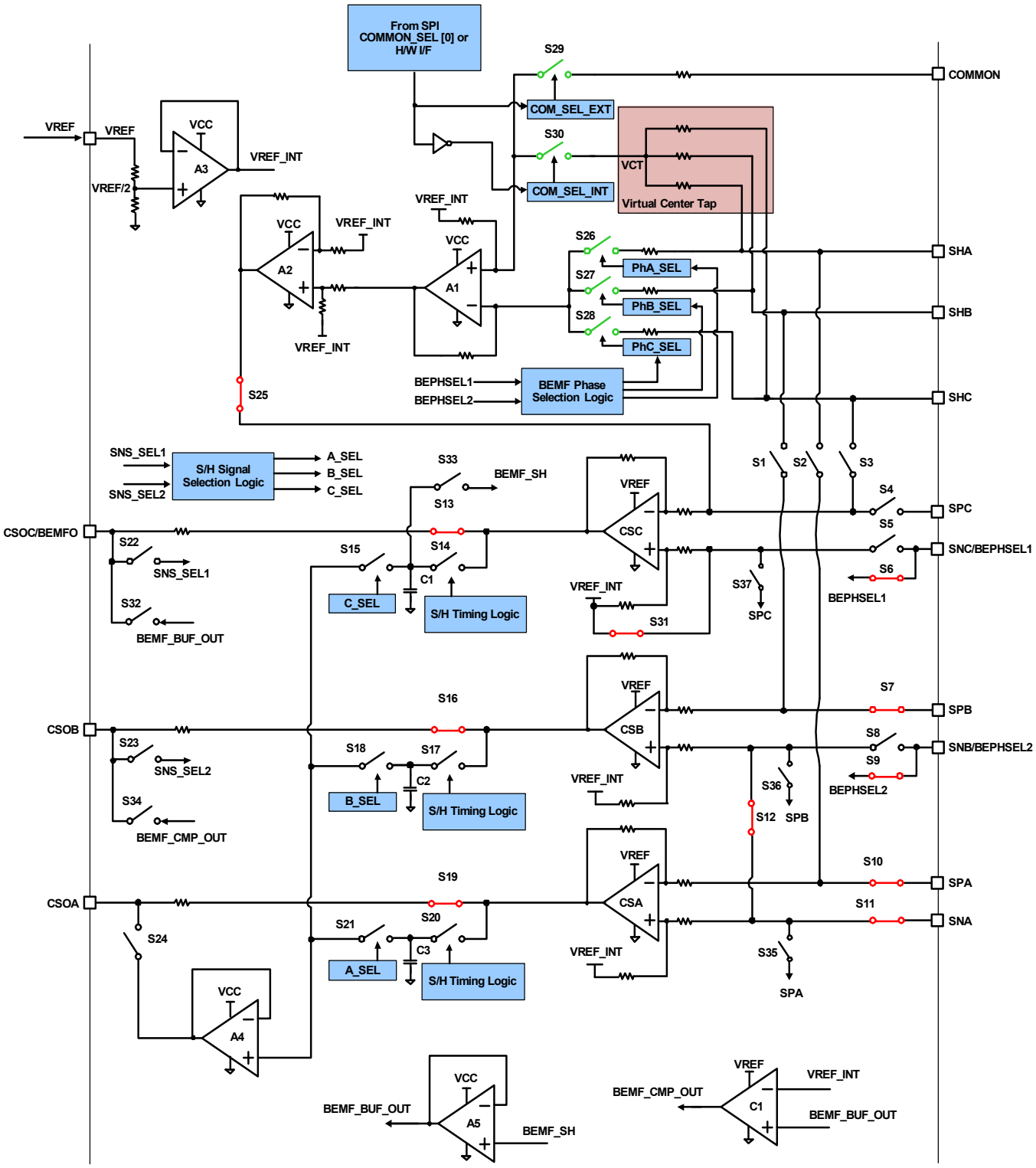


Figure 32. Configuration 4

The CSB amplifier negative input are connected to SNA. It may cause some current sensing error for CSB because of a non-ideal connection. This compensation is made because of the limited pins available, if two phase currents need to be sensed in this configuration. If only one shunt current sense is required, use CSA.

The switches colored in green are turning on and off based on the corresponding logic. For more details, see Table 11.

Table 11. Configuration 4

Switch	Description
S29	On if configured to use external motor center tap connection
S30	On if configured to use internal virtual center tap connection
S26	On if BEMF sensing selection phase is Phase A
S27	On if BEMF sensing selection phase is Phase B
S28	On if BEMF sensing selection phase is Phase C

5.3.2.5 Configuration 5

See the high level diagram in Figure 33. In Configuration 5 (BEMF disabled, shunt current sensing, current sensing S/H enabled), the switches colored in red are on permanently, and the switches in black are off permanently. This allows CSA, CSB, and CSC amplifiers to sense phases A, B, and C current through the shunts. S/H functions are enabled and the CSOC/BEMFO and CSOB pins are used as logic signal input pins to determine the selection which S/H signal is to be buffered and output to the CSOA pin.

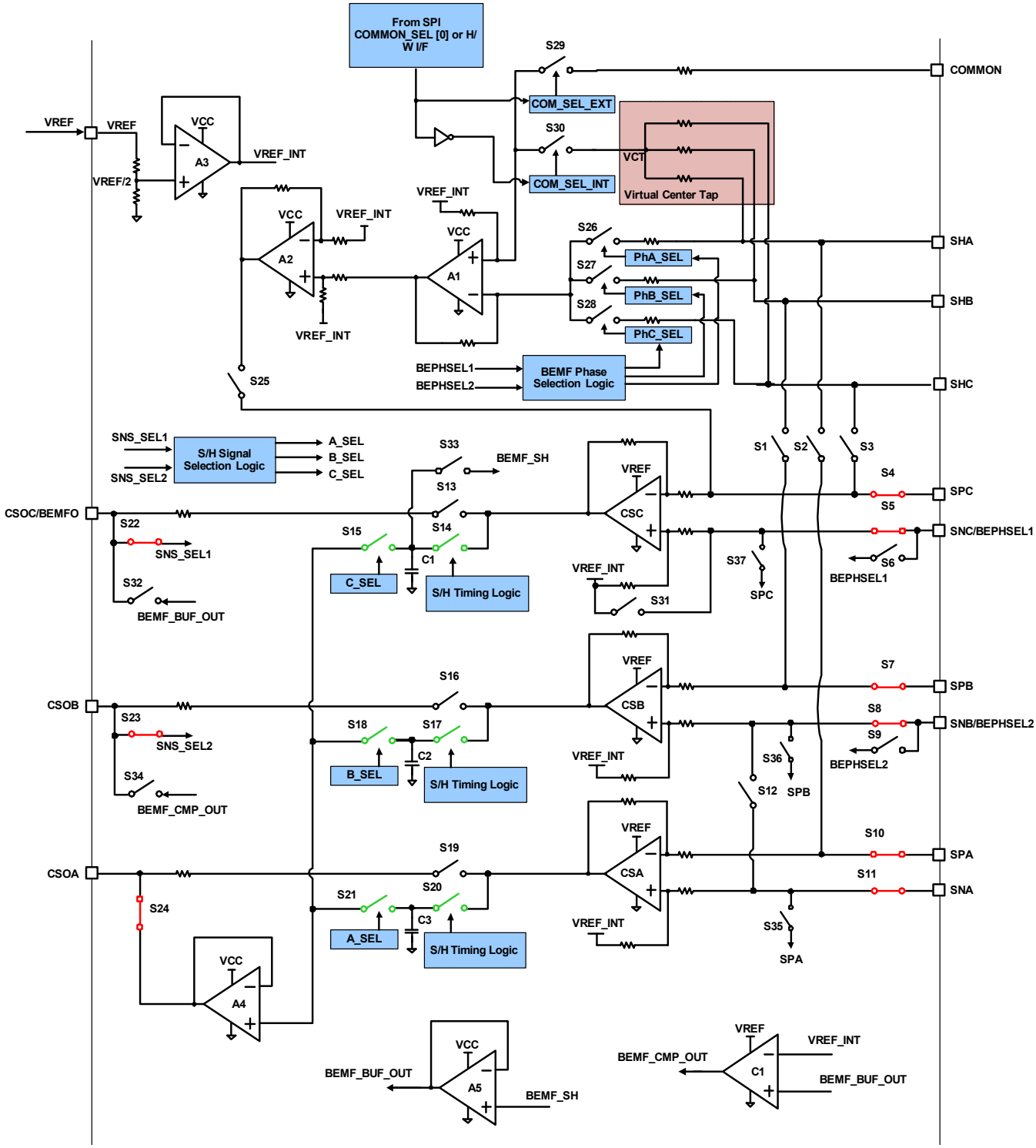


Figure 33. Configuration 5

Table 12. Configuration 5

Switch	Description
S15	On if selected to buffer the S/H sensed shunt voltage from CSC and output to the CSOA pin
S18	On if selected to buffer the S/H sensed shunt voltage from CSB and output to the CSOA pin
S21	On if selected to buffer the S/H sensed shunt voltage from CSA and output to the CSOA pin
S14, S17, S20	These are the S/H switches; their On/Off timing is determined by internal timing logic

5.3.2.6 Configuration 6

See the high level diagram in Figure 34. In Configuration 6 (BEMF disabled, shunt current sensing, current sensing S/H disabled), the switches colored in red are on permanently, and the switches in black are off permanently. This allows CSA, CSB, and CSC amplifiers to sense Phase A, B, and C current through the shunts.

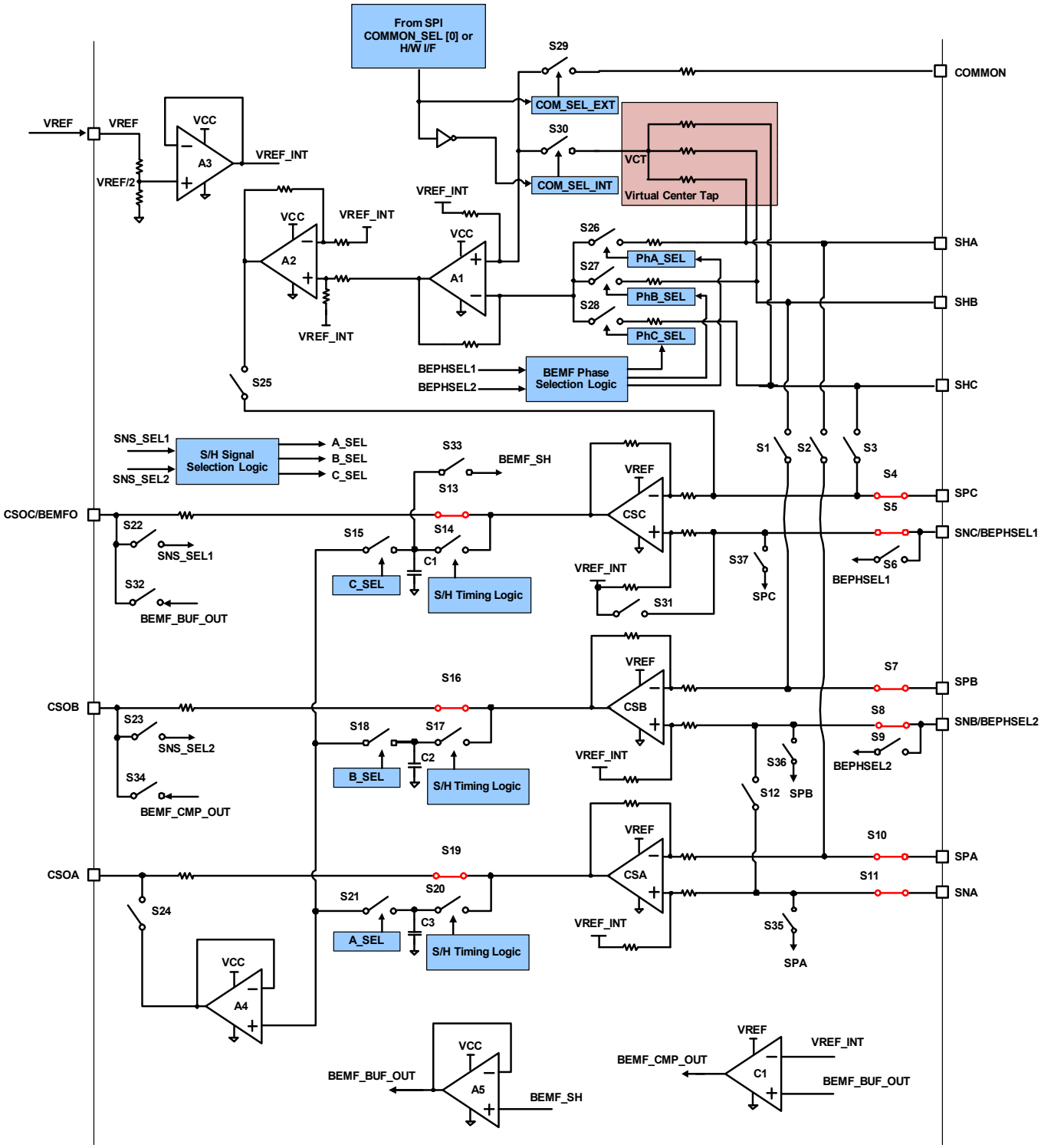


Figure 34. Configuration 6

5.3.2.7 Configuration 7

See the high level diagram in Figure 35. In Configuration 7 (BEMF disabled, $r_{DS(ON)}$ current sensing, current S/H disabled), the switches colored in red are on permanently, and the switches in black are off permanently. This allows CSA, CSB, and CSC amplifiers to sense Phase A, B, and C current through low-side MOSFET VDS drop during their on state.

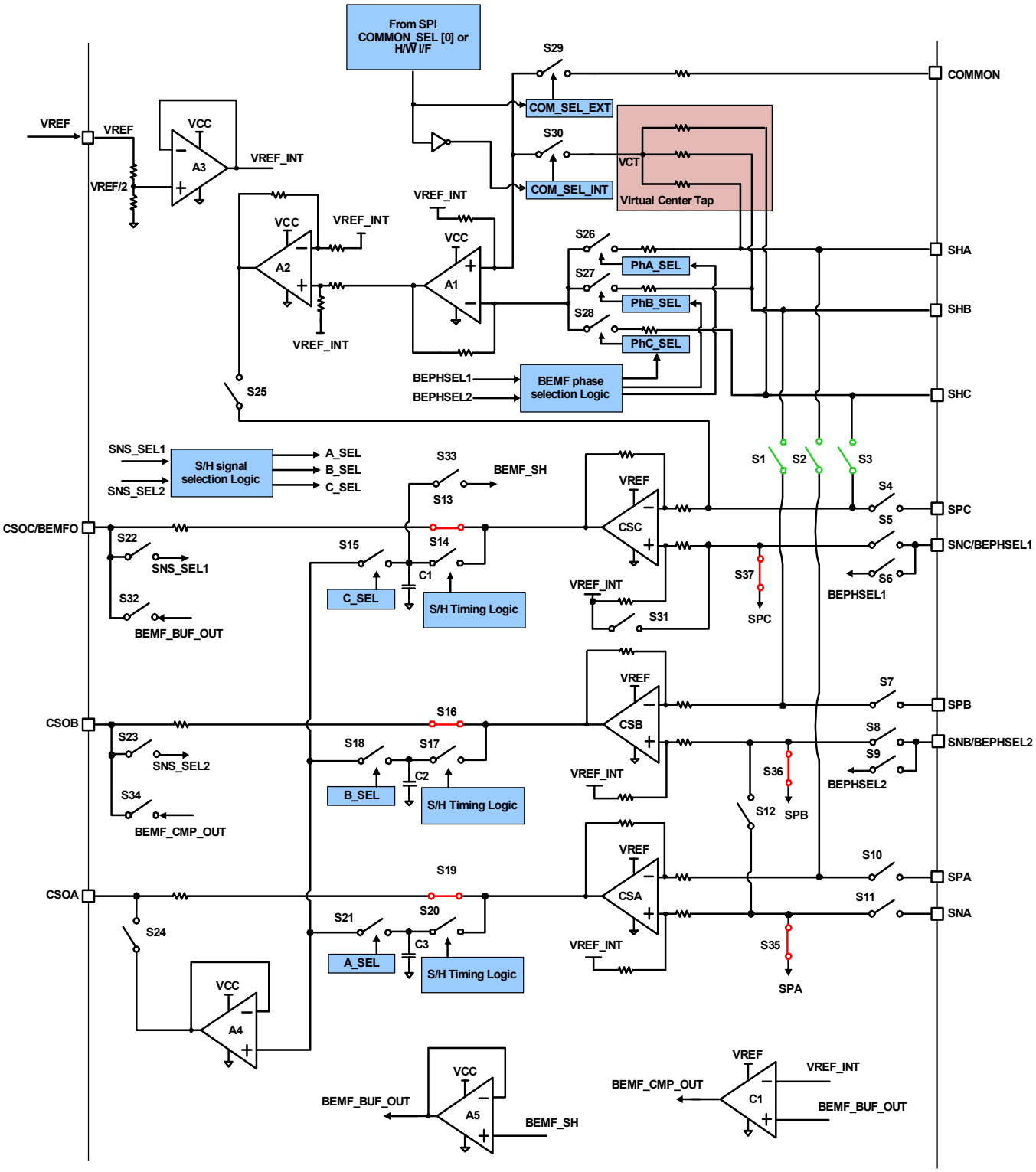


Figure 35. Configuration 7

The switches in green are on and off by internal logic. For more details, see Table 13.

Table 13. Configuration 7

Switch	Description
S1	On if Phase B low-side MOSFET is on
S2	On if Phase A low-side MOSFET is on
S3	On if Phase C low-side MOSFET is on

5.3.2.8 Configuration 8

See the high level diagram in Figure 36. In Configuration 8 (BEMF enabled, $r_{DS(ON)}$ current sensing, current S/H disabled, BEMF sensing S/H disabled), the switches colored in red are on permanently, and the switches in black are off permanently. Switches colored in green are controlled by internal logic. This allows CSA and CSB to sense currents from the low-side MOSFET VDS drop during on-state. Amplifiers A1, A2, and CSC are used to sense BEMF.

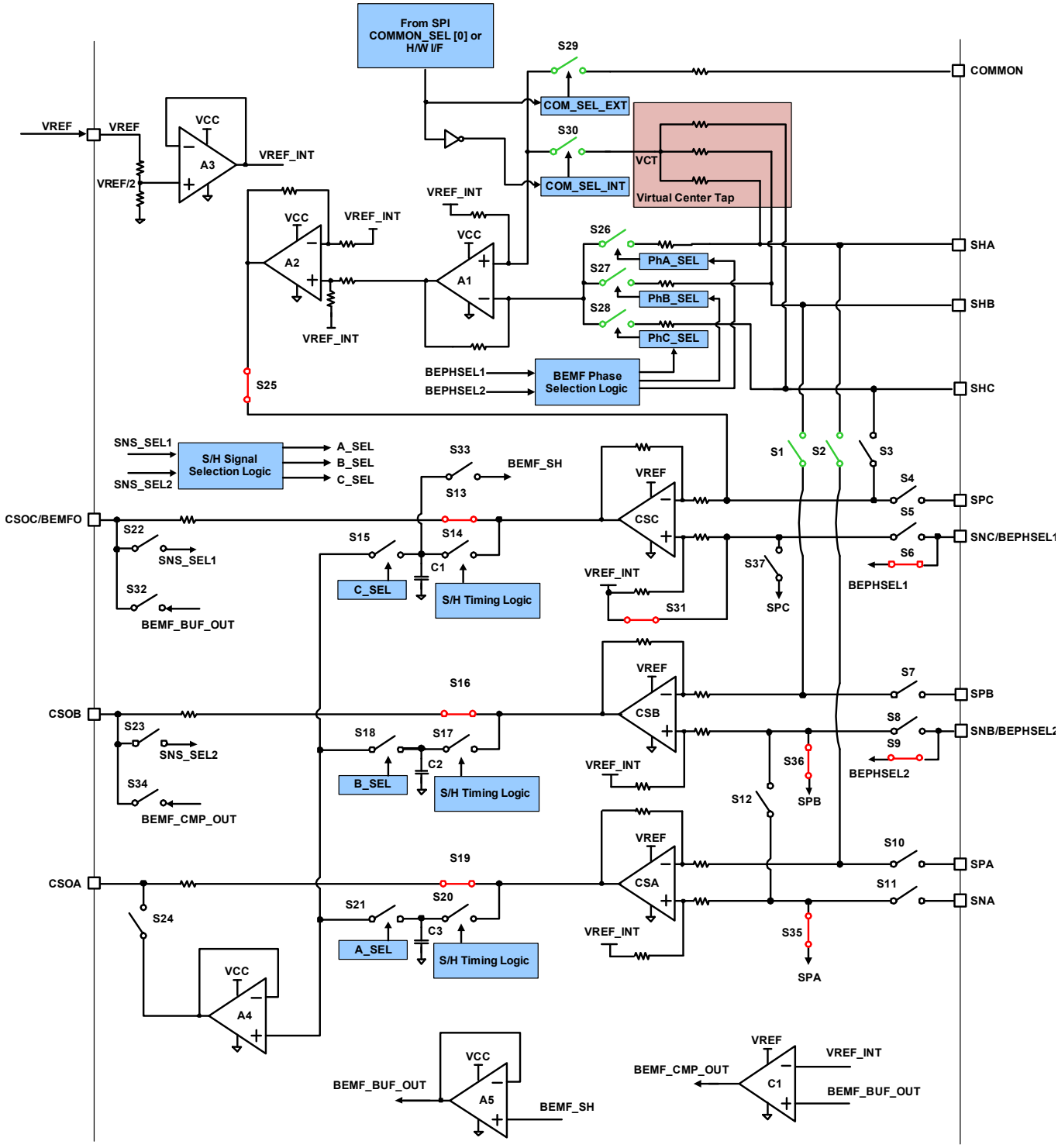


Figure 36. Configuration 8

The switches in green are on and off by internal logic. See Table 14 for details.

Table 14. Configuration 8

Switch	Description
S29	On if configured to use external motor center tap connection
S30	On if configured to use internal virtual center tap connection
S26	On if BEMF sensing selection phase is Phase A
S27	On if BEMF sensing selection phase is Phase B
S28	On if BEMF sensing selection phase is Phase C
S1	On if Phase B low-side MOSFET is on
S2	On if Phase A low-side MOSFET is on

5.3.2.9 Configuration 9

See the high level diagram in Figure 37. In Configuration 9 (BEMF enabled, shunt current sensing (Phase A), current S/H enabled, BEMF sensing S/H enabled), the switches colored in red are on permanently, and the switches in black are off permanently. Switches colored in green are controlled by internal logic. This allows CSA to sense currents through the shunt during the on-state. **Note:** Shunt sense OCP is still enabled for Phase B. Amplifiers A1, A2, and CSC are used to sense BEMF.

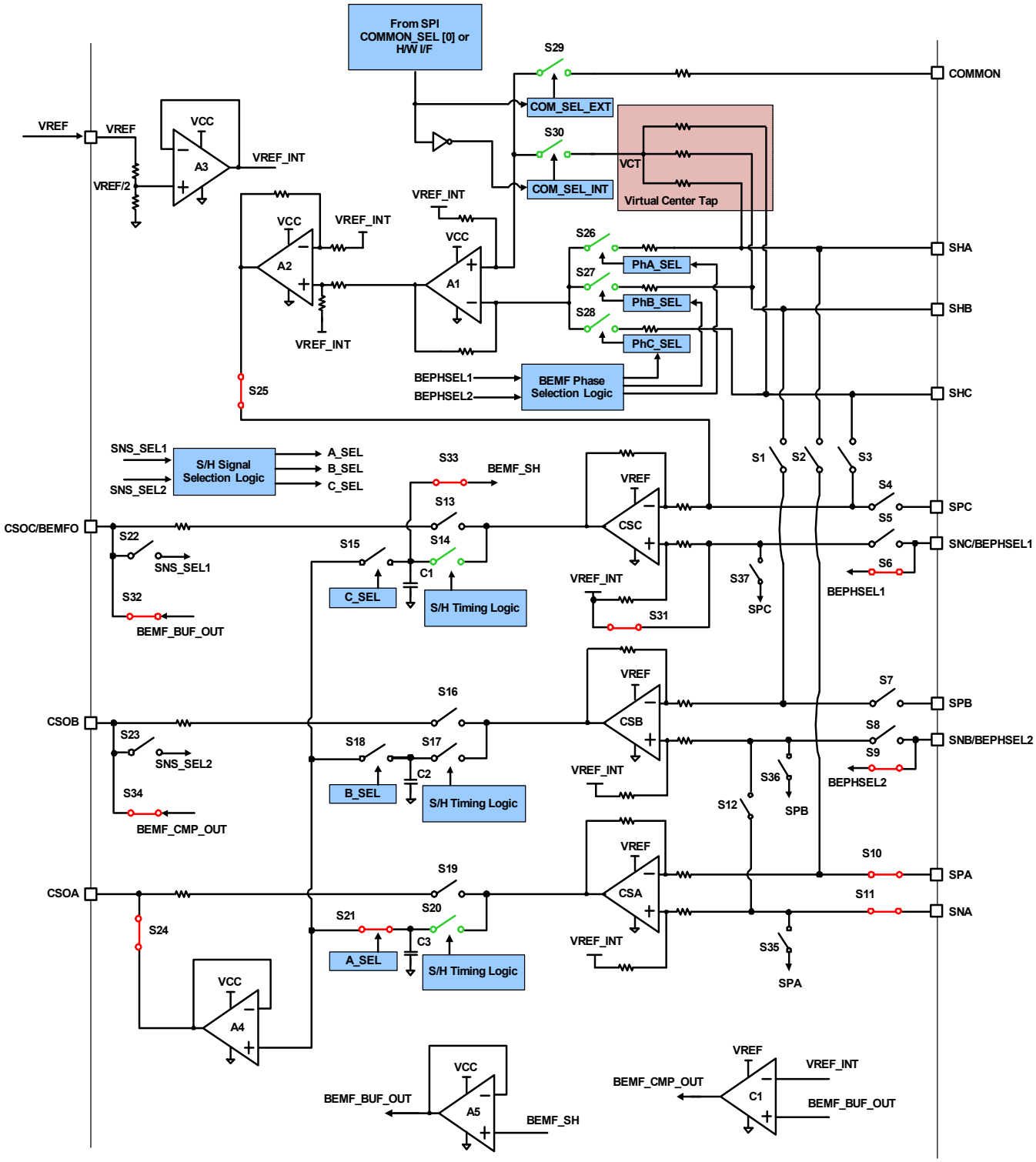


Figure 37. Configuration 9

The switches in green are on and off by internal logic. See Table 15 for details.

Table 15. Configuration 9

Switch	Description
S29	On if configured to use external motor center tap connection
S30	On if configured to use internal virtual center tap connection
S26	On if BEMF sensing selection phase is Phase A
S27	On if BEMF sensing selection phase is Phase B
S28	On if BEMF sensing selection phase is Phase C
S14, S20	These are the S/H switches; their on/off timing is determined by internal timing logic

5.3.3 Structure of Amplifiers CSA, CSB, and CSC

See the detailed block diagram in Figure 38 of amplifiers CSA, CSB, and CSC. **Note:** the block diagram only shows structures of one amplifier, and the naming of switches Q_1 to Q_8 is different from the previous high level diagrams, to avoid confusion. The following is key information:

- Support ground-side shunt current sense and low-side MOSFET $r_{DS(ON)}$ current sense
- For low-side MOSFET $r_{DS(ON)}$ current sense, the device does not implement temperature compensation to the sensed signal. It needs to be done in MCU digital domain.
- For low-side $r_{DS(ON)}$ sense, Q_5 is turned on shortly after low-side MOSFET is on and T_GT is completed.
- Q_6 is turned on permanently if BEMF sensing is enabled, allowing output of A2 to be connected to CSC.
- Sample and hold switch Q_8 and MUX switch Q_7 are added to support operation if internal S/H feature is enabled.
- Bidirectional current sense is able to sense both positive and negative current across shunt or low-side $r_{DS(ON)}$
- If BEMF sensing is enabled, amplifier CSC is used as the 3rd stage of the sensing signal chain. The 1st and 2nd stages are amplifiers A1 and A2.
- Adjustable gain (5 V/V, 10 V/V, 20 V/V, 40 V/V)
- Output biased at ½*V_{REF}. V_{REF} can be connected to AUXVCC; or a separate voltage reference can be supplied.
- DC offset calibration is automatically conducted on device power up. It can also be initiated by setting CAL_CSx bit in SPI register. It is done by turning off Q_3 and Q_4, turning on Q_1 and Q_2 (shorting differential amplifier inputs), and setting gain to be 40 V/V, and then going through an auto-zero routine to minimize amplifier input offset. **Note:** During power up, all three amplifiers are calibrated automatically. If initiating calibration through SPI, each amplifier can be calibrated individually by setting the individual CAL_CSx bit. Multiple CAL_CSx bits can be set simultaneously to perform calibration on multiple phases. **Note:** It takes approximately 768µs to finish calibration on three amplifiers. Renesas recommends allowing 1ms for the calibration to complete in actual application. Although the calibration can be initiated by SPI interface even on the fly, Renesas highly recommends conducting the calibration when no MOSFETs are switching and with all driver output pulled low to avoid any impact of noise on calibration accuracy. **Note:** Setting the CAL_CONN bit can select the amplifier inputs connection during calibration to be either shorted inside the device or still connected to the external shunt. If connecting to an external shunt, the offset of external circuitry is compensated but you need to ensure no current is flowing through the shunt.
- Input of the current sense amplifier is continuously monitored to detect overcurrent condition.

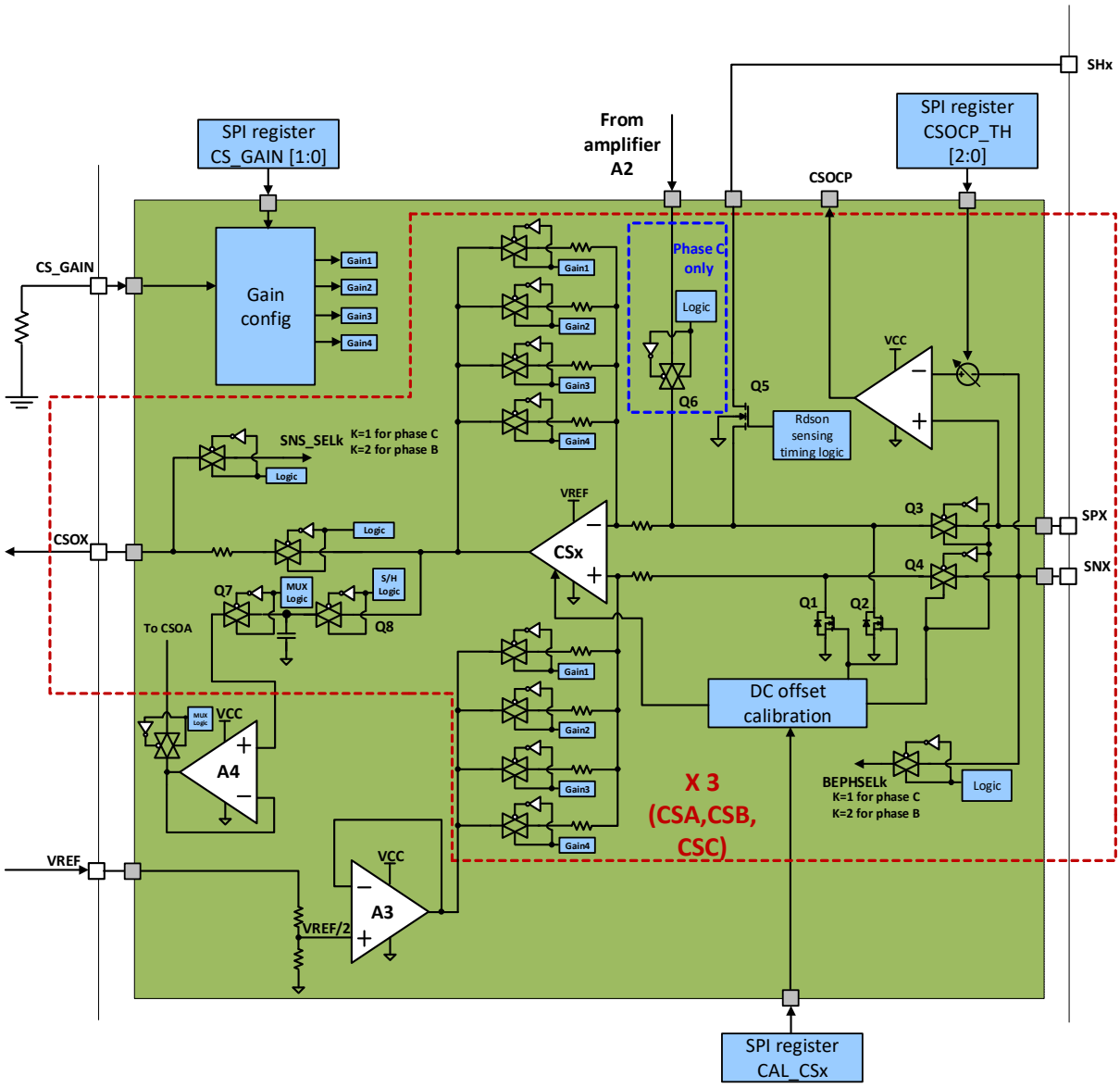


Figure 38. Detailed Block Diagram of CSA, CSB, and CSC Amplifiers

5.3.4 BEMF Sensing Control Signal Logic

Internal BEMF phase selection decoder logic generates four states based on two control signal inputs on SNC/BEPHSEL1 and SNB/BEPHSEL2 pins. These four states put the phase selection switches into the following on/off combinations.

Table 16. BEMF Sensing Control Signal Decoder

SNC/BEPHSEL1	SNB/BEPHSEL2	PhA_SEL	PhB_SEL	PhC_SEL
0	0	Off	Off	Off
0	1	On	Off	Off
1	0	Off	On	Off
1	1	Off	Off	On

5.3.5 Multiplexer Control Signal Logic

If the internal S/H feature is enabled, the CSOC/BEMF and CSOB pins are used as control signal inputs to select which S/H signal is MUXed out through buffer A4.

Table 17. Multiplexer Control Signal Logic

CSOC/BEMFO (SNS_SEL1)	CSOB (SNS_SEL2)	A_SEL	B_SEL	C_SEL
0	0	Off	Off	Off
0	1	On	Off	Off
1	0	Off	On	Off
1	1	Off	Off	On

5.3.6 Sample and Hold Timing Logic

The same S/H timing logic applies to both shunt current sense S/H and BEMF S/H. To explain the timing, a typical six step trapezoidal driving scheme is shown in Figure 39.

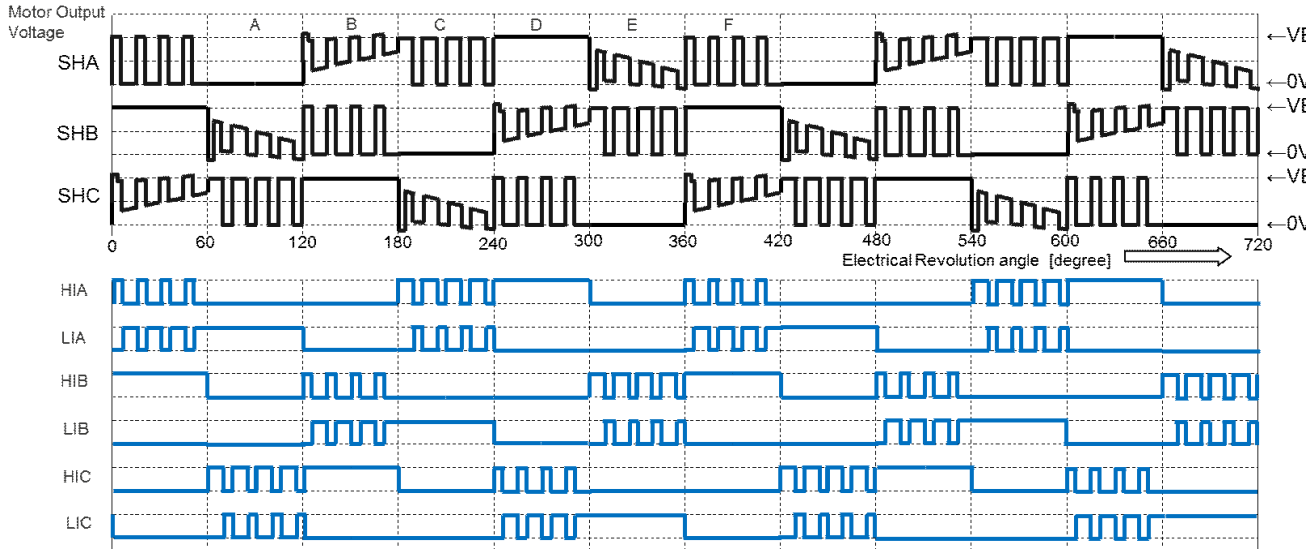


Figure 39. Typical Six Step Trapezoidal Driving Scheme

A full cycle of driving period consists of six commutation cycles (A, B, C, D, E, F), each of which lasts 60° electrical revolution angle. Assuming HI/LI driver mode within each commutation cycle, one phase (deactivated phase) is left floating. For example, both HI and LI inputs are low, the other two phases (active phases) are actively switching, where they can either do bipolar switching or unipolar switching. Figure 39 shows an example of unipolar switching. In the six commutation cycles (A, B, C, D, E, and F) shown in Figure 39, the current flows through the two active driving phases are C->A, C->B, A->B, A->C, B->C, and B->A respectively, and the other phase is the deactivated phase. For BEMF sensing, the switch node voltage (SHx) of deactivate phase is sensed. For shunt current sensing, voltage across the shunt resistor (SPx vs. SNx) of the phase with low-side ON is sensed.

The following is the general description of the S/H timing logic:

- The S/H switch is ON only when one or both high-side MOSFETs from the active phases is ON, and only one low-side MOSFET from the active phases is ON. That is the driving combination state when motor center tap voltage is approximately VBRIDGE/2.

- The actual turning on timing of the S/H switch needs to occur after any possible transition is over. That requires to turn on after a reasonable delay relative to the HI and LI rising edge. The delay time is realized by waiting for gate switching propagation delay (typical 40ns) plus the configured gate driver transition time T_GT.
- The actual turning off timing of the S/H switch aligns to the falling edge of the internal gate-off logic signal (which is issued shortly after HI or LI falling edge). This ensures the hold value is not affected by the OFF transition.

For example, the S/H timing within commutation period A is seen in Figure 40, when C and A are active driving phases and B is the deactivated phase. S/H starts with Sample period when tdly after HIC turns ON, and Hold period starts when HIC turns OFF. For BEMF sensing, SHB is sensed. For shunt current sensing, SPA vs. SNA is sensed.

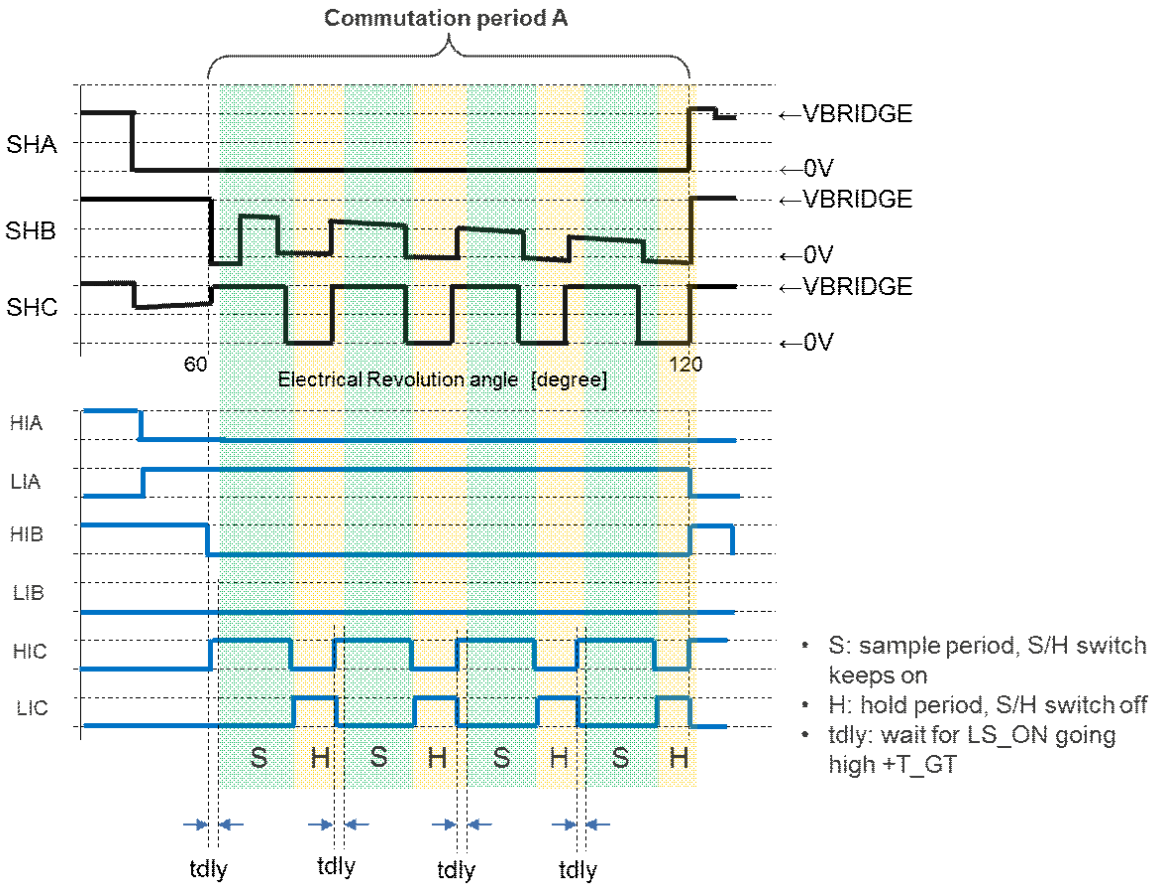


Figure 40. S/H Timing Within Commutation Period A

5.3.7 Low-Side $r_{DS(ON)}$ Current Sensing Timing Logic

If configured as low-side $r_{DS(ON)}$ current sense, the high voltage switch Q_5 is turned on after LS_ON plus configured gate transition time T_GT. Q_5 is turned off on the corresponding low-side gate-off logic signal, which is issued shortly after HI or LI falling edge.

5.4 Hardware Interface for Parameter Setting

5.4.1 Parameter Setting Tables

Table 18. MODE/SDO

Pin Configuration	PWM Mode	Current Sensing Mode
Tie to VCC	3-phase PWM	Shunt
60.4kΩ to SGND	3-phase PWM	Low-side $r_{DS(ON)}$
25kΩ to SGND	3-phase HI/LI	Low-side $r_{DS(ON)}$
Tie to SGND	3-phase HI/LI	Shunt

Table 19. CSGAIN/SCLK

Pin Configuration	CS_GAIN (V/V)
Tie to SGND	5
25kΩ to SGND	10
60.4kΩ to SGND	20
120kΩ to SGND	40

Table 20. IDRV/SDI, VDSTH/nSCS

Pin Configuration	I_{DRV} (src/snk) (mA)	V_{DS_TH} (V)
Tie to SGND	70/180	0.075
25kΩ to SGND	160/350	0.24
62kΩ to SGND	220/500	0.40
133kΩ to SGND	310/650	0.65
91kΩ to VCC	400/800	0.71
50kΩ to VCC	500/1000	1.2
25kΩ to VCC	700/1400	1.6
Tie to VCC	1100/2400	2.2

Table 21. DT/IFSEL/BEN

Pin Configuration	Dead Time (ns)	Interface Selection	BEMF sensing
Tie to VCC	150	SPI	Disabled by default. Can be enabled later by SPI bit
Tie to SGND	150	HW	Enabled. Use virtual common. Set default gain to 0.5
25kΩ to SGND	150	HW	Enabled. Use common pin. Set default gain to 0.5
60.4kΩ to SGND	250	HW	Disabled
120kΩ to SGND	450	HW	Disabled

5.5 Serial Peripheral Interface (SPI)

4-wire serial peripheral interface: nSCS (chip select, active low), SCLK (clock), SDI (data input), and SDO (data output). The SPI block of device only works in slave mode. **Note:** The SDO pin has internal pull-down switch resistance. Renesas recommends using a 2kΩ or higher pull-up resistor to avoid any issue.

5.5.1 Communication Protocol

The communication format contains one 16-bit word per transaction. MSB is R/W bit, low for write and high for read. It is followed by 3-bit of address bits (Add[2:0]). 12-bit of data bits (Data[11:0]) comes after that.

- Pulling nSCS low to select the SPI communication with the device; pulling nSCS high deselect the device from SPI communication.
- SDO data is propagated on SDO line on SCLK rising edge. SDI data is captured and latched by the device on falling edge of the SCLK.
- On SDO, the Most Significant Bit (MSB) shifts out first. For SDI, the MSB shifts in first.
- SCLK is low during nSCS transitions from low-to-high, and from high-to-low.
- Between each word transaction, nSCS is required to be pulled high for at least 400ns (t_{HInSCS}).
- The SPI register valid address range is 0x0 to 0x5. If the address bits (Add[2:0]) value is out of range, or the total number of bits transmitted in one transaction is not 16 bits, data word is ignored.
- For write command, the data currently in the SPI register is shifted out onto SDO.
- For applications that have multiple slave devices sharing the SPI bus, reference the Application Note for appropriate configurations.
- Write protocol:

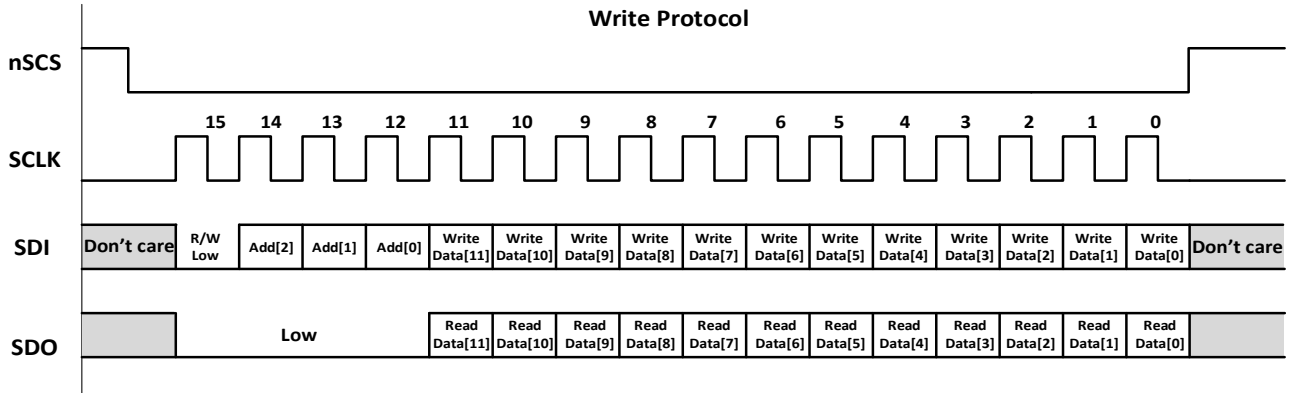


Figure 41. Write Protocol

- Read protocol:

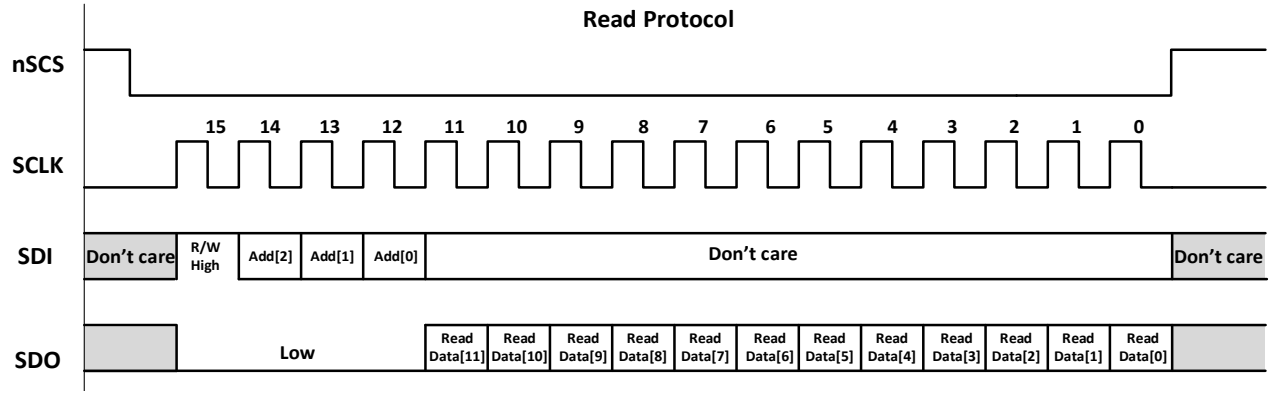


Figure 42. Read Protocol

5.5.2 Timing Diagram

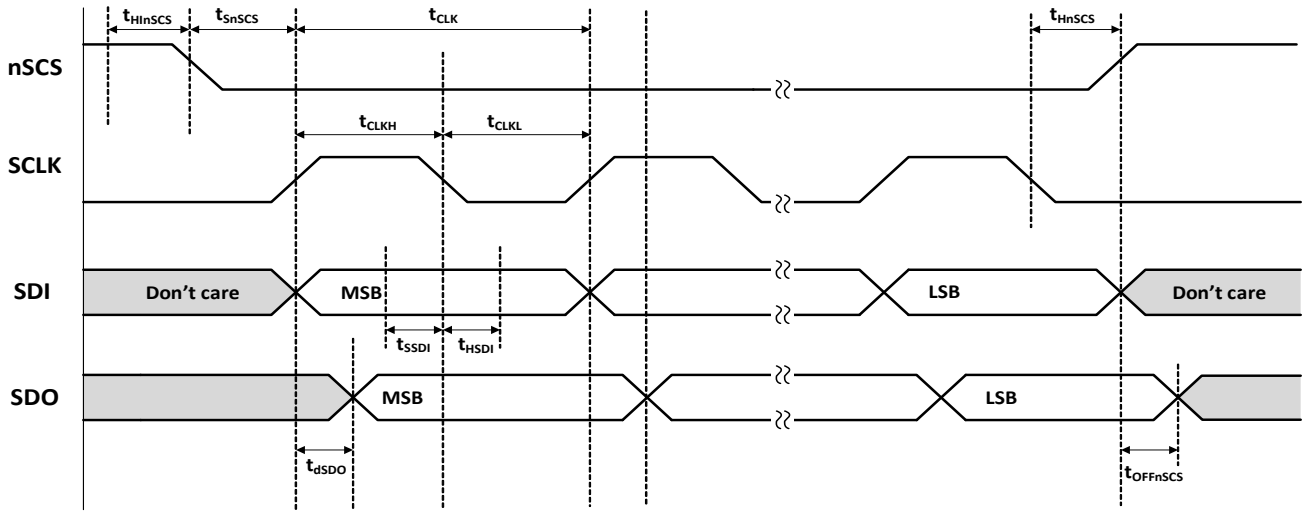


Figure 43. Timing Diagram

Table 22. Timing Specifications

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Sleep mode to SPI interface ready	t_{ready}	VCC > VCC_POR, EN from low to high		2		ms
SCLK period	t_{clk}		200			ns
SCLK high time	t_{clkH}		100			ns
SCLK low time	t_{clkL}		100			ns
SDI input data setup time	t_{SSDI}		40			ns
SDI input data hold time	t_{HSDI}		60			ns
SDO output data delay time	t_{dSDO}				60	ns
nSCS input setup time	t_{SnSCS}		100			ns
nSCS input hold time	t_{HnSCS}		100			ns
nSCS high time before pulling low	t_{HInSCS}		400			ns
Chip deselect off time	$t_{OFFnSCS}$			20		ns

6. Register Map

Table 23 and Table 24 show the bit maps for the Fault Status Registers 1 and 2 (0x0h and 0x1h). Table 25 to Table 28 show the bit definitions and default settings for the Control Registers 1 to 4 (0x2h to 0x5h). The control registers are reset to default settings when the device enters Sleep or Shutdown mode.

Table 23. Fault Status 1 (0x0h)

Bit	Field	Type	Default	Description	Note
[11]	FAULT	R	0b	Set if any fault occurs; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[10]	VM_UVLO	R	0b	Set if VM < VM_UVLO-hysteresis (3.9V typical); reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[9]	Reserved	R	0b	Reserved	
[8]	CP_UV	R	0b	Set if VCP-VM voltage < VCP_UV (typical 0.55*VDRV); reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[7]	VDS_OCP	R	0b	Set if any of the external MOSFETs VDS > VDS_TH; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[6]	CS_OCP	R	0b	Set if any shunt amplifier SPx-SNx > CSOCP_TH; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[5]	OTW	R	0b	Set if $T_J > T_{OTW}$ (value 140°C); reset when T_J drops below T_{OTW} - hysteresis	Thermal warning
[4]	OTSD	R	0b	Set if $T_J > T_{OTP}$ (value 160°C); reset by writing 1b to CLR_FLT or recovery low pulse on EN	Thermal shutdown
[3]	Reserved	R	0b	Reserved	
[2]	BB_OC2	R	0b	Set if $I_L > I_{OC2}$ (typical 1.6A); reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[1]	BB_UV	R	0b	Set if VDRV < $0.8*V_{out\_nominal}$ ($V_{FB} < 0.8*V_{REF}$); reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[0]	BB_OV	R	0b	Set if VDRV > $1.2*V_{out\_nominal}$ ($V_{FB} > 1.2*V_{REF}$); reset by writing 1b to CLR_FLT or recovery low pulse on EN	

Table 24. Fault Status 2 (0x1h)

Bit	Field	Type	Default	Description	Note
[11]	CSA_OC	R	0b	Set if shunt amplifier A indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[10]	CSB_OC	R	0b	Set if shunt amplifier B indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[9]	CSC_OC	R	0b	Set if shunt amplifier C indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[8]	VDSHA_OC	R	0b	Set if Phase A high-side MOSFET VDS indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[7]	VDSLA_OC	R	0b	Set if Phase A low-side MOSFET VDS indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[6]	VDSHB_OC	R	0b	Set if Phase B high-side MOSFET VDS indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[5]	VDSLB_OC	R	0b	Set if Phase B low-side MOSFET VDS indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	

Table 24. Fault Status 2 (0x1h) (Cont.)

Bit	Field	Type	Default	Description	Note
[4]	VDSHC_OC	R	0b	Set if Phase C high-side MOSFET VDS indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[3]	VDSLC_OC	R	0b	Set if Phase C low-side MOSFET VDS indicates OC; reset by writing 1b to CLR_FLT or recovery low pulse on EN	
[2]	Reserved	R	0b	Reserved	
[1]	Reserved	R	0b		
[0]	Reserved	R	0b		

Table 25. Control Register 1 (0x2h)

Bit	Field	Type	Default	Description	Note
[11]	CLR_FLT	R/W	0b	Write 1b to clear all the flagged fault status bit. This bit automatically resets to 0b after it has been written.	
[10]	WRITE_LOCK	R/W	0b	Write 110b to ignore all further register write except WRITE_LOCK[10:8]; write 011b to unlock to allow register write. Writing other values takes no effect.	
[9]	WRITE_LOCK	R/W	1b		
[8]	WRITE_LOCK	R/W	1b		
[7]	CPUV_EN	R/W	1b	1b: charge pump undervoltage protection is enabled; 0b: charge pump undervoltage only reports fault through nFault and SPI CP_UV bit, no protection action takes place	
[6]	BEMF_SH_EN	R/W	0b	0b: Disable S/H on BEMF sense amplifiers; 1b: enable S/H on BEMF sense amplifiers	EN bit for S/H sensed BEMF
[5]	OTW_REPORT	R/W	1b	1b: OT warning is reported both on nFault pin and SPI OTW bit; 0b: OT warning is only reported on SPI OTW bit	
[4]	PWM_MODE	R/W	0b	0b: 3-Phase LI/HI mode; 1b: 3-Phase PWM mode	Driver control input mode
[3]	DEAD_TIME	R/W	0b	00b: 100ns; 01b: 150ns; 10b: 250ns; 11b: 450ns	Dead time between HS and LS driver outputs
[2]	DEAD_TIME	R/W	1b		
[1]	CS_MODE	R/W	0b	0b: ground-side shunt sense; 1b: low-side $r_{DS(ON)}$ sense	
[0]	CS_SH_EN	R/W	0b	0b: Disable S/H on current sense amplifiers; 1b: enable S/H on current sense amplifiers	EN bit for S/H sensed current

Table 26. Control Register 2 (0x3h)

Bit	Field	Type	Default	Description	Note
[11]	VDSOCP_MODE	R/W	0b	00b: Latch on VDS OC fault, recover by EN pulse or CLR_FLT; 01b: Automatic retry on VDS OC fault based on setting in bit 3 (retry delay for VDS OCP); 10b: report on nFault and VDS_OCP bit only; 11b: no report on FAULT bit and no action take place. VDS OCP bits are set in registers Fault Status 1 and Fault Status 2.	Response mode for VDS OCP
[10]	VDSOCP_MODE	R/W	0b		

Table 26. Control Register 2 (0x3h) (Cont.)

Bit	Field	Type	Default	Description	Note
[9]	VDS_TH	R/W	1b	0000b: 35mV; 0001b: 75mV; 0010b: 160mV; 0011b: 240mV	VDS OCP threshold
[8]	VDS_TH	R/W	0b	0100b: 320mV; 0101b: 400mV; 0110b: 520mV; 0111b: 645mV	
[7]	VDS_TH	R/W	0b	1000b: 670mV; 1001b: 710mV; 1010b: 880mV; 1011b: 1200mV	
[6]	VDS_TH	R/W	1b	1100b: 1400mV; 1101b: 1600mV; 1110b: 1800mV; 1111b: 2150mV	
[5]	DEG_TIME	R/W	0b	00b: 1.4µs; 01b: 2.2µs; 10b: 3.2µs; 11b: 5.4µs	OCP deglitching time for both VDS OCP and CS OCP
[4]	DEG_TIME	R/W	1b		
[3]	RETRY_DELAY_VDSOCP	R/W	0b	0b: 4 ms; 1b: 70µs	Retry delay for VDS OCP
[2]	RETRY_DELAY_CSOCP	R/W	0b	0b: 4 ms; 1b: 70µs	Retry delay for CS OCP
[1]	CSOCP_MODE	R/W	0b	00b: Latch on CS OC fault, recover by EN pulse or CLR_FLT; 01b: automatic retry on CS OC fault based on settings in bit 2 (retry delay for CS OCP); 10b: report on nFault and CS_OCP bit only; 11b: no report on FAULT bit and no action take place. CS OCP bits are set in registers Fault Status 1 and Fault Status 2.	Response mode for CS OCP
[0]	CSOCP_MODE	R/W	0b		

Table 27. Control Register 3 (0x4h)

Bit	Field	Type	Default	Description	Note
[11]	CSOCP_TH	R/W	1b	000b: 50mV; 001b: 100mV; 010b: 150mV; 011b: 200mV; 100b: 250mV; 101b: 500mV; 110b: 750mV; 111b: 1000mV	
[10]	CSOCP_TH	R/W	0b		
[9]	CSOCP_TH	R/W	1b		
[8]	CS_GAIN	R/W	1b	00b: Gain = 5V/V; 01b: Gain = 10V/V; 10b: Gain = 20V/V; 11b: Gain = 40V/V	
[7]	CS_GAIN	R/W	0b		
[6]	CAL_CSA	R/W	0b	Write 1b to enable DC offset calibration for shunt amplifier A. This bit automatically resets to 0 after calibration is done	
[5]	CAL_CSB	R/W	0b	Write 1b to enable DC offset calibration for shunt amplifier B. This bit automatically resets to 0 after calibration is done	
[4]	CAL_CSC/CAL_BEMFS	R/W	0b	Write 1b to this bit to enable DC offset calibration for shunt amplifier C if BEMF sensing is disabled (BEMF_EN=0b). Write 1b to this bit to enable DC offset calibration for BEMF sensing amplifiers if BEMF sensing is enabled (BEMF_EN = 1b). This bit automatically resets to 0 after calibration is done	
[3]	BEMF_EN	R/W	0b	0b: BEMF sensing is disabled; 1b: BEMF sensing is enabled and shunt amplifier C is configured for BEMF sensing	
[2]	BEMF_GAIN	R/W	0b	00b: 0.25; 01b: 0.5; 10b: 1; 11b: 2	
[1]	BEMF_GAIN	R/W	1b		
[0]	COMMON_SEL	R/W	0b	0b: Select internal virtual common; 1b: Select common pin	

Table 28. Control Register 4 (0x5h)

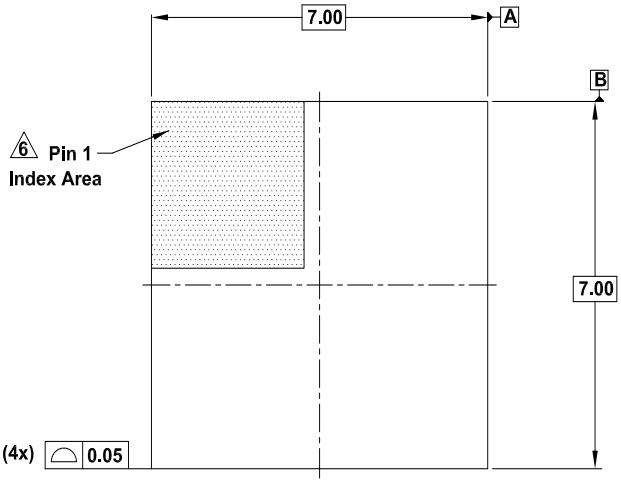
Bit	Field	Type	Default	Description	Note
[11]	T_GT	R/W	0b	00b: 0.5µs; 01b: 1.0µs; 10b: 2.0µs; 11b: 4.0µs	Gate driver transition time
[10]	T_GT	R/W	1b		High-side driver output source current; sink current is always 2*source current
[9]	I_SRC_HS	R/W	1b	0000b: 50mA; 0001b: 70mA; 0010b: 120mA; 0011b: 160mA	High-side driver output source current; sink current is always 2*source current
[8]	I_SRC_HS	R/W	1b	0100b: 200mA; 0101b: 220mA; 0110b: 250mA; 0111b: 310mA	
[7]	I_SRC_HS	R/W	1b	1000b: 350mA; 1001b: 400mA; 1010b: 440mA; 1011b: 500mA	
[6]	I_SRC_HS	R/W	1b	1100b: 580mA; 1101b: 700mA; 1110b: 900mA; 1111b: 1100mA	
[5]	I_SRC_LS	R/W	1b	0000b: 50mA; 0001b: 70mA; 0010b: 120mA; 0011b: 160mA	Low-side driver output source current; sink current is always 2 * source current
[4]	I_SRC_LS	R/W	1b	0100b: 200mA; 0101b: 220mA; 0110b: 250mA; 0111b: 310mA	
[3]	I_SRC_LS	R/W	1b	1000b: 350mA; 1001b: 400mA; 1010b: 440mA; 1011b: 500mA	
[2]	I_SRC_LS	R/W	1b	1100b: 580mA; 1101b: 700mA; 1110b: 900mA; 1111b: 1100mA	
[1]	CAL_CONN	R/W	0b	0b: During amplifiers DC calibration, the internal switches short the amplifier inputs 1b: During amplifiers DC calibration, the amplifier inputs are still connected to the external shunt.	
[0]	BEMF_CMP_MODE	R/W	0b	0b: Disables the BEMF comparator mode 1b: Enables the BEMF comparator mode	Modifications affect Configuration 9

7. Package Outline Drawing

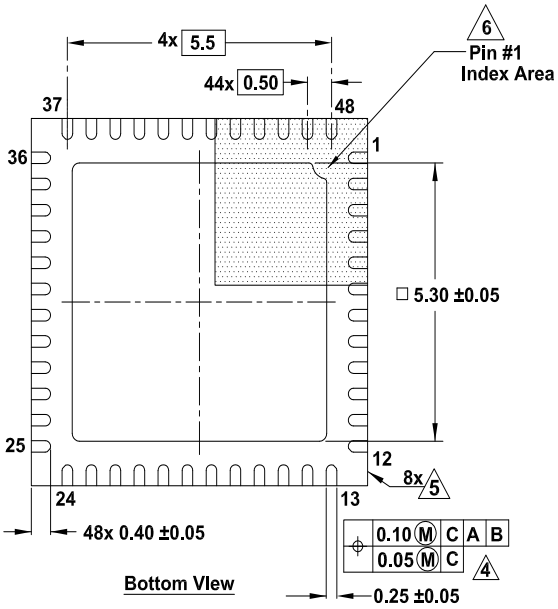
For the most recent package outline drawing, see L48.7x7Q.

L48.7x7Q

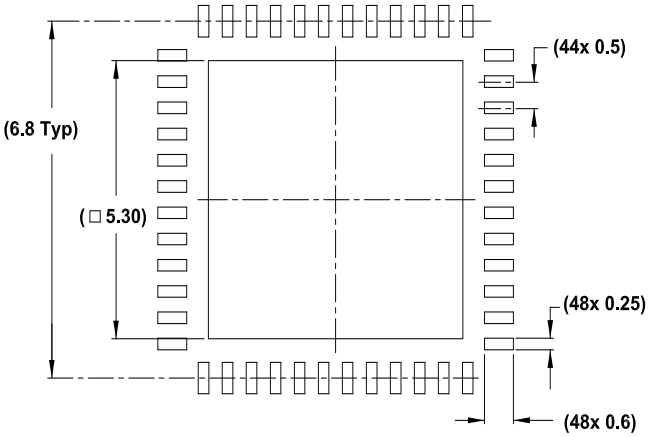
48 Lead Thin Quad Flat No Lead Plastic Package (0.5 mm pitch)
Rev 0, 6/20



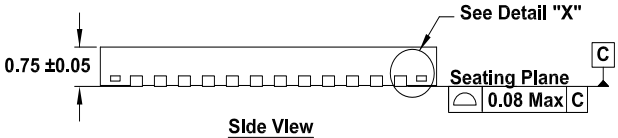
Top View



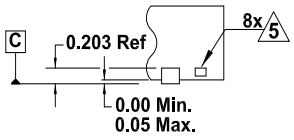
Bottom View



Typical Recommended Land Pattern



Side View



Detail "X"

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.

8. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA2270634GNP#MA0	RAA 227063	48 Ld QFN	L48.7x7Q	Reel, 250	-40 to +125°C
RAA2270634GNP#HA0				Reel, 4k	
RTKA227063DE0000BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL), see the Product Options on the RAA227063 product page (click the packaging icon). For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

9. Revision History

Rev.	Date	Description
1.03	Aug 5, 2022	Updated section 5.5.1 Communication Protocol. Updated Figures 41 to 43.
1.02	Mar 23, 2022	Added note for SPx and SNx connection when current sensing is not used. Added note to indicate control registers are reset by entering Sleep or Shutdown mode.
1.01	Nov 29, 2021	Added Power-On Sequence section. Updated Serial Peripheral Interface (SPI) section. Updated Table 5 by updating the Shunt OCP Condition and Recovery Condition (option 2).
1.00	Aug 3, 2021	Initial release.

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(Rev.1.0 Mar 2020)

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