NOT RECOMMENDED FOR NEW DESIGNS
POSSIBLE SUBSTITUTE PRODUCT
ISL6208

Data Sheet November 2001 File Number 9047

High Voltage Synchronous Rectified Buck MOSFET Driver

The ISL6205 is a high-voltage, high-frequency, dual MOSFET driver specifically designed to drive two N-Channel power MOSFETs in a synchronous rectified buck converter topology in mobile computing applications. This driver combined with an ISL6223 or other Intersil Multi-Phase Buck PWM controllers forms a complete single-stage core-voltage regulator solution for advanced mobile microprocessors.

The ISL6205 allows users to select a gate voltage ranging from 5V to 12V for the lower MOSFET in the synchronous rectified buck converter. Using a 12V gate voltage reduces the $R_{DS(ON)}$ and the conduction loss in the MOSFET. The upper gate is required to run at 5V.

The ISL6205 features a three-state PWM input that, working together with any Intersil multiphase PWM controllers, will prevent a negative transient on the output voltage when the output is being shut down. This feature eliminates the schottky diode that is usually seen in a microprocessor power system for protecting the microprocessor from any reversed output voltage damage.

The output drivers in the ISL6205 have the capacity to efficiently switch power MOSFETs at frequencies up to 2MHz. Each driver is capable of driving a 3000pF load with a 30ns propagation delay and 50ns transition time. This product implements bootstrapping on the upper gate, reducing implementation complexity and allowing the use of higher performance, cost effective, N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ISL6205CB	-10 to 85	8 Ld SOIC	M8.15
ISL6205CB-T	8 Ld SOIC Tape and Reel		

Features

- Drives Two N-Channel MOSFETs
- Adaptive Shoot-Through Protection
- 25V Operation voltage
- Supports High Switching Frequency
  - Fast Output Rise Time
  - Propagation Delay 30ns
- Small 8 Lead SOIC Package
- Dual Gate-Drive Voltages for the Lower MOSFET for Optimal Efficiency
- Three-State Input for Output Stage Shutdown
- Supply Under Voltage Protection
- 5V or 12V Drive for the Lower MOSFET

Applications

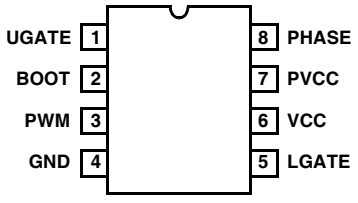
- Core Voltage Supplies for Intel Mobile Pentium® III, AMD® Mobile Athlon™ or Duron™ Microprocessors
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters
- High Input Voltage DC-DC Converters

Related Literature

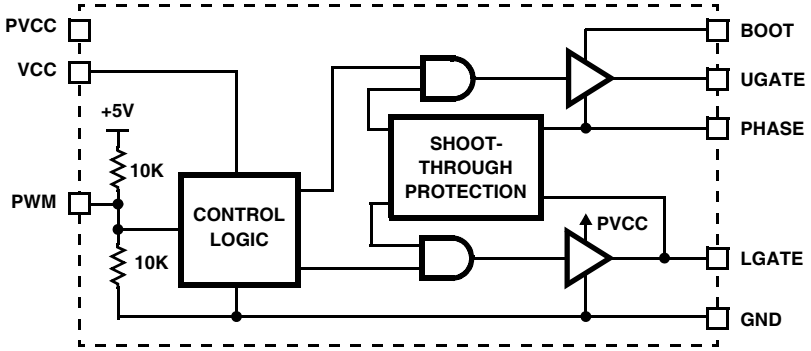
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Pinout

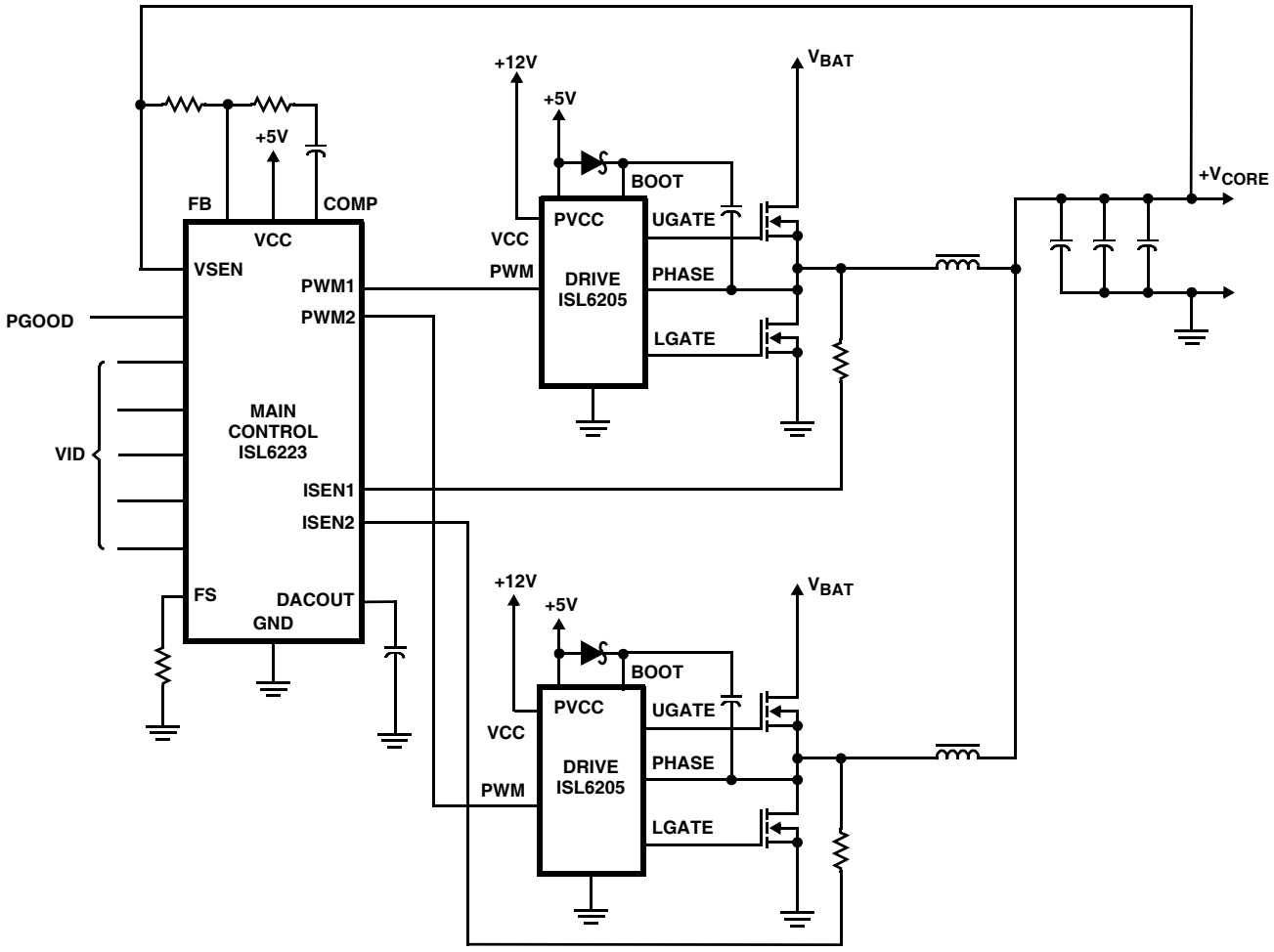
ISL6205CB, (SOIC)
TOP VIEW



Block Diagram



Typical Application - Two Phase Converter Using ISL6223 and ISL6205 Gate Drivers



Absolute Maximum Ratings

Supply Voltage (VCC, PVCC) 15V
Phase Voltage (V_{PHASE}) . . . . . -5V to 25V
BOOT Voltage (V_{BOOT} - V_{PHASE}) 7V
Input Voltage (V_{PWM}) . . . . . .GND - 0.3V to 7V
UGATE. . . . . .V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
LGATE . . . . . .GND - 0.3V to V_{PVCC} + 0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 4kV
Machine Model (Per EIAJ ED-4701 Method C-111) 200V

Operating Conditions

Ambient Temperature Range. . . . . -10°C to 85°C
Maximum Operating Junction Temperature. . . . . 125°C
Supply Voltage, VCC . . . . . 12V ±10%
Supply Voltage Range, PVCC . . . . . .5V to 12V
Boot Voltage (V_{BOOT} - V_{PHASE}) . . . . . 5V ±10%

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	97

Maximum Junction Temperature (Plastic Package) . . . . . .150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	f_{PWM} = 1MHz, V_{PVCC} = 5V	-	1.7	3.6	mA
		f_{PWM} = 1MHz, V_{PVCC} = 12V	-	1.7	3.6	mA
Upper Gate Bias Current	I_{PVCC}	f_{PWM} = 1MHz, V_{PVCC} = 5V	-	0.8	3.3	mA
POWER-ON RESET						
VCC Rising Threshold			9.6	9.95	10.4	V
VCC Falling Threshold			8.7	9.1	9.5	V
PWM INPUT						
Input Current	I_{PWM}	V_{PWM} = 0 or 5V (See Block Diagram)	-	500	-	µA
PWM Rising Threshold			3.45	3.6	-	V
PWM Falling Threshold			-	1.45	1.55	V
UGATE Rise Time	t_{RUGATE}	V_{PVCC} = 5V, 3nF Load	-	20	-	ns
LGATE Rise Time	t_{RLGATE}	V_{PVCC} = 5V, 3nF Load	-	50	-	ns
UGATE Fall Time	t_{FUGATE}	V_{PVCC} = 5V, 3nF Load	-	20	-	ns
LGATE Fall Time	t_{FLGATE}	V_{PVCC} = 5V, 3nF Load	-	20	-	ns
UGATE Turn-Off Propagation Delay	$t_{PDLUGATE}$	V_{PVCC} = 5V, 3nF Load	-	30	-	ns
LGATE Turn-Off Propagation Delay	$t_{PDLLGATE}$	V_{PVCC} = 5V, 3nF Load	-	20	-	ns
Shutdown Window			1.4	-	3.6	V
Shutdown Holdoff Time			-	230	-	ns
OUTPUT						
Upper Drive Source Impedance	R_{UGATE}	500mA Current	-	1.6	3.1	Ω
Upper Drive Sink Impedance	R_{UGATE}	500mA Current	-	2.3	4.0	Ω
Lower Drive Source Current	I_{LGATE}	V_{PVCC} = 5V	600	850	-	mA
Lower Drive Sink Impedance	R_{LGATE}	500mA Current	-	1.2	2.5	Ω

Functional Pin Description

UGATE (Pin 1)

Upper gate drive output. Connect to the gate of high-side power N-Channel MOSFET.

BOOT (Pin 2)

Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin and a schottky diode between this pin and a 5V supply. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Bootstrap Diode and Capacitor section under DESCRIPTION for guidance in choosing the appropriate capacitor value.

PWM (Pin 3)

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation. See the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.

GND (Pin 4)

Ground pin. All signals are referenced to this node.

LGATE (Pin 5)

Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.

VCC (Pin 6)

Connect this pin to a +12V bias supply. Place a high quality bypass capacitor from this pin to GND.

PVCC (Pin 7)

This pin supplies the lower gate drive bias. Connect this pin to either +12V or +5V.

PHASE (Pin 8)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. The PHASE voltage is monitored for adaptive shoot-through protection. This pin also provides a return path for the upper gate drive.

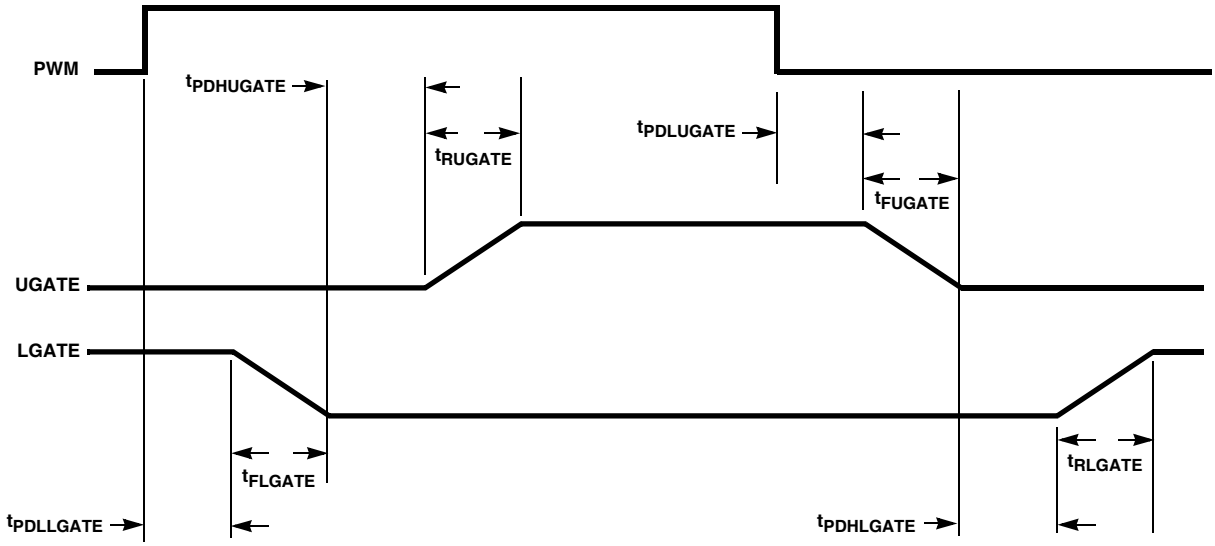
Description

Operation

Designed for versatility and speed, the ISL6205 dual MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

The upper and lower gates are held low until the driver is initialized. Once the VCC voltage surpasses the VCC Rising Threshold (See Electrical Specifications), the PWM signal takes control of gate transitions. A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [$t_{PDLLGATE}$], the lower gate begins to fall. Typical fall times [t_{FLGATE}] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [$t_{PDHUGATE}$] based on how quickly the LGATE voltage drops below 0.5V. This prevents both the lower and upper MOSFETs from conducting simultaneously or shoot-through. Once this delay period is complete the upper gate drive begins to rise [t_{RUGATE}] and the upper MOSFET turns on.

Timing Diagram



Three-State PWM Input

A unique feature of the ISL6205 and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the Electrical Specifications determine when the lower and upper gates are enabled.

Adaptive Shoot-Through Protection

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 0.5V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the PHASE voltage during UGATE turn-off. Once PHASE has dropped below a threshold of 3V, the LGATE is allowed to rise. PHASE continues to be monitored during the lower gate rise time. If PHASE has not dropped below 3V within 250ns of the falling edge of the PWM input, LGATE is taken high to keep the bootstrap capacitor charged. If the PHASE voltage exceeds the 3V threshold during this period and remains high for longer than 2μs, the LGATE transitions low. Both upper and lower gates are then held low until the next rising edge of the PWM signal.

Power-On Reset (POR) Function

During initial startup, the VCC voltage rise is monitored and gate drives are held low until a typical VCC rising threshold of 9.95V is reached. Once the rising VCC threshold is exceeded, the PWM input signal takes control of the gate drives. If VCC drops below a typical VCC falling threshold of 9.1V during operation, then both gate drives are again held low. This condition persists until the VCC voltage exceeds the VCC rising threshold.

Bootstrap Diode and Capacitor

An external bootstrap diode and a bootstrap capacitor are required for the bootstrap circuit. The connection is shown in the typical application schematic. Typically a schottky diode should be employed for its low forward drop. Its voltage rating must be greater than the maximum battery voltage plus 5V.

The bootstrap capacitor must have a maximum voltage rating above the maximum battery voltage plus 5V. The bootstrap capacitor can be chosen from the following equation:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}}$$

where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose a MOSFET is chosen as the upper MOSFET. Its gate charge, Q_{GATE}, from the data sheet is 30nC for a 5V upper gate drive. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.15μF is required. The next larger standard value capacitance is 0.22μF. A good quality ceramic capacitor is recommended.

Gate Driver Voltage

The ISL6205 provides the user flexibility in choosing the lower gate drive voltage. Simply applying a voltage from 5V up to 12V on PVCC will set the lower driver rail voltage. The upper gate driver rail voltage is set independently by connecting a 5V supply to the anode of the bootstrap diode, as shown in Figure 1.

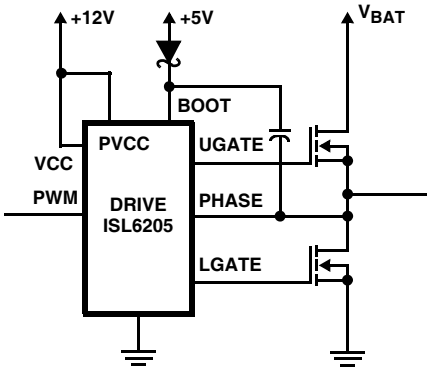


FIGURE 1. APPLICATION CIRCUIT TO USE 12V LOWER GATE VOLTAGE AND 5V UPPER GATE VOLTAGE

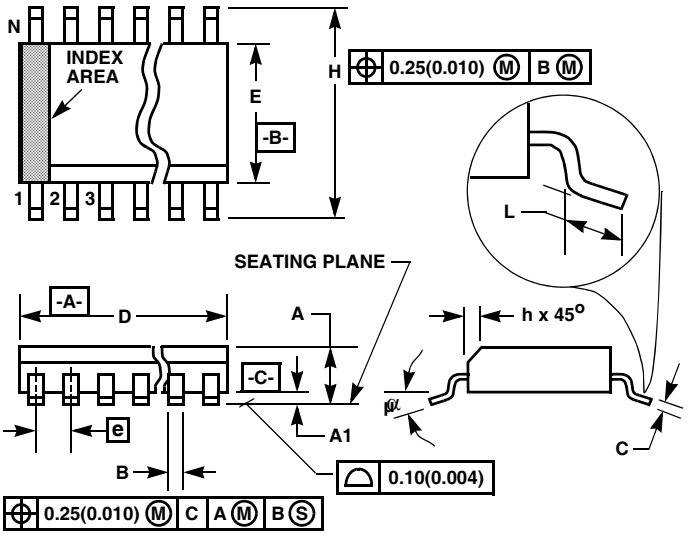
Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO-8 package is approximately 800mW. When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated as:

$$P = f_{sw}(V_U Q_U + V_L Q_L) + I_{DDQ} V_{CC}$$

where f_{sw} is the switching frequency of the PWM signal. V_U and V_L represent the upper and lower gate rail voltage. Q_U and Q_L is the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The I_{DDQ} V_{CC} product is the quiescent power of the driver and is typically 30mW.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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