RAA226110

Low-Side GAN FET Driver with Programmable Source Current and Adjustable Overcurrent Protection

The RAA226110 is a low-side driver designed to drive enhancement-mode Gallium Nitride (GaN) FETs in isolated and non-isolated topologies. The RAA226110 operates with a supply voltage from 6.5V to 18V and has both inverting (INB) and non-inverting (IN) inputs to satisfy requirements for inverting and non-inverting gate drives with a single device.

The RAA226110 provides 5.8V gate drive voltage (V_{DRV}) generated by an internal regulator that prevents the gate voltage from exceeding the maximum gate-source rating of enhancement-mode GaN FETs. The gate drive voltage features an Undervoltage Lockout (UVLO) protection that ignores the inputs (IN/INB) and keeps OUTL connected to VEEL to ensure the GaN FET is in an OFF state whenever V_{DRV} is below the UVLO threshold.

The RAA226110 IN/INB inputs can withstand voltages up to 18V regardless of the V_{DD} voltage, which allows the inputs to be connected directly to most PWM controllers. The split outputs of the RAA226110 offer the flexibility to adjust the turn-on and turn-off speed independently by adding additional impedance to the turn-on and turn-off paths.

The RAA226110 operates across the industrial temperature range from -40°C to +125°C and is offered in a 16 Ld QFN Package.

Features

- Wide operating voltage range of 6.5V to 18V
- Up to 18V logic inputs (regardless of V_{DD} level)
  - Inverting and non-inverting inputs
- Optimized to drive enhancement mode GaN FETs
  - Internal 5.8V regulated gate drive voltage
  - Independent outputs for adjustable turn-on/turn-off speeds
  - Source current programmable 0.3A, 0.75A, 2A
  - Overcurrent protection with adjustable thresholds of 40mV, 80mV, 120mV
- Fault pin and over-temperature protection
- Operating temperature range: -40°C to +125°C
- Flyback and forward converters
- Boost and PFC converters
- Secondary synchronous FET drivers

Related Literature

For a full list of related documents, visit our website:

- RAA226110 device page

Applications

- Switching-mode power supply
- GaN FET driver application

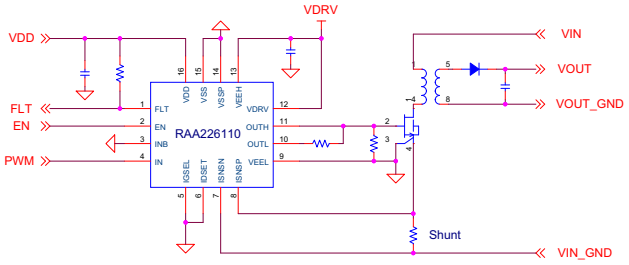


Figure 1. Typical Non-Inverting Input

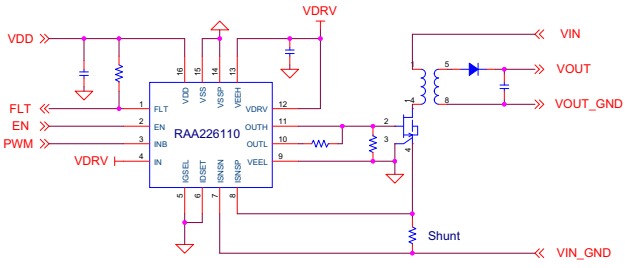


Figure 2. Typical Inverting Input

Contents

1. Overview

1.1 Ordering Information

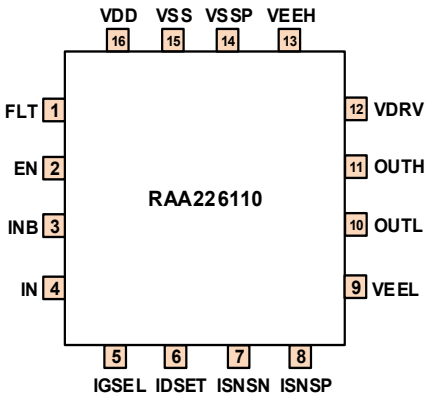
Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA2261104GNP#AA0	226110 04GNP	-40 to +125	-	16 Ld QFN	L16.4x4E
RAA2261104GNP#HA0	226110 04GNP	-40 to +125	6k	16 Ld QFN	L16.4x4E
RAA2261104GNP#MA0	226110 04GNP	-40 to +125	250	16 Ld QFN	L16.4x4E
RTKA226110DE0010BU	Half Bridge 0V Turn-Off Evaluation Board for the RAA226110				
RTKA226110DE0040BU	Half Bridge -3V Turn-Off Evaluation Board for the RAA226110				

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020
3. For Moisture Sensitivity Level (MSL), see the RAA226110 device page. For more information about MSL, see TB363.

1.2 Pin Configuration

16 Ld QFN
Top View



1.3 Pin Descriptions

Pin Number	Pin Name	Description
1	FLT	Open-drain fault output. Low indicates a no-fault condition. The FLT pin asserts high for Overcurrent Protection (OCP), Undervoltage Lockout (UVLO), and Over-Temperature Protection (OTP). Toggle the EN pin low to reset the FLT pin and the driver. Renesas recommends using a pull-up resistor value of 10kΩ. FLT can be pulled up to 3.3V, 5V, or higher. 18V is the highest recommended pull-up voltage.
2	EN	Driver output enable. Drive EN high to enable the driver. Driving EN low disables the driver and forces OUTL to a low state and OUTH to a Hi-Z state. EN can be driven with 3.3V, 5V, or higher. 18V is the highest recommended voltage. EN has an internal 90kΩ pull-down resistor to VSS.
3	INB	Inverting PWM input. OUT inverts the INB input logic level. INB is an edge triggered signal. Tie to VSS when using only IN. INB can be used as an enable function. Driving INB high disables the driver. INB can be driven with 3.3V, 5V, or higher. 18V is the highest recommended voltage. INB has an internal 180kΩ pull-up resistor to VDD.
4	IN	Non-inverting PWM input. IN is an edge triggered signal. Tie high when using only INB. IN can be used as an enable function. Driving IN low disables the driver. IN can be driven with 3.3V, 5V, or higher. 18V is the highest recommended voltage. IN has an internal 180kΩ pull-down resistor to VSS.
5	IGSEL	IGSEL selects the sourcing current for the OUTH pin. Connect IGSEL to VDRV for 0.3A. Connect IGSEL to VSS for 0.75A. Connect IGSEL to VSS through a 1MΩ resistor to select 2.0A.
6	IDSET	IDSET programs the OCP threshold voltage of the internal current sense comparator. Connect IDSET to VSS for 40mV threshold. Connect IDSET to VDRV for 120mV threshold. Connect IDSET to VSS through a 1MΩ resistor for 80mV threshold voltage.
7	ISNSN	Current sense input -
8	ISNSP	Current sense input +
9	VEEL	Gate turn-off voltage power supply. OUTL is connected to VEEL when the driver turns off. Connect to VSS for a 0V turn-off drive or -3V to -5V power supply for a negative drive.
10	OUTL	Output low pin that is the gate driver turn-off output. Connect to the gate of the GaN FET with a short, low inductance path.
11	OUTH	Output high pin that is the gate driver turn-on output. Connect to the gate of the GaN FET with a short, low inductance path.
12	VDRV	Internal 5.8V LDO output. Decouple with a 4.7µF capacitor to VSS.
13	VEEH	OUTL internal logic supply voltage. Connect to VDRV for 0V turn-off drive or VSS for negative turn-off drive.
14	VSSP	IC power ground. Connect to VSS on PCB.
15	VSS	IC analog ground. Connect to VSSP on PCB.
16	VDD	IC power supply. Supply with 6.5V to 18V power supply. Decouple with 10µF capacitor to VSS.
-	E pad	Thermal dissipation pad. Connect to VSS on the PCB.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DD}	-0.3	+24	V
IN, INB, EN, FLT	-0.3	+24	V
IGSEL, IDSET, ISNSN, ISNSP, VDRV	-0.3	+6.5	V
OUTH, OUTL	VEEL-0.3	VDRV+0.3	V
VEEH	-0.3	VEEL+6.5	V
VEEL	VEEH-6.5	+0.3	V
VSS, VSSP	-0.3	+0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	500		V
Charged Device Model (Tested per JS-002-2014)	750		V
Latch Up (Tested per JESD-78E; Class 2, Level A) at 125°C	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN Package (Notes 4, 5)	39	2.5

Notes:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board with direct attach features in free air. See TB379.
5. For θ_{JC}, the case temperature location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Case Operating Temperature Range	-40	+125	°C
V_{DD}	6.5	18	V
IN, INB, EN, FLT	0	18	V

2.4 Electrical Specifications

V_{DD} = 6.5V~18V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Unit
Power Supply						
Quiescent Supply Current	I_{DDQ}	V_{DD} = 6.5V~18V, IN = 0V, INB = V_{DD}		1.2	**2.0**	mA
Operating Supply Current	I_{DDO}	V_{DD} = 6.5V~18V, f_{PWM} = 500kHz		2.8	**3.5**	mA
Shutdown Supply Current	I_{DDSHD}	V_{DD} = 6.5V~18V		1.0	**2.0**	mA

V_{DD} = 6.5V~18V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Unit
Gate Drive Voltage						
VDRV Voltage	V_{DRV}	V_{DD} = 6.5V~18V	**5.5**	5.8	**6.0**	V
Current Limit of VDRV	I_{LIM}	V_{DD} = 6.5V, 12V, 18V; V_{DRV} drop 10%		80		mA
VDRV Dropout Voltage	VDO1	I_{DRV} = 10mA		40		mV
VDRV Dropout Voltage	VDO2	I_{DRV} = 30mA		140		mV
Undervoltage Lockout (UVLO) on V_{DRV}						
UVLO Rising Threshold	$V_{DRUVLOR}$	V_{DD} = 6.5V, 12V, 18V	**3.82**	3.92	**4.02**	V
UVLO Falling Threshold	$V_{DRUVLOF}$	V_{DD} = 6.5V, 12V, 18V	**3.62**	3.72	**3.82**	V
UVLO Hysteresis	$V_{DRUVLOH}$	V_{DD} = 6.5V, 12V, 18V		200		mV
Input Pins IN and INB						
High Level Threshold	V_{IH}		**2.5**			V
Low Level Threshold	V_{IL}				**1.6**	V
Input Hysteresis	V_{IHYS}			700		mV
IN Pull-Down Resistor	R_{IND}	IN to V_{DD}, measure I and calculate R		180		kΩ
INB Pull-Up Resistor	R_{INU}	IN to V_{SS}, measure I and calculate R		180		kΩ
Minimum Pulse Width	T_{PULSE_MIN}			20		nS
Input Pins EN						
High Level Threshold	V_{IH}		**2.3**			V
Low Level Threshold	V_{IL}				**1.0**	V
Input Hysteresis	V_{IHYS}			550		mV
EN Pull-Down Resistor	R_{IND}			90		kΩ
EN Falling Delay Time	t_{FALL_EN}			140		ns
EN Rising Delay Time	t_{RISE_EN}			170		ns
OUTH Output						
Peak Source Current	I_{SRC1}	C_L = 220nF, VDD = 6.5V and 18V, IGSEL = VDRV		0.3		A
Peak Source Current	I_{SRC2}	C_L = 220nF, VDD = 6.5V and 18V, IGSEL = GND		0.75		A
Peak Source Current	I_{SRC3}	C_L = 220nF, VDD = 6.5V and 18V, IGSEL = 1MΩ to GND		2.0		A
Driver Output Resistance	r_{ONP1}	I_{OUTH} = 45mA, IGSEL = VDRV,		11		Ω
Driver Output Resistance	r_{ONP2}	I_{OUTH} = 45mA, IGSEL = GND		4		Ω
Driver Output Resistance	r_{ONP3}	I_{OUTH} = 45mA, IGSEL = 1MΩ to GND		1.6		Ω
Output Leakage Current	I_{LKP}	OUTH = 0V, VDD = 6.5V and 18V	**-15**	0.25	**15**	nA
OUTL Output						
Peak Sink Current	I_{SNK}	C_L = 220nF, VDD = 6.5V and 18V, VEEL = 0V, VEEH = VDRV		3.0		A
		C_L = 220nF, VDD = 6.5V and 18V, VEEL = -3V, VEEH = V_{SS}		1.2		A

V_{DD} = 6.5V~18V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Unit
Driver Output Resistance	r_{ONN}	C_L = 220nF, VDD = 6.5V and 18V, VEEL = 0V, VEEH = VDRV		1.2		Ω
		C_L = 220nF, VDD = 6.5V and 18V, VEEL = -3V, VEEH = GND		2.5		Ω
Switching Characteristics						
Turn-On Propagation Delay	t_{DON}	C_L = 1000pF		20		ns
Turn-Off Propagation Delay	t_{DOFF}	C_L = 1000pF		20		ns
Rise Time (10% to 90%)	t_{RISE}	C_L = 200pF		2.0		ns
		C_L = 1500pF		6.5		ns
		C_L = 10000pF		30		ns
Fall Time (90% to 10%)	t_{FALL}	C_L = 200pF		2.0		ns
		C_L = 1500pF		6.0		ns
		C_L = 10000pF		31		ns
Overcurrent Protection (Equation 1)						
OCP Comparator Threshold	OCP_{TH1}	IDSET = VDRV	**107**	120	**130**	mV
OCP Comparator Threshold	OCP_{TH2}	IDSET = 1MΩ to GND	**70**	80	**90**	mV
OCP Comparator Threshold	OCP_{TH3}	IDSET = GND	**30**	40	**50**	mV
OCP Response Time	OCP_{RESP}		**60**	80	**105**	ns
Fault Pin						
Low Level Voltage	FLT_{VOL}	Sink Current = 3mA			**0.4**	V
High Level Leakage	FLT_{LKG}	VPULLUP = 18V	**-1**	0.01	**1**	µA
FLT Pin Delay	FLT_{DLY}			45		us
Over-Temperature Protection						
Temperature Shutdown	T_{SHDN}			185		°C
Temperature Shutdown Hysteresis	$T_{SHDNHYS}$			20		°C

Note:
6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

2.5 Timing Diagrams

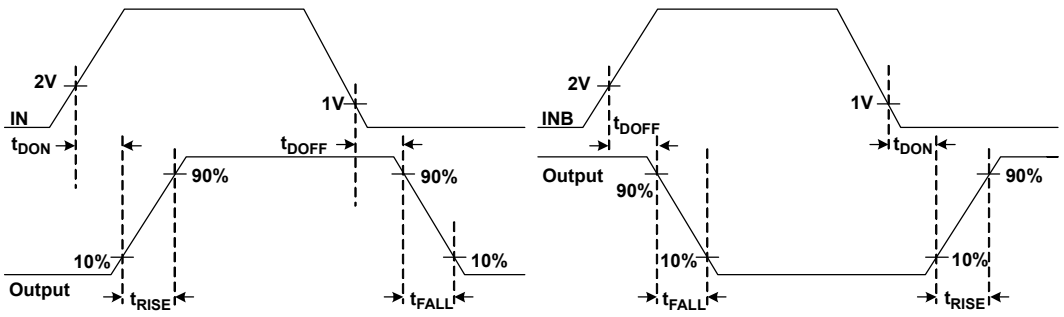


Figure 3. Timing Diagram

The RAA226110 gate source and sink current capability are tested based on Figure 4 and Figure 5 circuits.

Source current capability is tested as shown in Figure 4.

1. Connect a 300mΩ current shunt resistor in series with 100µF capacitor between OUTH and VEEL.
2. Measure the current shunt resistor actual resistance.
3. Discharge the 100µF capacitor to VEEL.
4. Send a 1µs pulse to turn on the driver. Measure the voltage across the 300mΩ current shunt resistor.
5. Use the voltage across the resistor and its exact value to calculate the source current.

Sink current capability is tested as shown in Figure 5.

1. Connect a 300mΩ current shunt resistor in series with 100µF capacitor between OUTL and VEEL.
2. Charge the 100µF capacitor to VDRV.
3. Send a 1µs pulse to turn off the driver (through INB). Measure the voltage across the 300mΩ current shunt resistor.
4. Use the voltage across the resistor and its exact value to calculate the sink current.

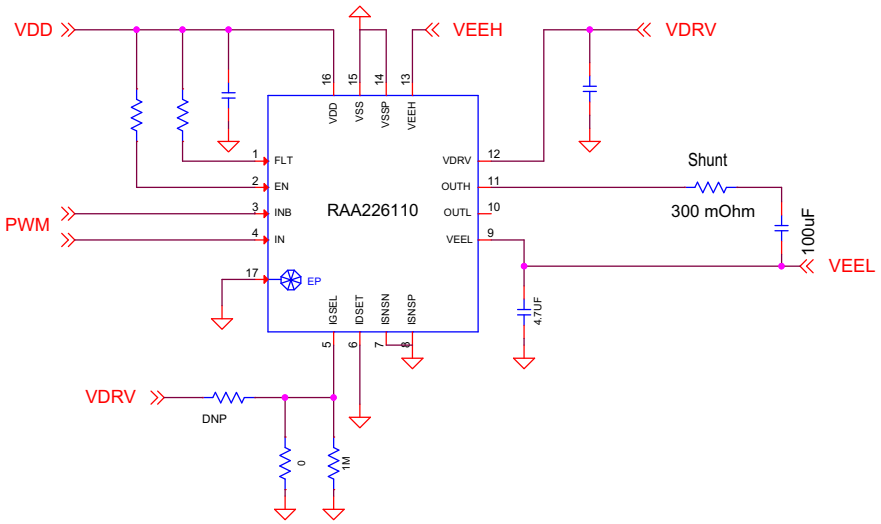


Figure 4. Gate Source Current Measurement

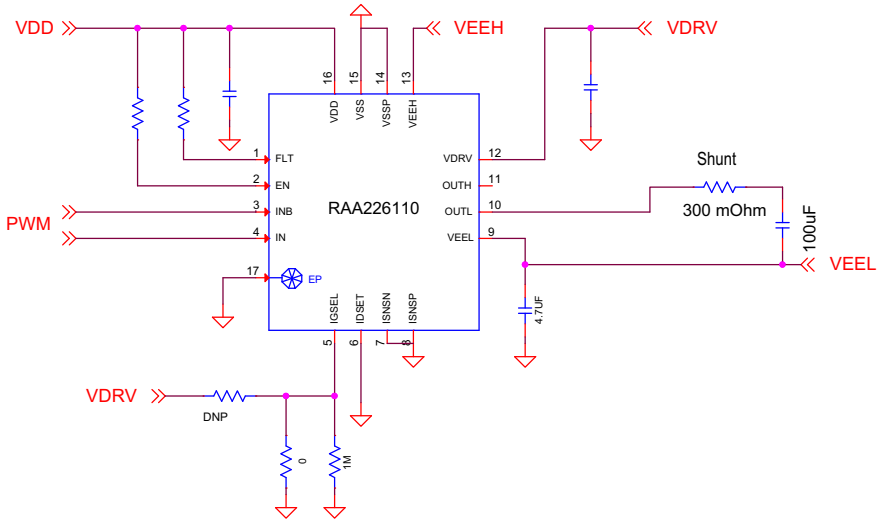


Figure 5. Gate Sink Current Measurement

3. Typical Performance Curves

V_{DD} = 6.5V, 18V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL, unless otherwise noted.

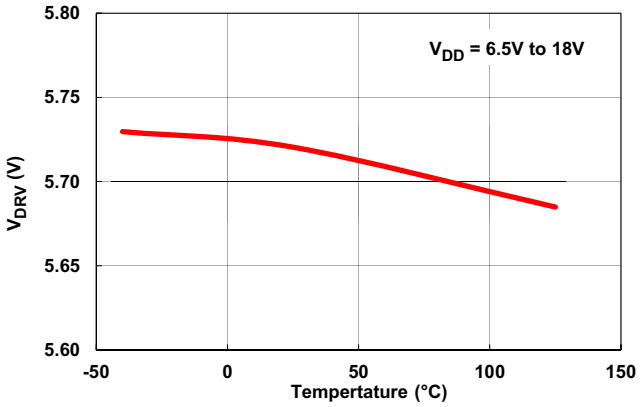


Figure 6. V_{DRV} vs Temperature

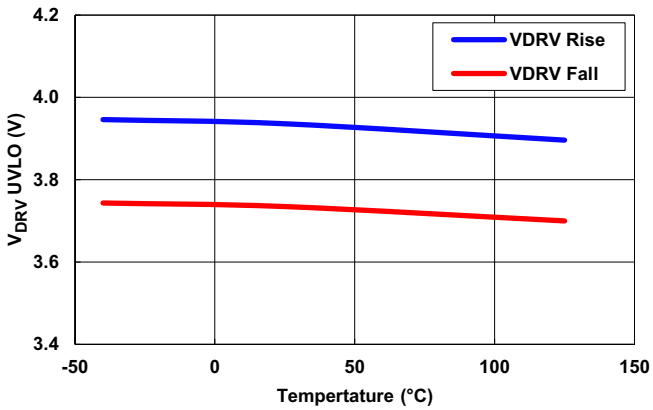


Figure 7. V_{DRV} UVLO vs Temperature

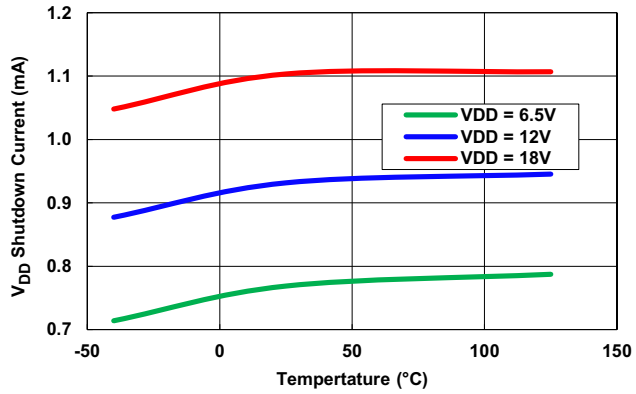


Figure 8. Shutdown Current vs Temperature

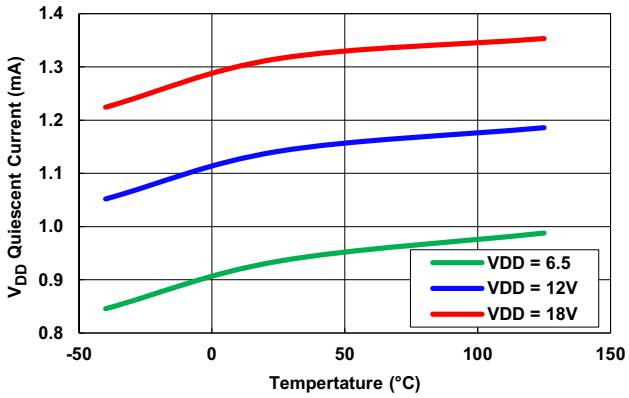


Figure 9. Quiescent Current vs Temperature

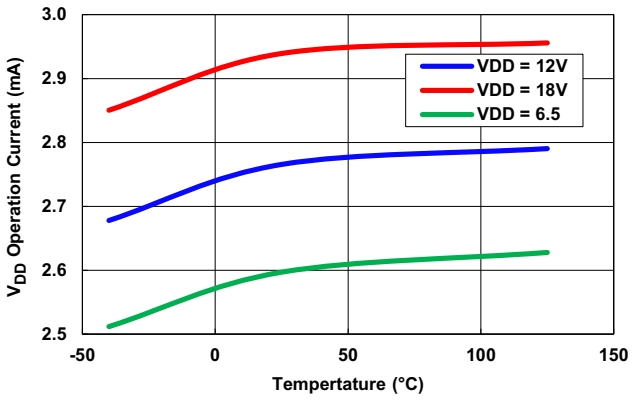


Figure 10. V_{DD} Operation Current vs Temperature

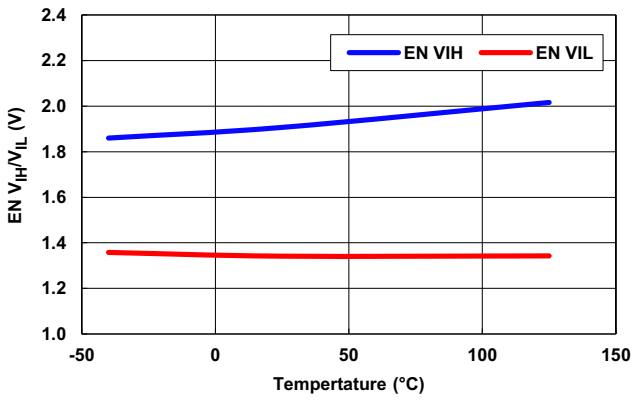


Figure 11. EN V_{IL} and V_{IH} vs Temperature

V_{DD} = 6.5V, 18V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL, unless otherwise noted. **(Continued)**

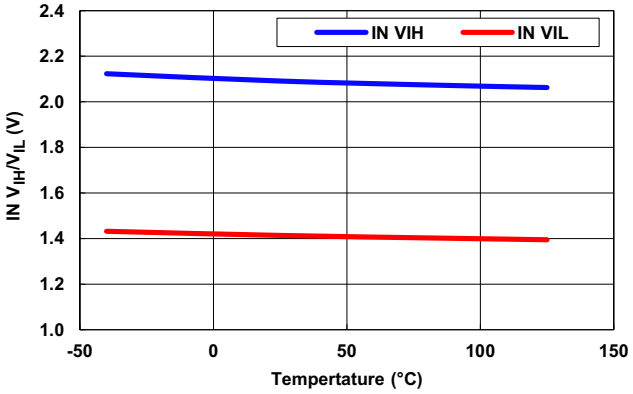


Figure 12. IN V_{IL} and V_{IH} vs Temperature

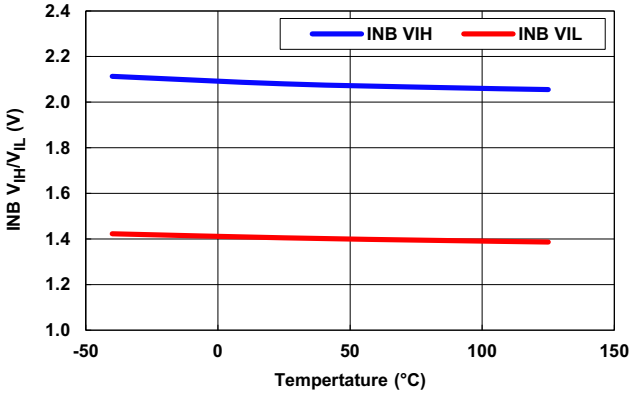


Figure 13. INB V_{IL} and V_{IH} vs Temperature

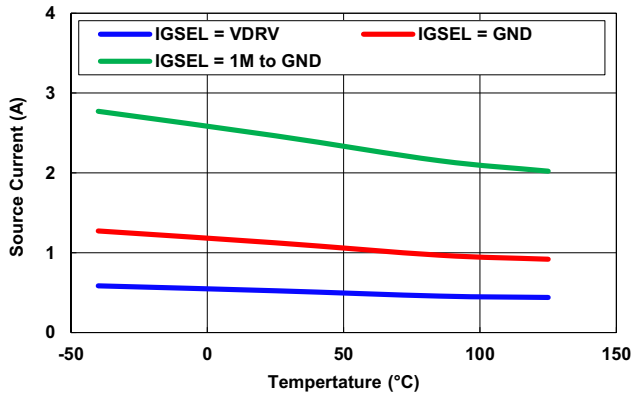


Figure 14. Source Current vs Temperature

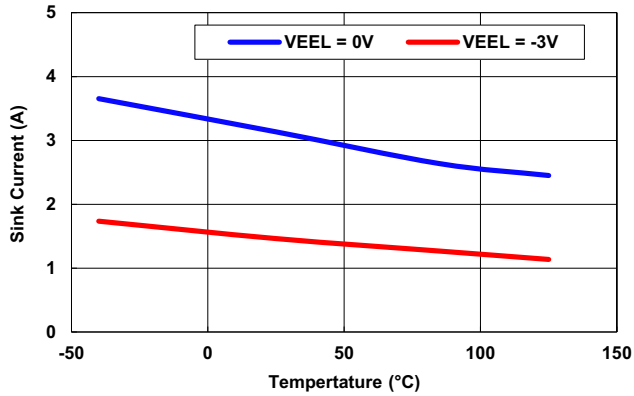


Figure 15. Sink Current vs Temperature

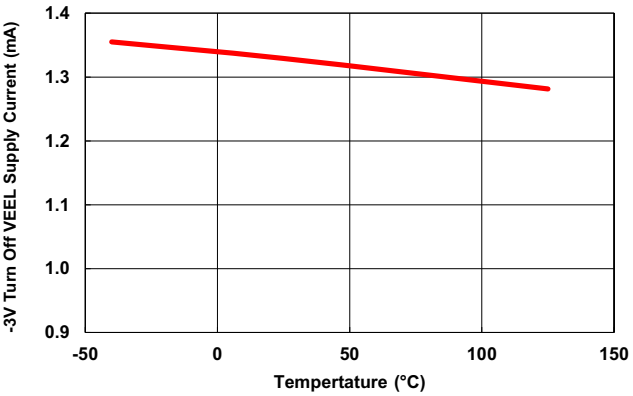


Figure 16. VEEL Supply Current vs Temperature

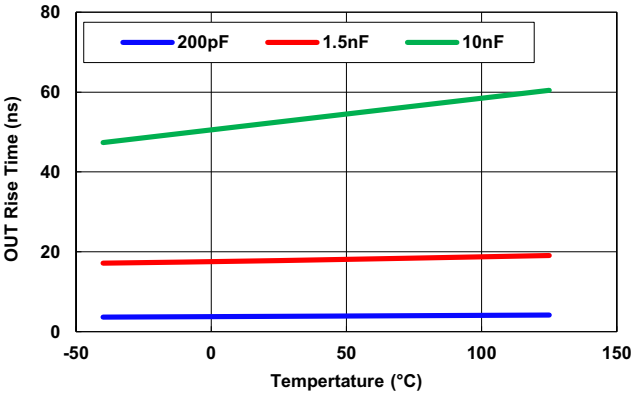


Figure 17. OUT Rise Time vs Temperature (Source Current: 2A)

V_{DD} = 6.5V, 18V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL, unless otherwise noted. **(Continued)**

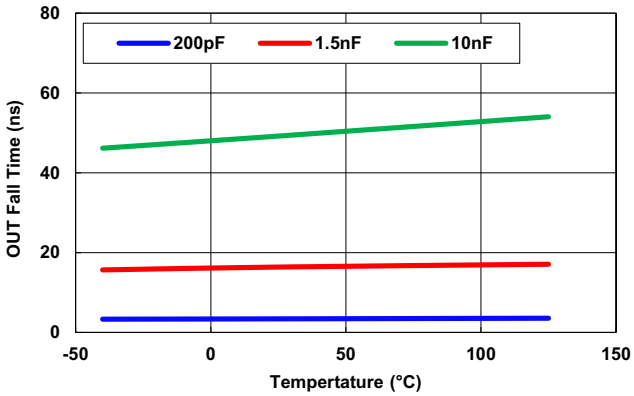


Figure 18. OUT Fall Time vs Temperature (0V Turn-Off)

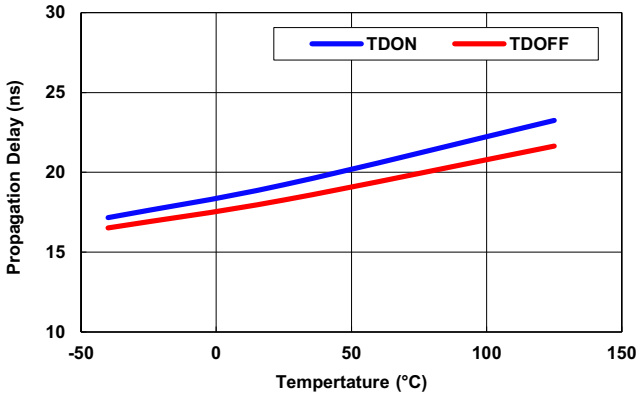


Figure 19. IN Propagation Delay vs Temperature

4. Functional Description

4.1 Gate Drive for Enhancement N-Channel GaN FETs

New technologies based on wide-bandgap semiconductors produce High Electron Mobility Transistors (HEMT). An example of HEMT is the GaN-based power transistors such as the GS66508B and GS66516T, which offer low $r_{DS(ON)}$ and gate charge (Qg). These attributes make the devices capable of supporting high switching frequency operation without suffering significant efficiency loss. However, GaN power FETs have special gate drive requirements that the RAA226110 is specifically designed to address.

The following are key properties of a gate driver for GaN FETs:

- Gate drive signals need to be sufficiently higher than the V_{GS} threshold specified in GaN FET datasheets for proper operation.
- A well-regulated gate drive voltage keeps the V_{GS} lower than the specified absolute maximum level of 6V.
- Split pull-up and pull-down gate connections add series gate resistors to independently adjust turn-on and turn-off speed without the need for a series diode with a voltage drop that may cause an insufficient gate drive voltage.
- Driver low pull-down resistance eliminates undesired Miller turn-on.
- High source/sink current capability and low propagation delay achieve high switching frequency operation.

4.2 Functional Overview

The RAA226110 is a single channel high-speed enhancement-mode GaN FET driver.

The RAA226110 has a wide operating supply range of 6.5V to 18V. The gate drive voltage is generated from an internal linear regulator to keep the gate-to-source voltage below the absolute maximum level of 6V.

The input stage can handle inputs to 18V independent of V_{DD} and has both inverting and non-inverting inputs. The split output stage can source and sink high currents and allows for independent adjustment of the turn-on and turn-off speeds. The typical propagation delay of 20ns enables high switching frequency operation.

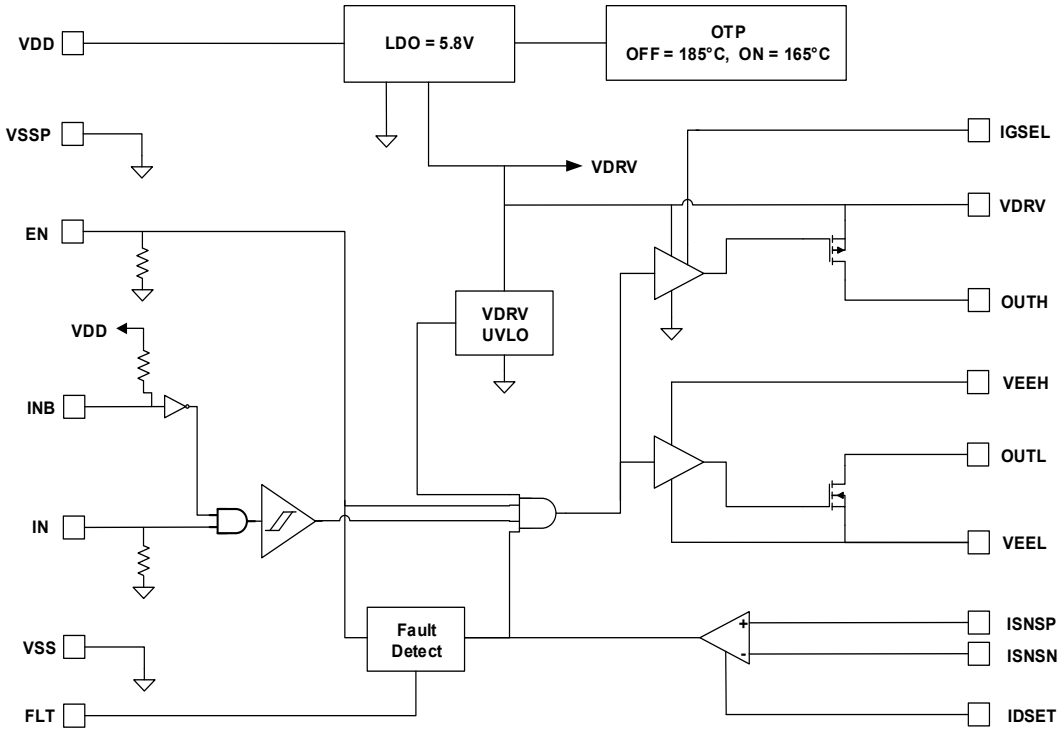


Figure 20. Logic Diagram

5. Applications Information

5.1 Undervoltage Lockout

The VDD pin accepts a recommended supply voltage range from 6.5V to 18V and is the input to the internal linear regulator. VDRV is the 5.8V output of the regulator. VDRV provides the bias for all internal circuitry and the gate drive turn-on voltage for the output stage.

A UVLO circuitry monitors the voltage on VDRV and is designed to prevent unexpected glitches on VDRV when VDD is being turned on or turned off. When VDRV < UVLO, an internal 500Ω resistor is connected between OUTH and VEEL, which helps keep the gate voltage close to ground. Also, OUTL is shorted to VEEL through the internal power NFET. This ensures the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates from the Miller capacitance.

When VDRV > UVLO, the output is ready to respond to the logic inputs following the next rising edge on IN or falling edge on INB. In the non-inverting operation (PWM signal applied to the IN pin) the output is in phase with the input. In the inverting operation (PWM signal applied to the INB pin), the output is out of phase with the input.

For the negative transition of V_{DD} through the UVLO voltage, when VDRV < 3.7V, OUTH is connected to VEEL with 500Ω resistor internally. OUTL is shorted to VEEL through the internal power NFET, regardless of the input logic states.

To ensure an off-state during power-up and power-down, Renesas recommends using a 3.3kΩ resistor between the GaN FET gate and VEEL on the PCB.

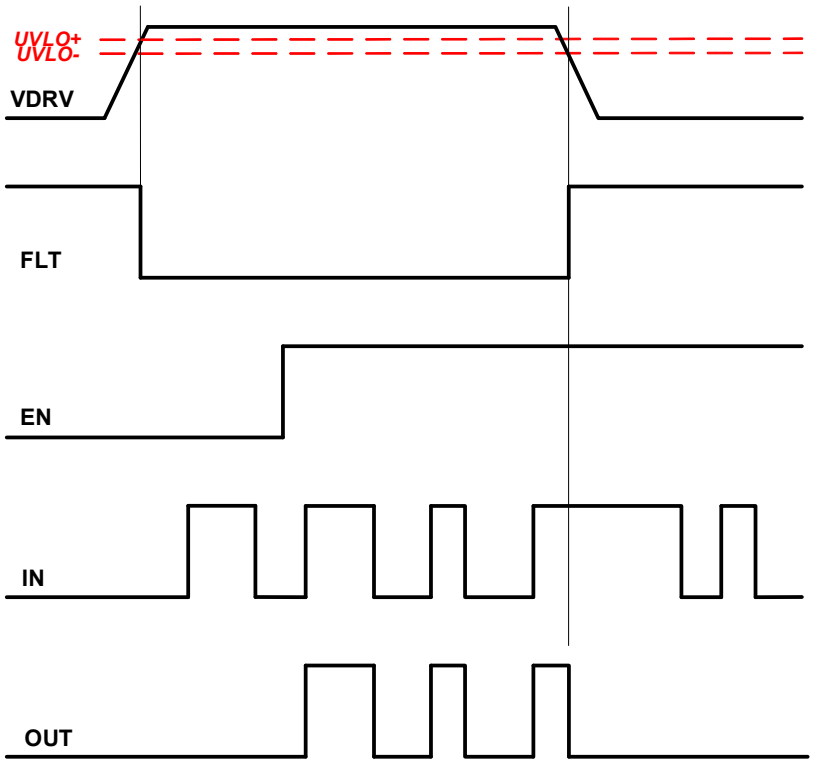


Figure 21. VDRV UVLO Logic Diagram

5.2 Input Stage

The RAA226110 input thresholds are based on a TTL and CMOS compatible input threshold logic that is independent of the supply voltage. The PWM input is recognized as low when the IN/INB input is lower than 1.6V. The PWM input is recognized as high when the IN/INB input is higher than 2.5V. The logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V, 5V, or higher voltage power controllers.

The RAA226110 offers both inverting and non-inverting inputs. The IN and INB pins are designed as edge-triggered signals. The state of the output pin is dependent on the bias on both input pins at the rising and falling edges. Table 1 summarizes the input to output relationships.

Table 1. Truth Table

IN	INB	EN	OUT (Note 7)	OUTH	OUTL
X	X	0	0	Hi-Z	0
X	1	X	0	Hi-Z	0
0	X	X	0	Hi-Z	0
0	0	1	0	Hi-Z	0
1	0	1	1	1	Hi-Z
1	1	1	0	Hi-Z	0

Note:
7. OUT is the combination of OUTH and OUTL connected together. Hi-Z represents a high impedance state.

As a protection mechanism, if any of the input pins are left in a floating condition, OUTL is held in the low state and OUTH is high impedance. This state is achieved using a 180kΩ pull-up resistor on the INB pin to VDD, a 180kΩ pull-down resistor on the IN pin to VSS, and a 90kΩ pull-down resistor on the EN pin to VSS. For proper operation in non-inverting applications, connect INB to VSS. For proper operation in inverting applications, connect IN to VDD.

5.3 Enable Function

The RAA226110 input thresholds are based on a TTL and CMOS compatible input threshold logic that is independent of the supply voltage. The EN input is recognized as low when the EN voltage is lower than 1.0V. The EN input is recognized as high when the EN voltage is higher than 2.3V. The logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V and 5V power controllers.

- In a non-inverting configuration, the INB pin can be used to implement the enable/disable function. OUT (OUTH connected to OUTL) is enabled when INB is biased low, acting as an active-low enable pin.
- In an inverting configuration, the IN pin can be used to implement the enable/disable function. OUT is enabled when IN is biased high, acting as an active-high enable pin.

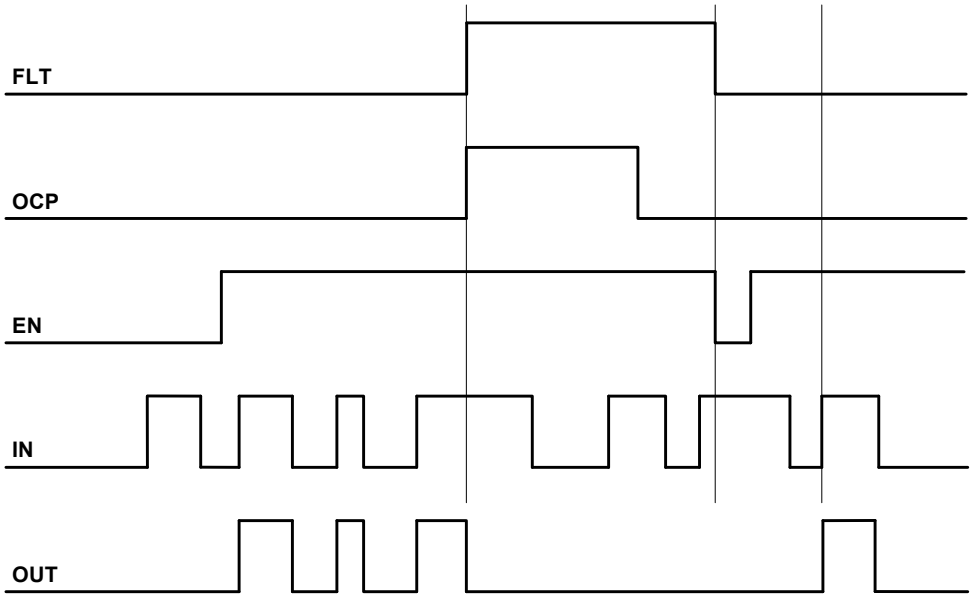


Figure 22. EN Logic Diagram

5.4 Power Sequencing RAA226110

Renesas recommends using the RAA226110 by tying the EN pin to an external MCU logic I/O for proper power sequencing control.

- The proper power turn-on sequence is:
  1. Supply V_{DD} (V_{DD} and negative power supply for negative drive)
  2. The EN pin pulled high to enable the driver
  3. Send PWM to IN/INB
- The proper power turn-off sequence is:
  1. Remove PWM from IN/INB
  2. The EN pin pulled low to disable the driver
  3. Remove V_{DD} (V_{DD} and negative power supply for negative drive)

Renesas does not recommend inputting a PWM on IN/INB before V_{DD}. If this recommendation is not followed, place a 220nF filter capacitor between EN and VSS.

In the negative drive application, Renesas recommends supplying the V_{DD} and negative power supply at the same time or V_{DD} before a negative power supply. If a negative power supply is supplied before V_{DD}, it is not permitted to put a load between VDRV and VEEL exceeding 40mA.

5.5 IGSEL and IDSET Configuration

5.5.1 IGSEL Configuration

IGSEL configures the OUTH source current. The source current is 0.3A when IGSEL is connected to VDRV. The source current is 0.75A when IGSEL is connected to VSS. The source current is 2A when IGSEL is connected to VSS with a 1MΩ resistor. To further increase the flexibility of adjusting the turn-on speed, the turn-on resistor can be placed between OUTH and Gate of the GaN FET. Adjust the turn-off speed by the turn-off resistor between OUTL and Gate of the GaN FET.

Table 2. IGSEL Configuration

IGSEL	VDRV	VSS	1M Resistor to VSS
Gate source current	0.3A	0.75A	2A

5.5.2 IDSET Configuration

IDSET configures the OCP trigger point voltage level between ISNSP and ISNSN. The trigger point voltage level is 40mV when IDSET is connected to VSS. The trigger point voltage level is 80mV when IDSET is connected to VSS with a 1MΩ resistor. The trigger point voltage level is 120mV when IDSET is connected with VDRV. Renesas recommends using a Low parasitic inductance current shunt resistor to decrease the noise in the OCP circuit to ISNSP and ISNSN. When OCP triggers, the RAA226110 shuts down immediately. OUTL toggles to low regardless of the state of IN or INB. FLT goes high.

Table 3. IDSET Configuration

IDSET	VDRV	VSS	1M Resistor to VSS
OCP inside comparator trigger point	120mV	40mV	80mV

For example, if the current sense resistor is 1mΩ and IDSET is connected to VSS, Equation 1 shows how to calculate the OCP trigger current.

(EQ. 1) $$OCP = \frac{40mV}{1m\Omega} = 40A$$

5.6 Over-Temperature Protection

RAA226110 has an internal over-temperature protection function. When the IC junction temperature exceeds 185°C, the over-temperature protection triggers and shuts down the IC. OUTL is pulled to VEEL voltage and the FLT pin toggles high. As long as the load current is within specification, VDRV continues to operate as normal.

RAA226110 has an internal LDO to convert VDD to VDRV = 5.8V. Although VDRV can be used to drive an external load, the load current must be within the specifications stated in the Electrical Specifications table.

Note: When over-temperature protection has triggered, Renesas recommends turning off the external VDRV load to protect the IC from further over-heating.

5.7 Driver Power Dissipation

The RAA226110 power dissipation is dominated by the losses associated with the gate charge of the driven bridge FETs and the switching frequency. The internal bias current also contributes to the total dissipation but is usually not significant compared to the gate charge losses.

The driver total power dissipation includes the quiescent loss, the voltage drop loss inside the LDO, the turn-on loss and the turn-off loss inside the driver. Use Equation 2 to calculate the power dissipation of the driver. The driver junction temperature is calculated using Equation 3.

(EQ. 2)
$$P_{Total} = P_{Quiescent} + P_{LDO(Vdrop)} + P_{Turn(ON-inside)} + P_{Turn(OFF-inside)}$$
$$= P_{Quiescent} + (P_{Turn(ON)} + P_{Turn(OFF)}) \bullet \frac{VDD - V_{DRV}}{V_{DRV}} + P_{Turn(ON-inside)} + P_{Turn(OFF-inside)} = VDD \bullet I_{DDQ}$$
$$+ (Q_c \bullet f_s \bullet V_{GS}) \bullet \frac{V_{DRV}}{V_{DRV} - VEEL} \bullet \frac{VDD - V_{DRV}}{V_{DRV}} + \frac{1}{2} Q_c \bullet f_s \bullet V_{GS} \bullet \frac{R_{OUTH}}{R_{OUTH} + R_{ON}} + \frac{1}{2} Q_c \bullet f_s \bullet V_{GS} \bullet \frac{R_{OUTL}}{R_{OUTL} + R_{OFF}}$$
$$+ Duty \bullet (VDD - V_{DRV}) \bullet \frac{V_{DRV}}{R_{pulldown}}$$

(EQ. 3)
$$T_{Junction} = P_{Total} \bullet \Theta_{JA} + T_A$$

where:

- $P_{LDO(Vdrop)}$ = LDO power loss inside the driver
- $P_{Turn(ON-inside)}$ = Turn-on loss inside the driver
- $P_{Turn(OFF-inside)}$ = Turn-off loss inside the driver
- $P_{Turn(ON)}$ = Turn-on loss inside the driver and the outside gate resistor turn-on loss
- $P_{Turn(OFF)}$ = Turn-off loss inside the driver and the outside gate resistor turn-off loss
- f_s = Switching frequency
- $V_{GS} = V_{DRV}$ - VEEL
- Q_c = Gate charge for V_{GS}
- R_{ON} = Outside gate driver ON-resistance
- R_{OFF} = Outside gate driver OFF-resistance
- R_{OUTH} = OUTH inside resistor
- R_{OUTL} = OUTL inside resistor
- R_{OUTL} = OUTL inside resistor
- T_A = Ambient temperature
- θ_{JA} = Thermal resistance from junction to ambient
- Duty = Duty cycle of the power switch

- $R_{pulldown}$ = Gate pull-down resistor outside the driver. 3.3kΩ is a common value for this resistor.

Note: The gate power dissipation is proportionally shared with the external gate resistor. Do not overlook the power dissipated by the external gate resistor.

5.8 Typical Application Diagrams

The RAA226110 provides for several types of PWM input configurations.

The IN pin can be used as a non-inverting PWM input. Both EN and INB can be used as enable pins when IN is configured as a PWM input. If EN is used for the enable function, toggle EN from low to high to reset RAA226110 when OCP triggers. If INB is used for the enable function, INB cannot reset RAA226110 when OCP triggers. Toggle EN low to high or power cycle RAA226110. For a fast enable and disable response time requirement application, INB can be used as an enable pin that responds faster than EN.

The INB pin can be used as an inverting PWM input. Both EN and IN can be used as enable functions when INB is configured as a PWM input. If EN is used as an enable function, toggle EN low to high to reset RAA226110 after OCP triggers. If IN is used as an enable function, IN cannot reset RAA226110 when OCP is triggered. Toggle EN low to high or power cycle RAA226110. In a fast enable and disable response time requirement application, IN can be used as an enable pin that responds faster than EN.

Figure 23 shows a typical non-inverting 0V turn-off boost application. Gate source current capability is configured by the IGSEL pin. Sink current can be adjusted by changing the resistor connected to OUTL. The OCP trigger comparator threshold voltage is configured by the IDSET pin. The OCP trigger current is sensitive to the voltage signal across the 1mΩ current sense resistor. For improved noise immunity, Renesas recommends using a low ESL shunt resistor. ROHM PML100HZPJV1L0 provides good performance for this application. Renesas recommends using a differential or common-mode filter to filter the noise signal in the current shunt resistor. The differential mode filter (R1 = 5.6Ω, C3 = 22pF, R2 = 0Ω, C1 and C2 DNP) is effective in most applications. In some applications the common-mode filter (R1 = R2 = 8.2Ω, C1 = C2 = 820pF, C3 DNP) provides better performance than the differential mode filter.

In the 0V turn-off voltage application, connect VEEH to VDRV and connect VEEL to 0V as shown in Figure 23.

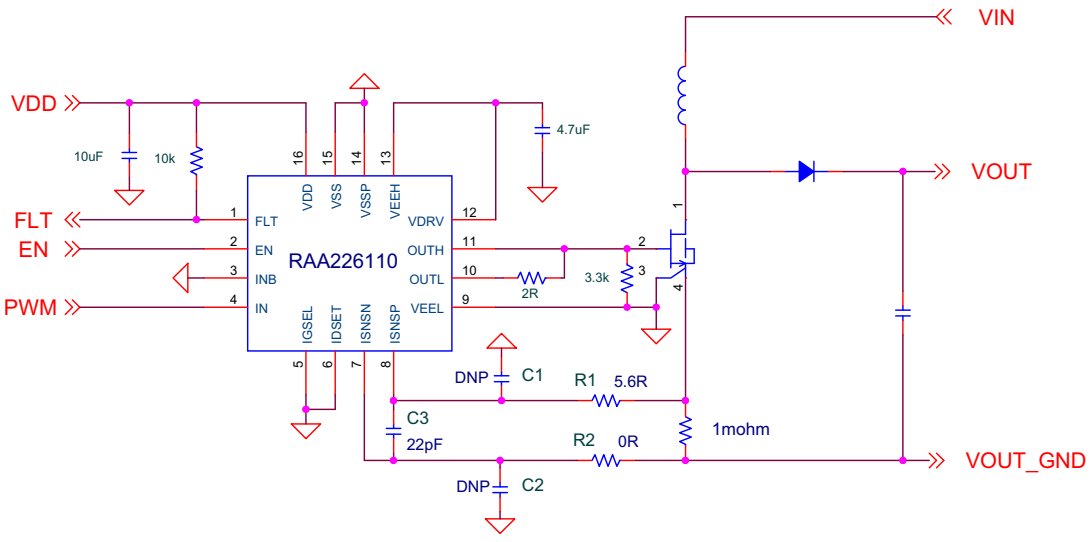


Figure 23. Non-Inverting 0V Turn-Off Boost Application

When RAA226110 is configured for negative drive, supply VDD with 6.5V to 18V and supply VEEL with -3V to -5V.

Connect VEEH to VSS for the negative drive application. Figure 24 shows how to generate VDD and negative voltage (-3V~-5V) with one 12V power supply. With the 12V power supply connected between net (VDD = 9V) and net (-3V), put a 9V Zener in series with 300Ω between (VDD = 9V) and (-3V). The anode of the Zener is the GND net. The 9V (VDD = 9V), GND, and -3V (-3V) bias voltages are provided by this configuration.

Table 4. Turn-Off Drive Voltage VEEH / VEEL Configuration

Turn-Off Drive Voltage	0V Turn-Off	Negative Turn-Off
VEEH	VDRV	0V
VEEL	0V	-3V ~ -5V

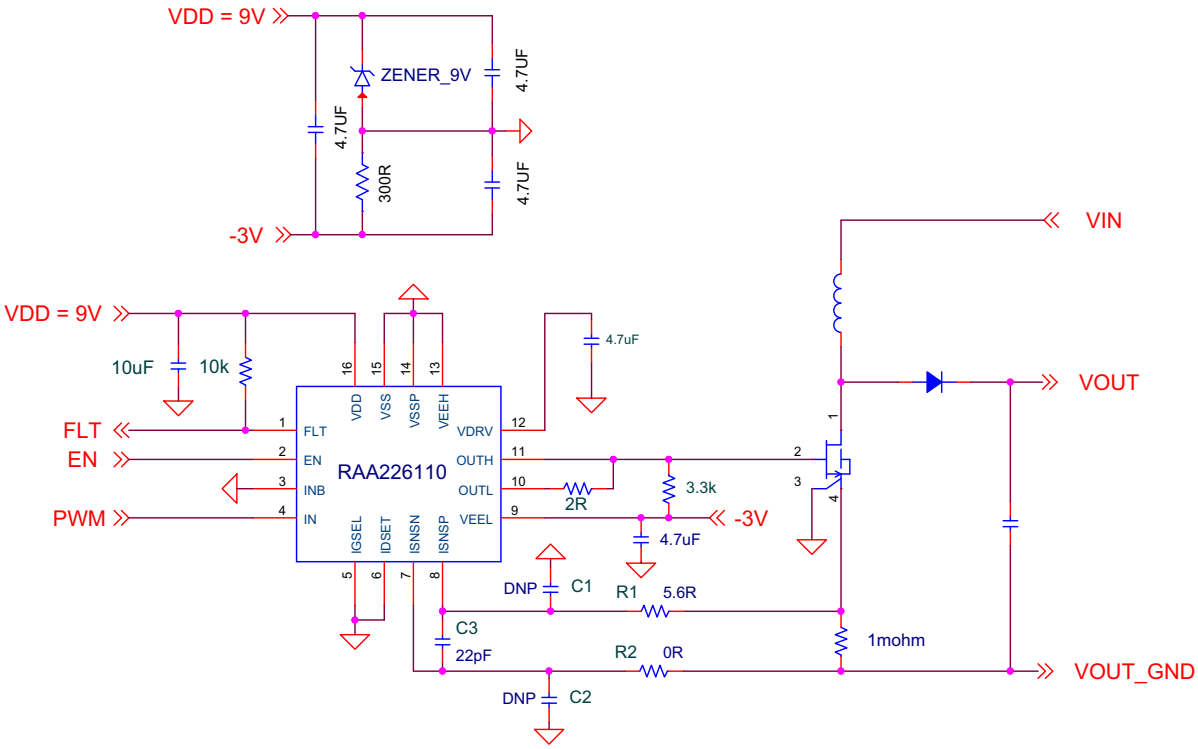


Figure 24. Non-Inverting -3V Turn-Off Boost Application

When RAA226110 is configured as an inverting PWM input and 0V turn-off, pull IN high to VDRV or VDD. The PWM is sent to INB, VEEH is connected to VDRV, and VEEL is connected to 0V as shown in Figure 25.

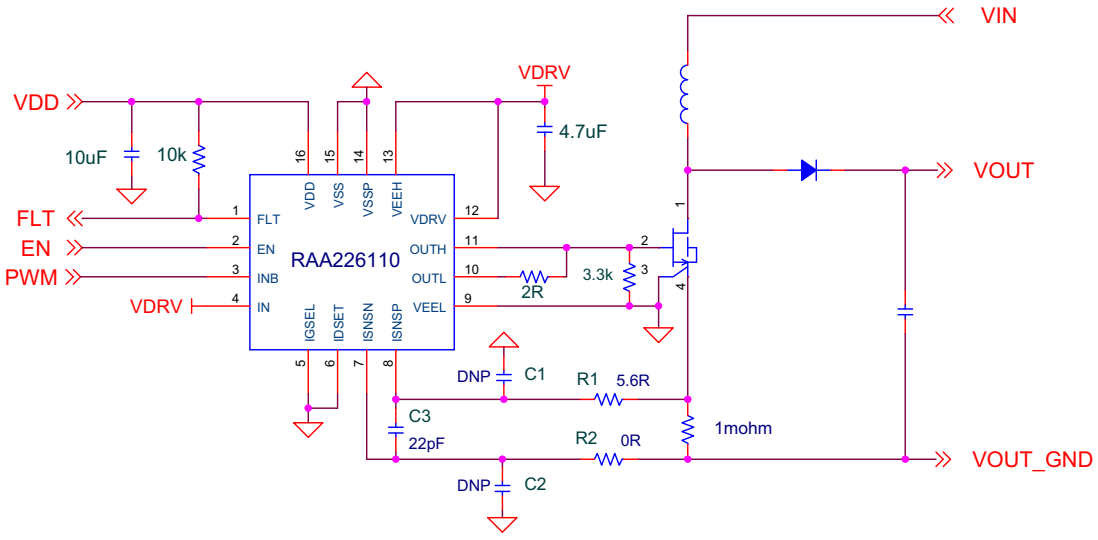


Figure 25. Inverting 0V Turn-Off Boost Application

When RAA226110 is configured as an inverting PWM with a negative drive, pull IN high to VDRV or VDD. The PWM is sent to INB, VEEH is connected to VSS, and VEEL is connected to -3V voltage source as shown in Figure 26.

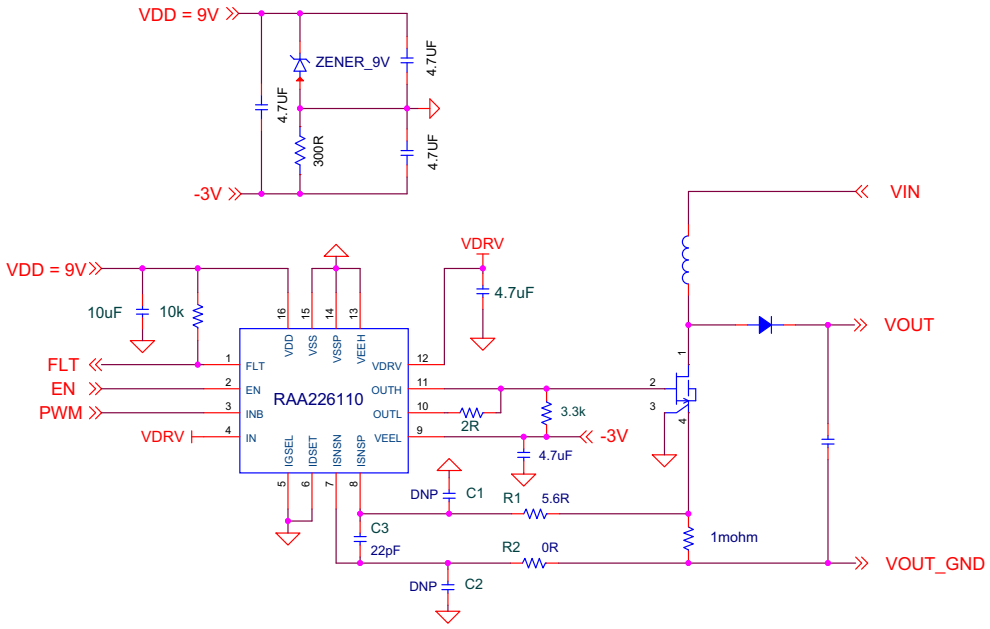


Figure 26. Inverting -3V Turn-Off Boost Application

When RAA226110 is configured as an inverting PWM half bridge with a negative drive. The recommended application is shown in Equation 27.

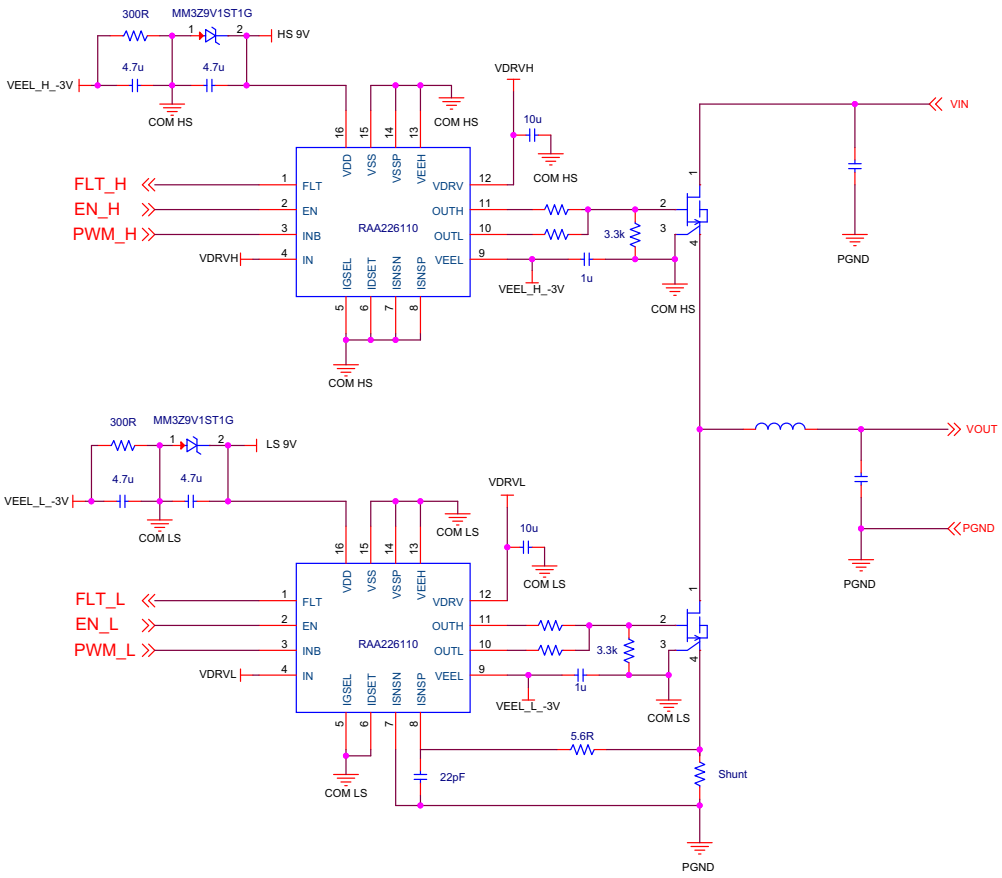


Figure 27. Inverting -3V Turn-Off Half Bridge Application

5.9 PCB Layout Considerations

The RAA226110 AC performance depends significantly on the Printed Circuit Board (PCB) design. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET induce significant voltage transients on the associated traces
- Keep power loops as short as possible by paralleling the source and return traces
- Use planes where practical. They are usually more effective than parallel traces
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt induces currents and consequently, noise voltages in the low level signal lines
- When practical, minimize impedances in low level signal circuits. The noise that is magnetically induced on a 10kΩ resistor is 10 times larger than the noise on a 1kΩ resistor
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in the magnetic cores of these structures are especially bad for emitting flux
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended
- Use decoupling capacitors to reduce the influence of parasitic inductance in the VDRV, VDD, and GND leads. To be effective, these capacitors must also have the shortest possible conduction paths. If using vias, connect several paralleled vias to reduce the inductance of the vias
- It may be necessary to add resistance to dampen resonating parasitic circuits, especially on OUTH. If an external gate resistor is unacceptable, the layout must be improved to minimize lead inductance
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the RAA226110
- Avoid placing a signal ground plane under a high amplitude dv/dt circuit. This injects di/dt currents into the signal ground paths
- Calculate power dissipation and voltage drop for the power traces. Many PCB/CAD programs have built-in tools for calculating trace resistance
- Large power components (such as power FETs, electrolytic caps, and power resistors) have internal parasitic inductance that cannot be eliminated
- If the circuits are simulated, consider including parasitic components, especially parasitic inductance
- The GaN FETs have a separate substrate connection that is internally tied to the source pin. The source and substrate should be at the same potential. Limit the inductance in the OUTH/L to Gate trace by keeping it as short and wide as possible.

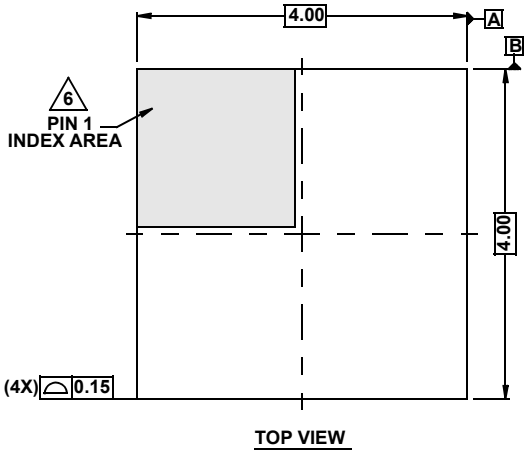
6. Revision History

Rev.	Date	Description
1.00	Sep.15.20	Initial release.

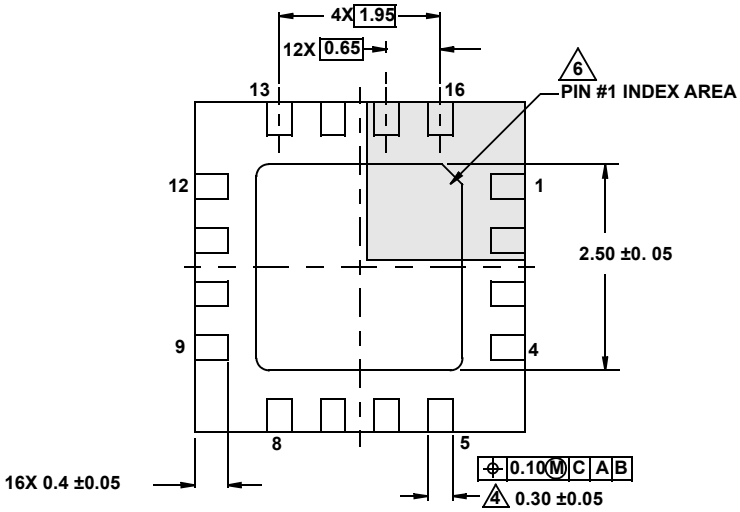
7. Package Outline Drawing

For the most recent package outline drawing, see L16.4x4E.

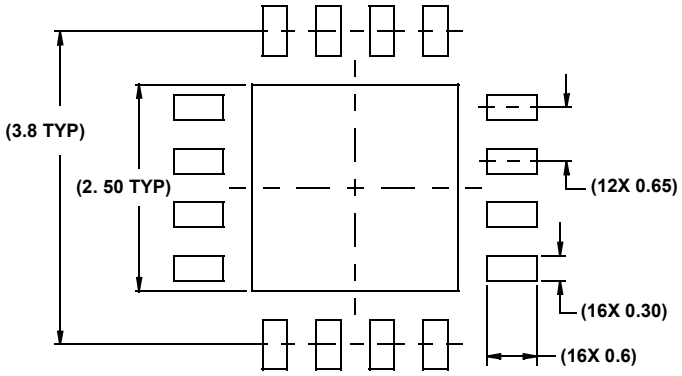
L16.4x4E
16 Lead Quad Flat No-lead Plastic Package
Rev 0, 4/08



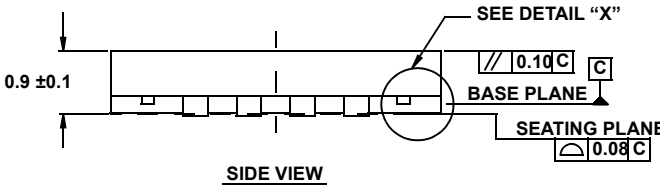
TOP VIEW



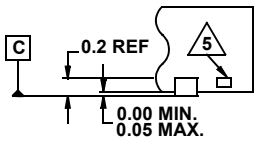
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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(Rev.1.0 Mar 2020)

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