# CIPOS™ Mini

## IGCM06F60GA

## Description

The CIPOS™ module family offers the chance for integrating various power and control components to increase reliability and optimize PCB size and system cost. It is designed to control 3-phase motors in variable speed drives. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also less EMI and overload protection. To deliver excellent electrical performance, Infineon's leading-edge RC-Drives IGBTs are combined with an optimized SOI gate driver.

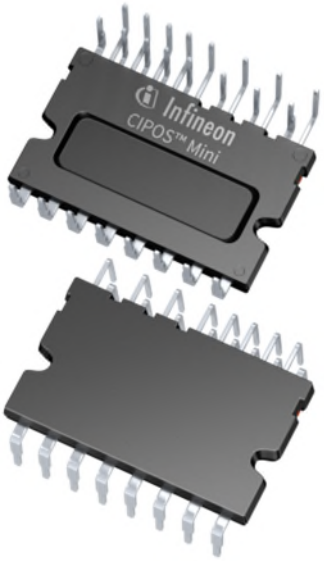
## Features

Package

- Fully isolated dual in-line molded module
- Lead-free terminal plating; RoHS compliant

Inverter

- Reverse Conducting Drives IGBTs
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative $V_S$ potential up to -11 V for signal transmission at $V_{BS}$ = 15 V
- Integrated bootstrap functionality
- Overcurrent shutdown
- Built-in NTC thermistor for temperature monitor
- Undervoltage lockout at all channels
- Low-side emitter pins accessible for phase current monitoring (open emitter)
- Cross-conduction prevention
- All of 6 switches turn off during protection




## Potential applications

- Home appliances, low power motor drives

## Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

**Table 1 Product Information**

| Base Part Number | Package Type | Standard Pack | | Remarks |
|---|---|---|---|---|
| | | Form | MOQ | |
| IGCM06F60GA | DIP 36x21 | 14 pcs / Tube | 280 pcs | |

# Table of contents

# 1 Internal Electrical Schematic

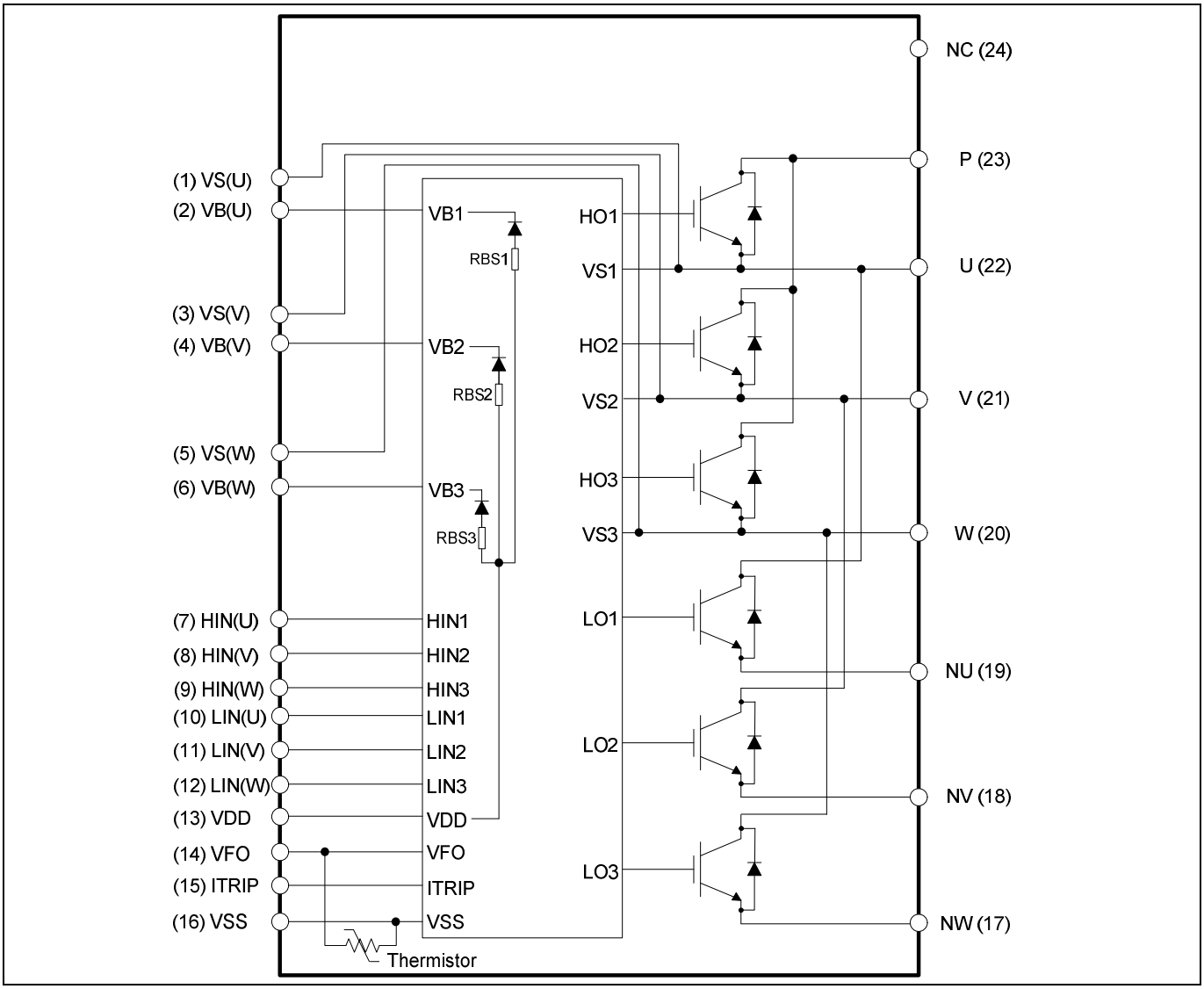



**Figure 1 Internal electrical schematic**

# 2 Pin Description

## 2.1 Pin Assignment

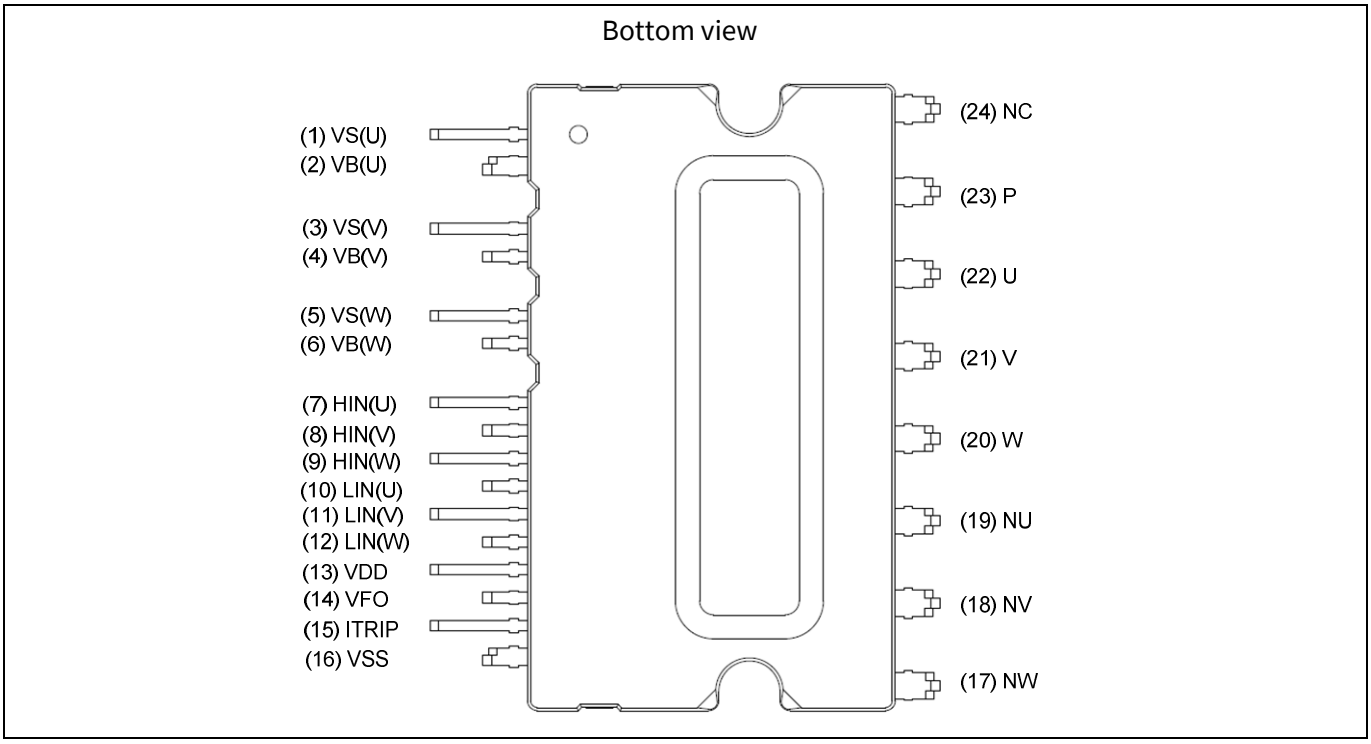



**Figure 2 Pin configuration**

**Table 2 Pin assignment**

| Pin number | Pin name | Pin description |
|---|---|---|
| 1 | $V_S$(U) | U-phase high-side floating IC supply offset voltage |
| 2 | $V_B$(U) | U-phase high-side floating IC supply voltage |
| 3 | $V_S$(V) | V-phase high-side floating IC supply offset voltage |
| 4 | $V_B$(V) | V-phase high-side floating IC supply voltage |
| 5 | $V_S$(W) | W-phase high-side floating IC supply offset voltage |
| 6 | $V_B$(W) | W-phase high-side floating IC supply voltage |
| 7 | HIN(U) | U-phase high-side gate driver input |
| 8 | HIN(V) | V-phase high-side gate driver input |
| 9 | HIN(W) | W-phase high-side gate driver input |
| 10 | LIN(U) | U-phase low-side gate driver input |
| 11 | LIN(V) | V-phase low-side gate driver input |
| 12 | LIN(W) | W-phase low-side gate driver input |
| 13 | $V_{DD}$ | Low-side control supply |
| 14 | $V_{FO}$ | Fault output / temperature monitor |
| 15 | ITRIP | Overcurrent shutdown input |
| 16 | $V_{SS}$ | Low-side control negative supply |
| 17 | NW | W-phase low-side emitter |
| 18 | NV | V-phase low-side emitter |

| | | |
|---|---|---|
| 19 | NU | U-phase low-side emitter |
| 20 | W | Motor W-phase output |
| 21 | V | Motor V-phase output |
| 22 | U | Motor U-phase output |
| 23 | P | Positive bus input voltage |
| 24 | NC | No connection |

## 2.2 Pin Description

**HIN(U, V, W) and LIN(U, V, W) (Low-side and high-side control pins, Pin 7 - 12)**

These pins are positive logic and they are responsible for the control of the integrated IGBTs. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. A pull-down resistor of about 5 kΩ is internally provided to pre-bias inputs during supply start-up, and a zener clamp is provided to protect the pins. Input Schmitt-trigger and noise filter provide noise rejection to short input pulses.

The noise filter suppresses control pulses shoter than the filter time $t_{FIL,IN}$. The Figure 4 describes how the filter works. An input pulse-width shorter than 1 µs is not recommended.

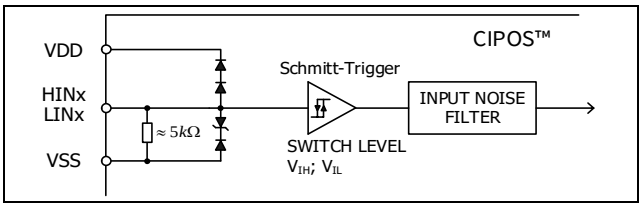



**Figure 3 Input pin structure**

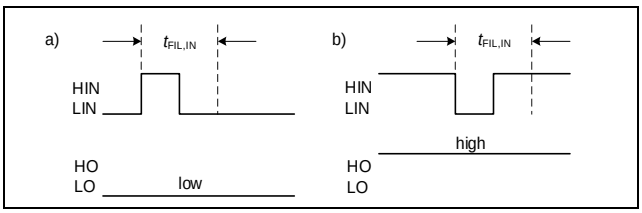



**Figure 4 Input filter timing diagram**

The integrated gate driver additionally provides a shoot-through prevention capability that avoids the simultaneous on-states of the same leg. When both inputs of the same leg are activated, only formerly activated one is remained activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 380 ns is also provided by driver, in order to reduce cross-conduction of the IGBTs.

**$V_{FO}$ (Fault-output and NTC, Pin 14)**

The $V_{FO}$ pin indicates a module failure in case of undervoltage at pin $V_{DD}$ or in case of triggered overcurrent detection at ITRIP. An external pull-up resistor is required.

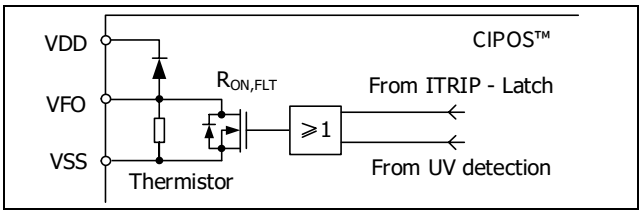



**Figure 5 Internal circuit at pin $V_{FO}$**

The pin 14 provides direct access to the NTC which is referenced to $V_{SS}$. An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

**ITRIP (Overcurrent detection function, Pin 15)**

The CIPOS™ product family provides an overcurrent detection function by connecting the ITRIP input with the IGBT current feedback. The ITRIP comparator threshold (typ. 0.47 V) is referenced to $V_{SS}$. An input noise filter ($t_{ITRIP}$ = typ. 530 ns) prevents the driver to detect false overcurrent events.
Overcurrent detection generates a shutdown of all outputs of the gate driver.
The fault-clear time is set to minimum 40 µs.

**$V_{DD}$, $V_{SS}$ (Low-side control supply and reference, Pin 13, 16)**

$V_{DD}$ is the control supply and it provides power both to input logic and to output stage. Input logic is referenced to $V_{SS}$ ground.

The undervoltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+}$ = 12.1 V is present.
The gate driver shuts down all the outputs, when the $V_{DD}$ supply voltage is below $V_{DDUV-}$ = 10.4 V. This prevents the IGBTs from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

### $V_B$(U, V, W) and $V_S$(U, V, W) (High-side supplies, Pin 1 - 6)

$V_B$ to $V_S$ is the high-side supply voltage. The high-side circuit can float with respect to $V_{SS}$ following the high-side IGBT emitter voltage.
Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.
The undervoltage detection operates with a rising supply threshold of typical $V_{BSUV+}$ = 12.1 V and a falling threshold of $V_{BSUV-}$ = 10.4 V.
$V_S$(U, V, W) provide a high robustness against negative voltage in respect of $V_{SS}$ of -50 V transiently. This ensures very stable designs even under harsh conditions.

### NW, NV, NU (Low-side emitter, Pin 17 - 19)

The low-side emitters are available for current measurement of each phase leg. It is recommended to keep the connection to pin $V_{SS}$ as short as possible to avoid unnecessary inductive voltage drops.

### W, V, U (High-side emitter and low-side collector, Pin 20 - 22)

These pins are connected to motor U, V, W input pins

### P (Positive bus input voltage, Pin 23)

The high-side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

# 3 Absolute Maximum Ratings

($V_{DD}$ = 15 V and $T_J$ = 25°C, if not stated otherwise)

## 3.1 Module Section

| Description | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -40 ~ 125 | °C |
| Operating case temperature | $T_C$ | Refer to Figure 7 | -40 ~ 125 | °C |
| Operating junction temperature | $T_J$ | | -40 ~ 150 | °C |
| Isolation test voltage | $V_{ISO}$ | 1 min, RMS, f = 60 Hz | 2000 | V |

## 3.2 Inverter Section

| Description | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| Max. blocking voltage | $V_{CES}$ | | 600 | V |
| DC link supply voltage of P-N | $V_{PN}$ | Applied between P-N | 450 | V |
| DC link supply voltage (surge) of P-N | $V_{PN(surge)}$ | Applied between P-N | 500 | V |
| Output current[1] | $I_C$ | $T_C$ = 25°C, $T_J$ < 150°C | ±6 | A |
| | | $T_C$ = 100°C, $T_J$ < 150°C | ±4 | |
| Maximum peak collector current | $I_{C(peak)}$ | $T_C$ = 25°C, $T_J$ < 150°C less than 1 ms | ±12 | A |
| Power dissipation per IGBT | $P_{tot}$ | | 23.6 | W |
| Short circuit withstand time | $t_{SC}$ | $V_{DC}$ ≤ 400 V, $T_J$ = 150°C | 5 | µs |

## 3.3 Control Section

| Description | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| High-side offset voltage | $V_S$ | | 600 | V |
| Repetitive peak reverse voltage of bootstrap diode | $V_{RRM}$ | | 600 | V |
| Module supply voltage | $V_{DD}$ | | -1 ~ 20 | V |
| High-side floating supply voltage ($V_B$ reference to $V_S$) | $V_{BS}$ | | -1 ~ 20 | V |
| Input voltage (LIN, HIN, ITRIP) | $V_{IN}$ | | -1 ~ 10 | V |

[1] Pulse width and period are limited by junction temperature

# 4 Thermal Characteristics

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Single IGBT thermal resistance, junction to case | $R_{thJC}$ | See Figure 7 for $T_C$ measurement point | - | - | 5.3 | K/W |

# 5 Recommended Operation Conditions

All voltages are absolute voltages referenced to $V_{SS}$ -potential unless otherwise specified.

| Description | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| DC link supply voltage of P-N | $V_{PN}$ | 0 | - | 400 | V |
| Low-side supply voltage | $V_{DD}$ | 14.0 | 16.0 | 18.5 | V |
| High-side floating supply voltage ($V_B$ vs. $V_S$) | $V_{BS}$ | 13.5 | - | 18.5 | V |
| Logic input voltages LIN, HIN, ITRIP | $V_{IN}$<br>$V_{ITRIP}$ | 0 | - | 5 | V |
| Inverter PWM carrier frequency | $f_{PWM}$ | - | - | 20 | kHz |
| External deadtime between HIN and LIN | DT | 1.0 | - | - | µs |
| Voltage between $V_{SS}$ – N (including surge) | $V_{COMP}$ | -5 | - | 5 | V |
| Minimum input pulse width | $PW_{IN(ON)}$<br>$PW_{IN(OFF)}$ | 1 | - | - | µs |
| Control supply variation | $\Delta V_{BS}$<br>$\Delta V_{DD}$ | -1<br>-1 | -<br>- | 1<br>1 | V/µs |

# 6 Static Parameters

($V_{DD}$ = $V_{BS}$ = 15 V and $T_J$ = 25°C, if not stated otherwise)

## 6.1 Inverter Section

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Collector-emitter voltage | $V_{CE(Sat)}$ | $I_C$ = 4 A, $T_J$ = 25°C<br>$I_C$ = 4 A, $T_J$ = 150°C | -<br>- | 1.6<br>1.8 | 2.0<br>- | V |
| Collector-emitter leakage current | $I_{CES}$ | $V_{CE}$ = 600 V | - | - | 1 | mA |
| Diode forward voltage | $V_F$ | $I_F$ = 4 A, $T_J$ = 25°C<br>$I_F$ = 4 A, $T_J$ = 150°C | -<br>- | 1.75<br>1.8 | 2.2<br>- | V |

## 6.2 Control Section

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Logic "1" input voltage (LIN, HIN) | $V_{IH}$ | | - | 2.1 | 2.5 | V |
| Logic "0" input voltage (LIN, HIN) | $V_{IL}$ | | 0.7 | 0.9 | - | V |
| ITRIP positive going threshold | $V_{IT,TH+}$ | | 400 | 470 | 540 | mV |
| ITRIP input hysteresis | $V_{IT,HYS}$ | | 40 | 70 | - | mV |
| $V_{DD}$ and $V_{BS}$ supply undervoltage positive going threshold | $V_{DDUV+}$ | | 10.8 | 12.1 | 13.0 | V |
| | $V_{BSUV+}$ | | 10.8 | 12.1 | 13.0 | |
| $V_{DD}$ and $V_{BS}$ supply undervoltage negative going threshold | $V_{DDUV-}$ | | 9.5 | 10.4 | 11.2 | V |
| | $V_{BSUV-}$ | | 9.5 | 10.4 | 11.2 | |
| $V_{DD}$ and $V_{BS}$ supply undervoltage lockout hysteresis | $V_{DDUVH}$<br>$V_{BSUVH}$ | | 1.0 | 1.7 | - | V |
| Quiescent $V_{Bx}$ supply current ($V_{Bx}$ only) | $I_{QBS}$ | $H_{IN}$ = 0 V | - | 300 | 500 | µA |
| Quiescent $V_{DD}$ supply current ($V_{DD}$ only) | $I_{QDD}$ | $L_{IN}$ = 0 V, $H_{INX}$ = 5 V | - | 370 | 900 | µA |
| Input bias current for LIN, HIN | $I_{IN+}$ | $V_{IN}$ = 5 V | - | 1.0 | 1.5 | mA |
| | $I_{IN-}$ | $V_{IN}$ = 0 V | - | 2.0 | - | µA |
| Input bias current for ITRIP | $I_{ITRIP+}$ | $V_{ITRIP}$ = 5 V | - | 65 | 150 | µA |
| Input bias current for $V_{FO}$ | $I_{FO}$ | $V_{FO}$ = 5 V, $V_{ITRIP}$ = 0 V | - | 60 | - | µA |
| $V_{FO}$ output voltage | $V_{FO}$ | $I_{FO}$ = 10 mA, $V_{ITRIP}$ = 1 V | - | 0.5 | - | V |
| Bootstrap diode forward voltage | $V_{F\_BSD}$ | $I_F$ = 20 mA | - | 2.6 | - | V |
| Bootstrap diode resistance of U-phase[1] | $R_{BS(U)}$ | $V_{S(V)}$ or $V_{S(W)}$ = 300 V, $T_J$ = 25°C<br>$V_{S(V)}$ and $V_{S(W)}$ = 0 V, $T_J$ = 25°C<br>$V_{S(V)}$ or $V_{S(W)}$ = 300 V, $T_J$ = 125°C<br>$V_{S(V)}$ and $V_{S(W)}$ = 0 V, $T_J$ = 125°C | - | 35<br>40<br>50<br>65 | - | Ω |

[1] $R_{BS(V)}$ and $R_{BS(W)}$ have same values to $R_{BS(U)}$

# 7 Dynamic Parameters

($V_{DD}$ = 15 V and $T_J$ = 25°C, if not stated otherwise)

## 7.1 Inverter Section

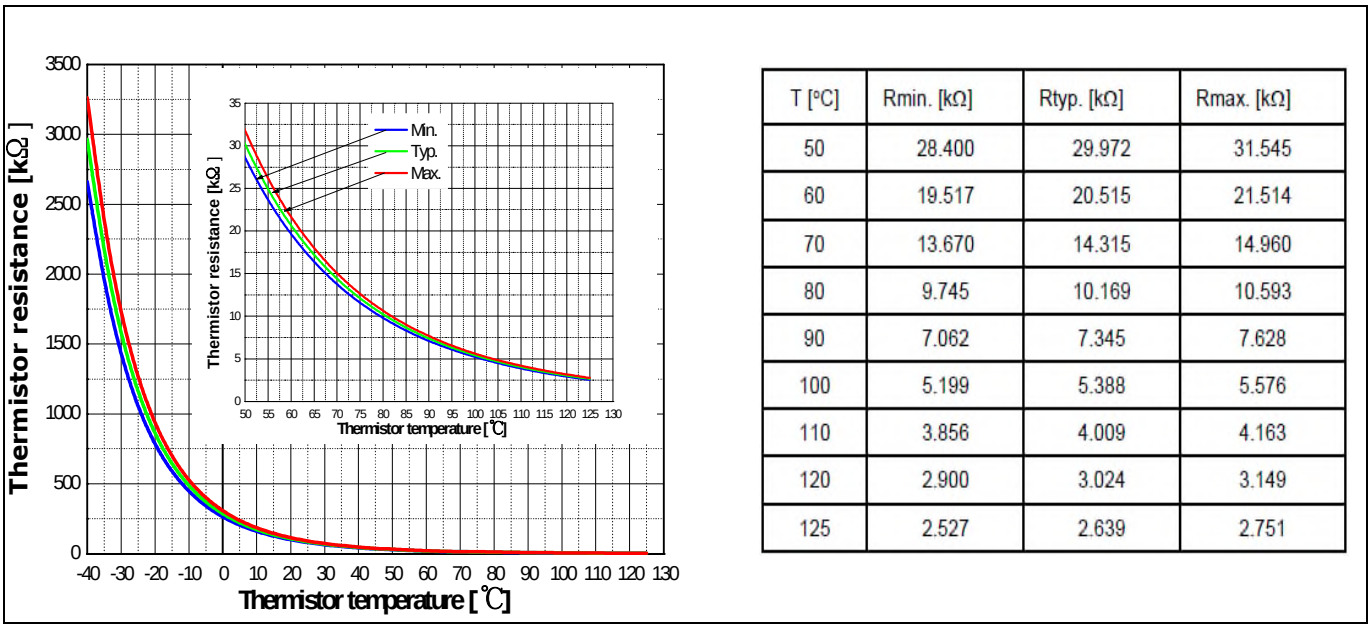
| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Turn-on propagation delay time | $t_{on}$ | $V_{LIN, HIN}$ = 5 V, $I_C$ = 4 A, $V_{DC}$ = 300 V | - | 650 | - | ns |
| Turn-on rise time | $t_r$ | | - | 20 | - | ns |
| Turn-on switching time | $t_{c(on)}$ | | - | 100 | - | ns |
| Reverse recovery time | $t_{rr}$ | | - | 130 | - | ns |
| Turn-off propagation delay time | $t_{off}$ | $V_{LIN, HIN}$ = 0 V, $I_C$ = 4 A, $V_{DC}$ = 300 V | - | 680 | - | ns |
| Turn-off fall time | $t_f$ | | - | 180 | - | ns |
| Turn-off switching time | $t_{c(off)}$ | | - | 220 | - | ns |
| Short circuit propagation delay time | $t_{SCP}$ | From $V_{IT,TH+}$ to 10% $I_{SC}$ | - | 1420 | - | ns |
| IGBT turn-on energy (includes reverse recovery of diode) | $E_{on}$ | $V_{DC}$ = 300 V, $I_C$ = 4 A<br>$T_J$ = 25°C<br>$T_J$ = 150°C | <br>-<br>- | <br>75<br>130 | <br>-<br>- | µJ |
| IGBT turn-off energy | $E_{off}$ | $V_{DC}$ = 300 V, $I_C$ = 4 A<br>$T_J$ = 25°C<br>$T_J$ = 150°C | <br>-<br>- | <br>120<br>190 | <br>-<br>- | µJ |
| Diode recovery energy | $E_{rec}$ | $V_{DC}$ = 300 V, $I_C$ = 4 A<br>$T_J$ = 25°C<br>$T_J$ = 150°C | <br>-<br>- | <br>40<br>70 | <br>-<br>- | µJ |

## 7.2 Control Section

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Input filter time ITRIP | $t_{ITRIP}$ | $V_{ITRIP}$ = 1 V | - | 530 | - | ns |
| Input filter time at LIN, HIN for turn on and off | $t_{FIL,IN}$ | $V_{LIN, HIN}$ = 0 V or 5 V | - | 290 | - | ns |
| Fault clear time after ITRIP-fault | $t_{FLTCLR}$ | | 40 | 65 | 200 | µs |
| ITRIP to fault propagation delay | $t_{FLT}$ | $V_{LIN, HIN}$ = 0 or $V_{LIN, HIN}$ = 5 V, $V_{ITRIP}$ = 1 V | - | 680 | 1000 | ns |
| Internal deadtime | $DT_{IC}$ | | - | 380 | - | ns |
| Bootstrap diode reverse recovery time | $t_{rr\_BS}$ | $I_F$ = 0.6 A, di/dt = 80 A/µs | - | 50 | - | ns |

# 8 Thermistor

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Resistance | $R_{NTC}$ | $T_{NTC}$ = 25°C | - | 85 | - | kΩ |
| B-constant of NTC (negative temperature coefficient) thermistor | B(25/100) | | - | 4092 | - | K |




| T [°C] | Rmin. [kΩ] | Rtyp. [kΩ] | Rmax. [kΩ] |
|---|---|---|---|
| 50 | 28.400 | 29.972 | 31.545 |
| 60 | 19.517 | 20.515 | 21.514 |
| 70 | 13.670 | 14.315 | 14.960 |
| 80 | 9.745 | 10.169 | 10.593 |
| 90 | 7.062 | 7.345 | 7.628 |
| 100 | 5.199 | 5.388 | 5.576 |
| 110 | 3.856 | 4.009 | 4.163 |
| 120 | 2.900 | 3.024 | 3.149 |
| 125 | 2.527 | 2.639 | 2.751 |

**Figure 6 Thermistor resistance – temperature curve and table**
**(For more information, please refer to the application note)**

# 9 Mechanical Characteristics and Ratings

| Description | Condition | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Comparative tracking index (CTI) | | 550 | - | - | V |
| Mounting torque | M3 screw and washer | 0.59 | 0.69 | 0.78 | Nm |
| Backside curvature | Refer to Figure 8 | -50 | - | 100 | µm |
| Weight | | - | 6.15 | - | g |

# 10 Qualification Information

| | | |
|---|---|---|
| **UL certification** | File number: E314539 | |
| **Moisture sensitivity level (SOP23 only)** | - | |
| **RoHS compliant** | Yes (Lead-free terminal plating) | |
| **ESD** | HBM(human body model) class | 2 |
| | CDM(charged device model) class | C3 |

# 11 Diagrams and Tables

## 11.1 $T_C$ Measurement Point

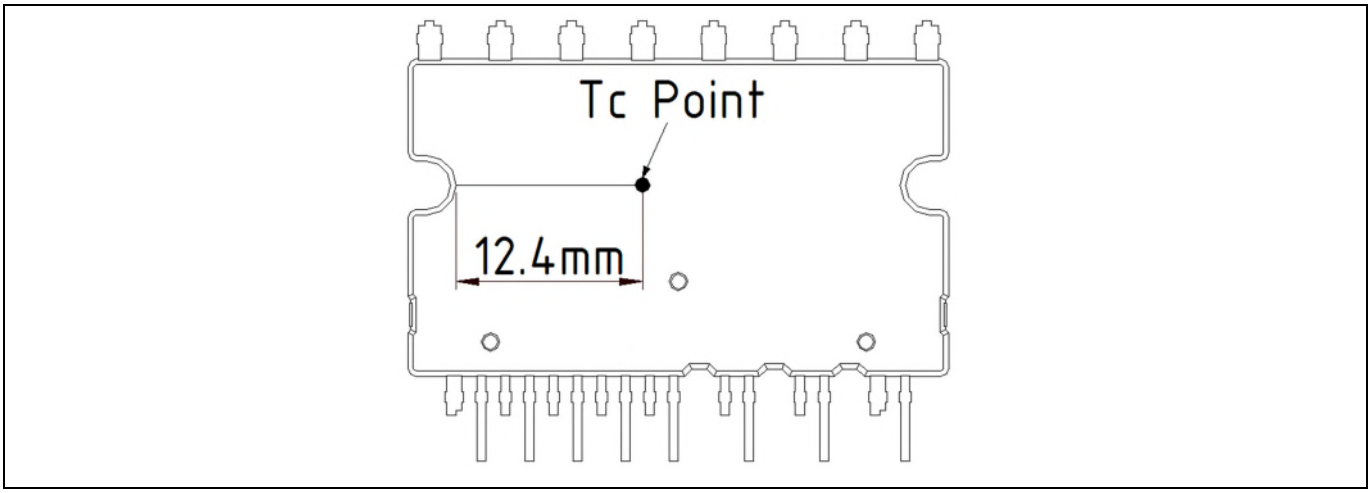



**Figure 7 $T_C$ measurement point[1]**

## 11.2 Backside Curvature Measurment Point

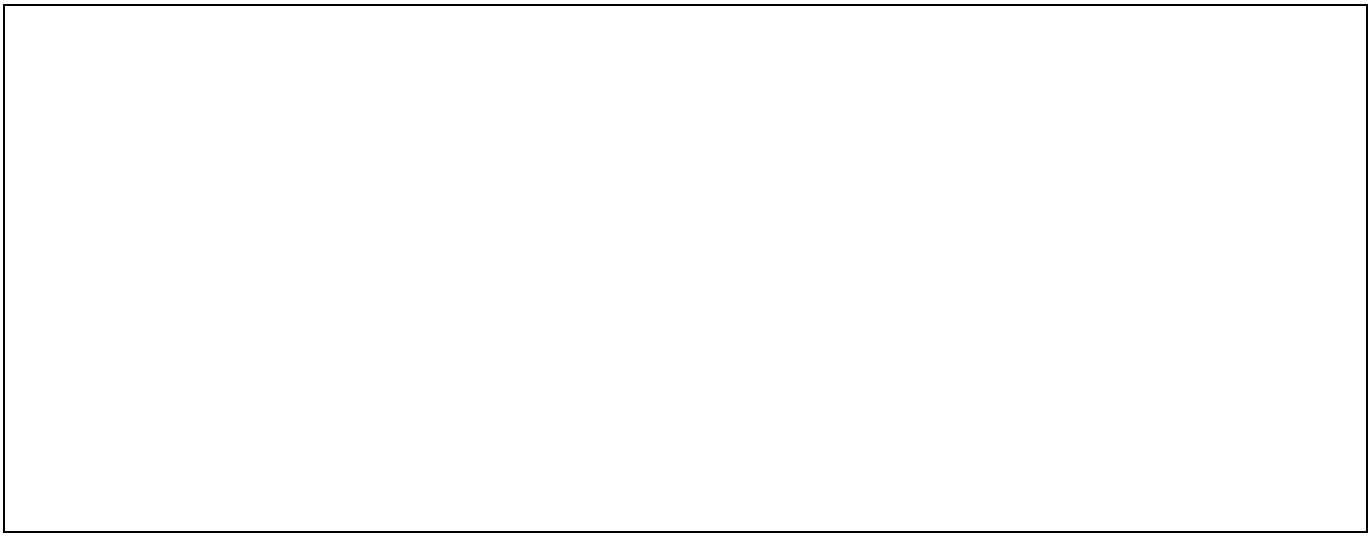


**Figure 8 Backside curvature measurement position**

[1]Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

## 11.3 Switching Time Definition

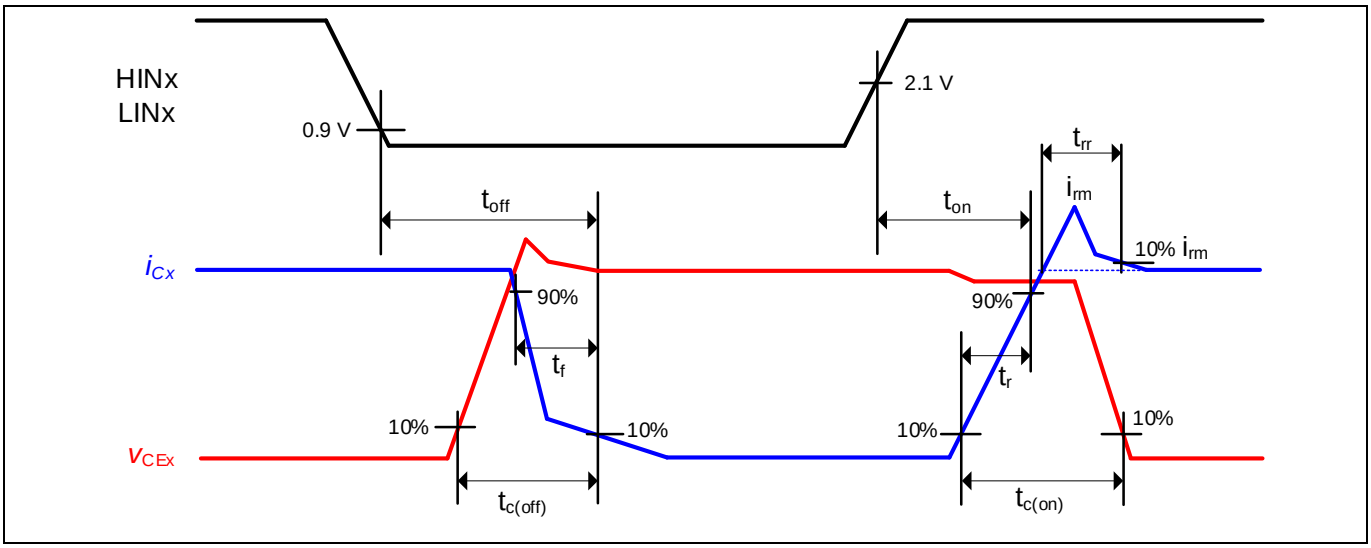



**Figure 9 Switching time definition**

# 12 Application Guide

## 12.1 Typical Application Schematic

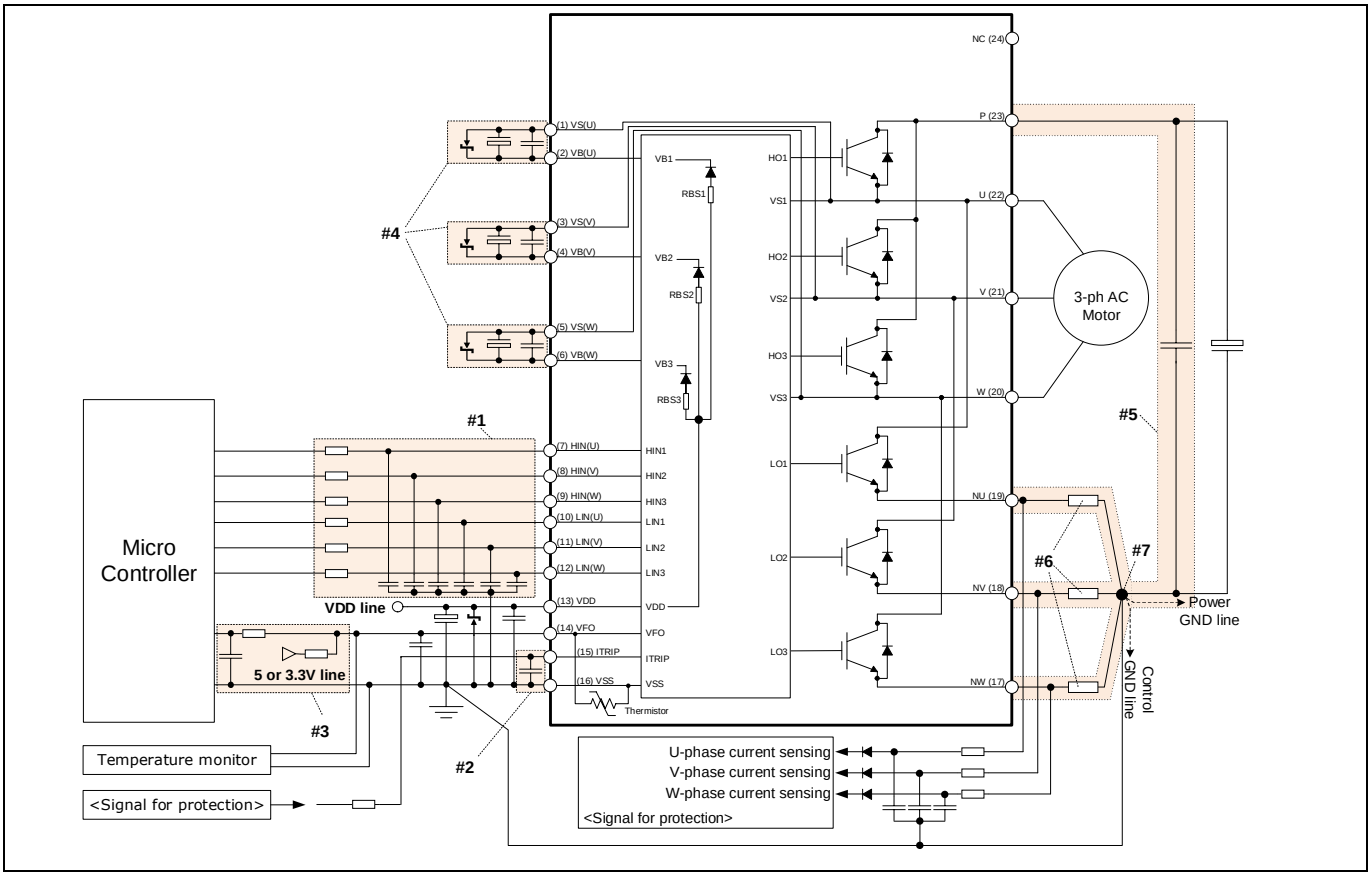



**Figure 10 Typical application circuit**

- #1 Input circuit
  - RC filter circuit can be used to reduce input signal noise (e.g. 100 Ω, 1 nF).
  - The filter capacitors should be placed close to the IPM (to $V_{SS}$ pin especially).
- #2 ITRIP circuit
  - To prevent protection function errors, RC filter circuit is recommended.
  - The filter capacitor should be placed close to ITRIP and $V_{SS}$ pins.
- #3 $V_{FO}$ circuit
  - $V_{FO}$ pin is an open-drain output. This signal line should be pulled up to the bias voltage of the 5 V/3.3 V with a proper resistor.
  - It is recommended that RC filter circuit is placed close to the controller.
- #4 $V_B$-$V_S$ circuit
  - Capacitors for high-side floating supply voltage should be placed close to $V_B$ and $V_S$ pins.
- #5 Snubber capacitor
  - The wiring among the IPM, snubber capacitor and shunt resistors should be short as possible.
- #6 Shunt resistor
  - SMD-type resistors are strongly recommended to minimize stray inductance.
- #7 Ground pattern
  - Power ground and signal ground should be connected at a single point. It is recommended to connect them at the end of shunt resistor.

## 12.2 Performance Chart

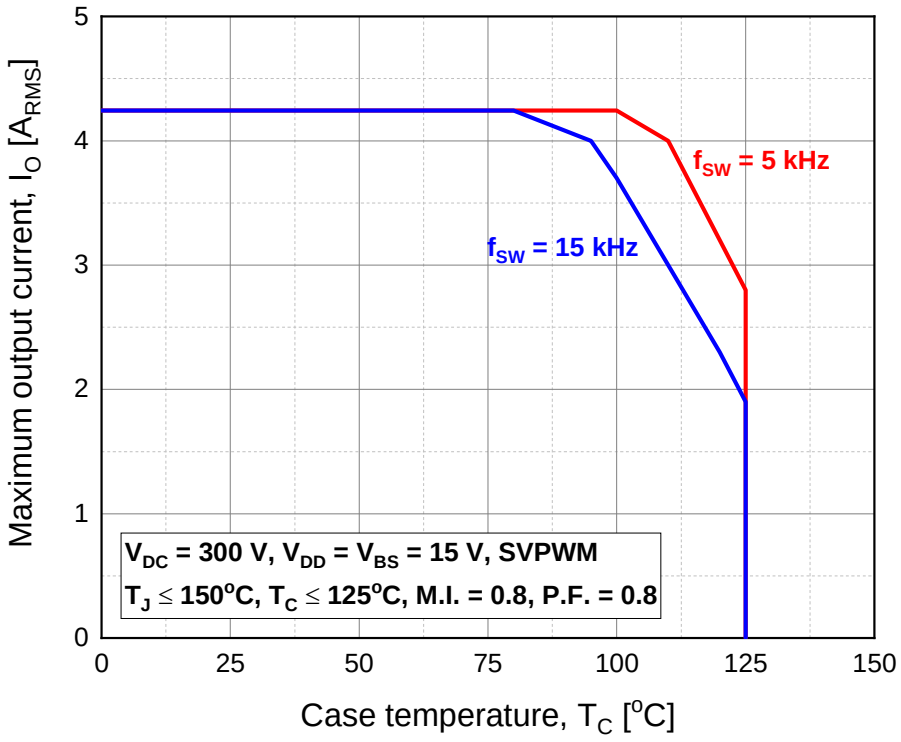



**Figure 11 Maximum operating current SOA[1]**

[1]This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

# 13 Package Outline

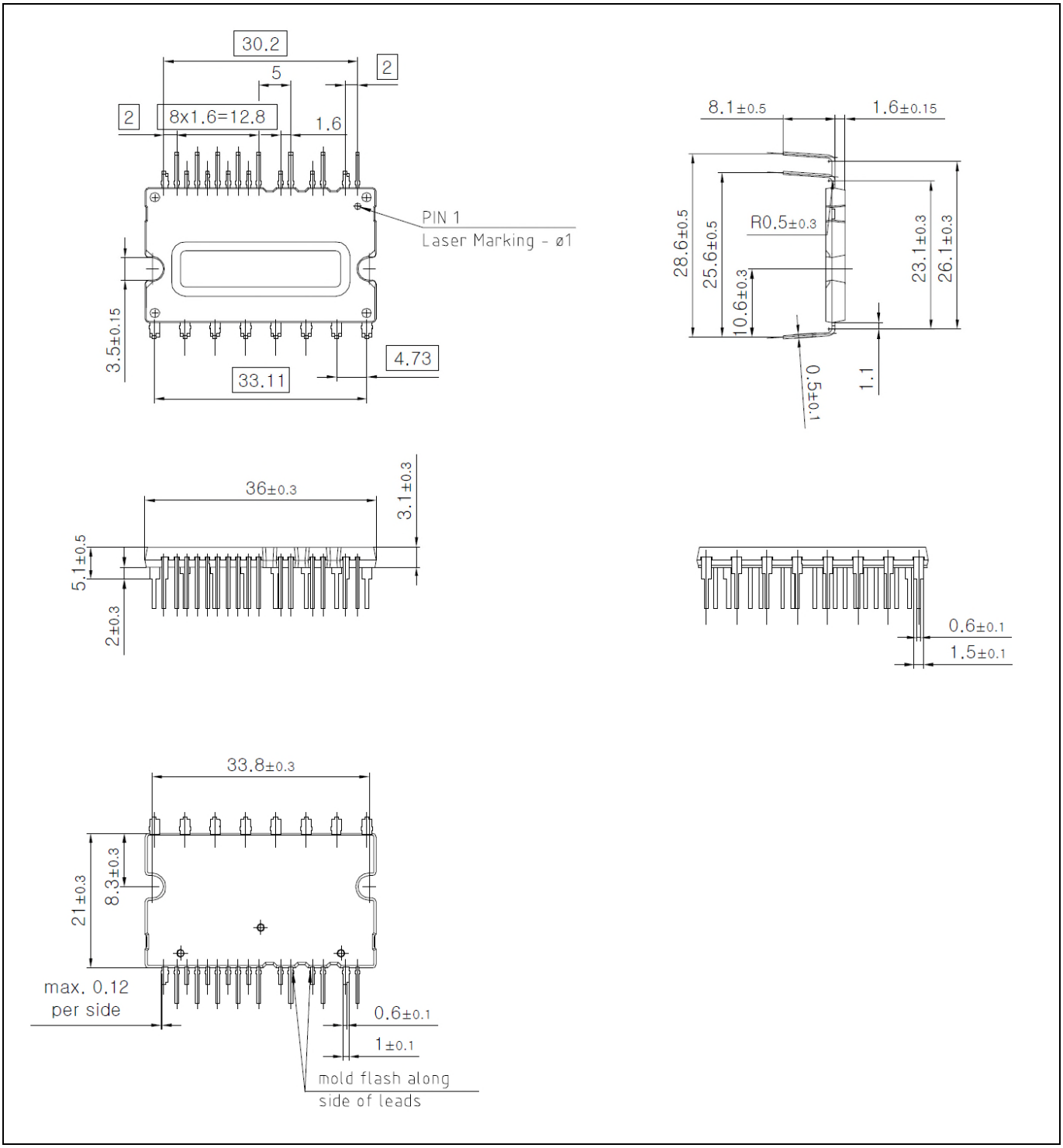



**Figure 12 IGCM06F60GA**

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| 2.8 | Sep. 2017 | Maximum operating case temperature, $T_C$ = 125°C<br>Package outline update |
| 3.0 | Jan. 2023 | Updated Figure 11 |
| 3.1 | Jun. 2023 | Corrected error in $I_{IN-}$ |

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