Description

The 5P8390x is a high performance, 1-to-4/6/8 crystal input to LVCMOS fanout buffer with output enable pins. This device accepts a fundamental mode crystal from 10MHz to 40MHz and outputs LVCMOS clocks with best-in-class phase noise performance.

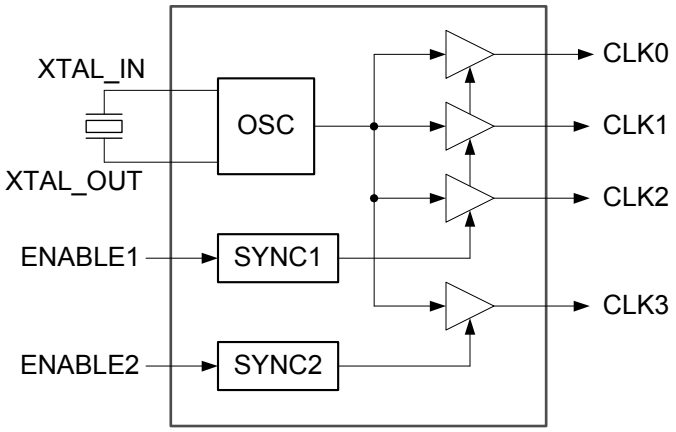
The 5P8390x family (5P83904, 5P83905, and 5P83908) features a synchronous glitch-free Output Enable function to eliminate any intermediate incorrect output clock cycles when enabling or disabling outputs. It comes in standard TSSOP packages or small QFN packages and can operate from 1.8V to 3.3V supplies.

Features

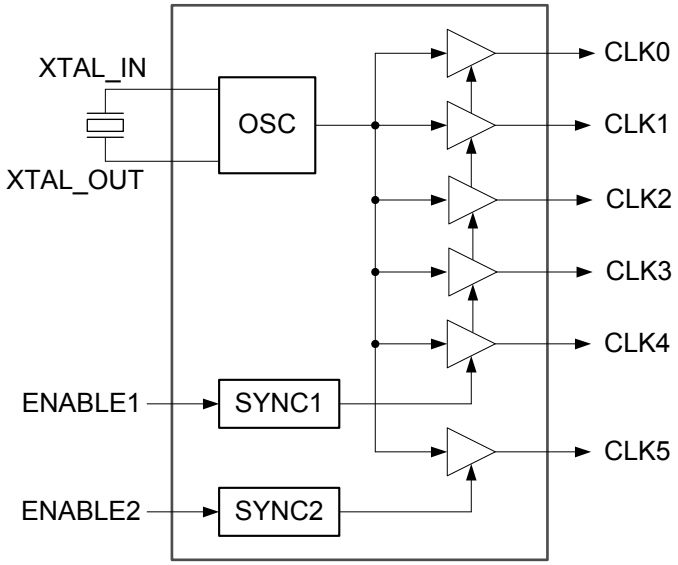
- 4/6/8 copies of LVCMOS output clocks with best-in-class phase noise performance
- Phase Noise:

  Offset Noise Power (3.3V)
  - 100Hz: -131 dBc/Hz
  - 1KHz: -145 dBc/Hz
  - 10KHz: -154 dBc/Hz
  - 100KHz: -161 dBc/Hz
- Operating power supply modes:
  - Full 3.3V, 2.5V, 1.8V
  - Mixed 3.3V core/2.5V output operating supply
  - Mixed 3.3V core/1.8V output operating supply
  - Mixed 2.5V core/1.8V output operating supply
- Crystal Oscillator Interface
- Synchronous Output Enable
- Packaged in 16-, 20-pin TSSOP and QFN packages (Pb free, fully RoHS compliant)
- Extended (-40°C to +105°C) temperature range

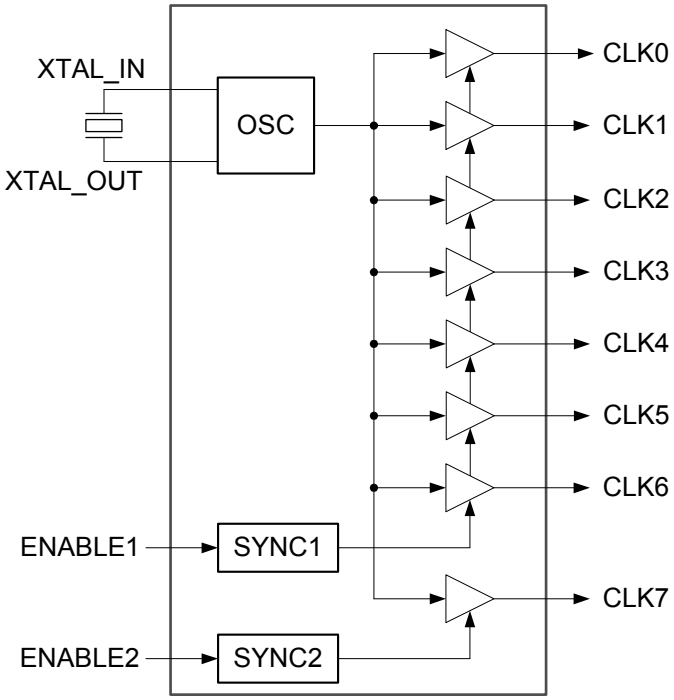
5P83904 Block Diagram



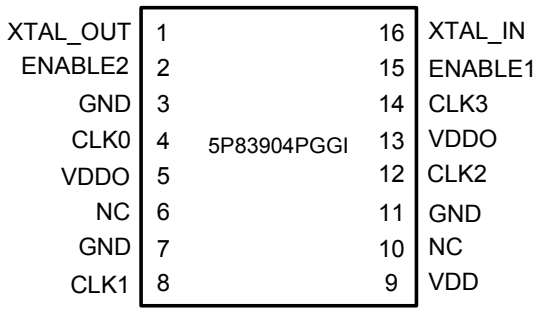
5P83905 Block Diagram

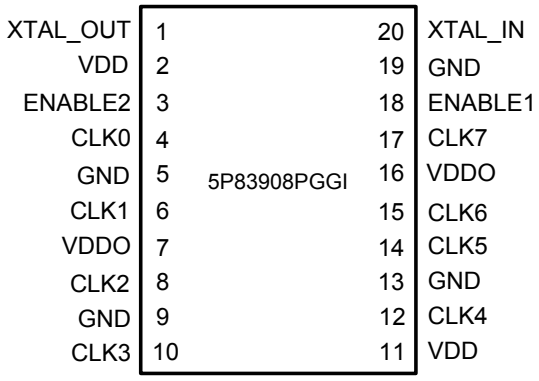


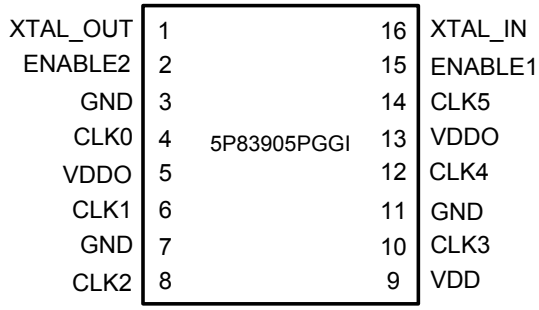
5P83908 Block Diagram



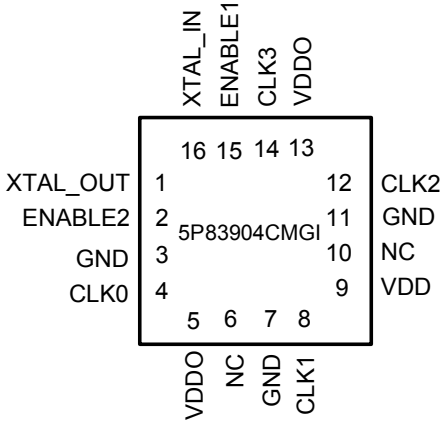
Pin Assignments for TSSOP Packages

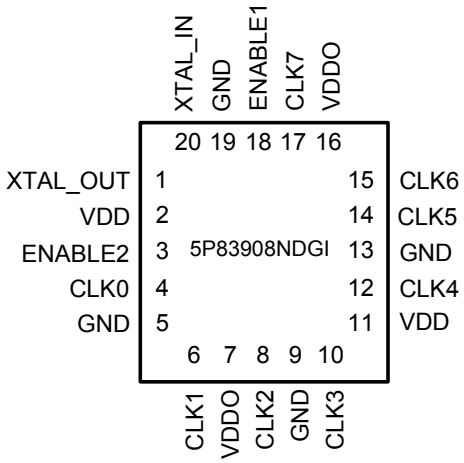


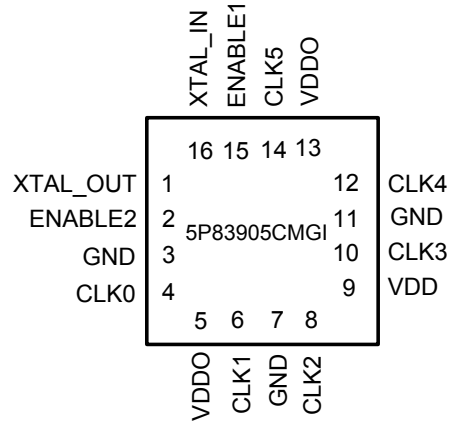




Pin Assignments for QFN Packages







Pin Descriptions

Pin Name	Pin Number			Pin Type	Pin Description
	5P83904	5P83905	5P83908		
XTAL_IN	16	16	20	Input	Oscillator Input from Crystal.
XTAL_OUT	1	1	1	Input	Oscillator Output to drive Crystal.
VDD	9	9	2, 11	Power	Positive power supply for core.
VDDO	5, 13	5, 13	7, 16	Power	Positive power supply for outputs.
GND	3, 7, 11	3, 7, 11	5, 9, 13, 19	Power	Power supply ground.
ENABLE1	15	15	18	Input	Output Enable pin. Please see below Output Enable Function Table. Active High. Internal pull-up.
ENABLE2	2	2	3	Input	Output Enable pin. Please see below Output Enable Function Table. Active High. Internal pull-up.
CLK0	4	4	4	Output	LVCMOS Clock Output 0. Voltage set by VDDO.
CLK1	8	6	6	Output	LVCMOS Clock Output 1. Voltage set by VDDO.
CLK2	12	8	8	Output	LVCMOS Clock Output 2. Voltage set by VDDO.
CLK3	14	10	10	Output	LVCMOS Clock Output 3. Voltage set by VDDO.
CLK4	—	12	12	Output	LVCMOS Clock Output 4. Voltage set by VDDO.
CLK5	—	14	14	Output	LVCMOS Clock Output 5. Voltage set by VDDO.
CLK6	—	—	15	Output	LVCMOS Clock Output 6. Voltage set by VDDO.
CLK7	—	—	17	Output	LVCMOS Clock Output 7. Voltage set by VDDO.
NC	6, 10	—	—	NC	No connect.

Output Enable Function Table

ENABLE1	ENABLE2	5P83904 CLK0-2	5P83905 CLK0-4	5P83908 CLK0-6	5P83904 CLK3	5P83905 CLK5	5P83908 CLK7
0	0	Low	Low	Low	Low	Low	Low
0	1	Low	Low	Low	Active	Active	Active
1	0	Active	Active	Active	Low	Low	Low
1(default)	1(default)	Active	Active	Active	Active	Active	Active

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5P8390x. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Output Enable and All Outputs	-0.4 V to VDD+0.5 V
CLKIN	-0.4 V to 3.465V
Ambient Operating Temperature (extended)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	XTAL_IN, ENABLE1/2 pins	0.7xVDD			V
Input Low Voltage	V_{IL}	XTAL_IN, ENABLE1/2 pins			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	1.65		1.85	V
Output Low Voltage	V_{OL}	I_{OL} = 4 mA	0.03		0.05	V
Nominal Output Impedance	Z_O			14		Ω
Operating Supply Current						
5P83904	IDD	Outputs On, 25MHz with No Load		8.9		mA
5P83905		Outputs On, 25MHz with No Load		9.0		
5P83908		Outputs On, 25MHz with No Load		9.2		

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	XTAL_IN, ENABLE1/2 pins	0.7xVDD			V
Input Low Voltage	V_{IL}	XTAL_IN, ENABLE1/2 pins			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.31		2.58	V
Output Low Voltage	V_{OL}	I_{OL} = 4 mA	0.03		0.05	V
Nominal Output Impedance	Z_O			14		Ω
Operating Supply Current						
5P83904	IDD	Outputs On, 25MHz with No Load		10.6		mA
5P83905		Outputs On, 25MHz with No Load		10.7		
5P83908		Outputs On, 25MHz with No Load		10.8		

VDD=3.3 V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage, CLKIN	V_{IH}	XTAL_IN, ENABLE1/2 pins	0.7xVDD			V
Input Low Voltage, CLKIN	V_{IL}	XTAL_IN, ENABLE1/2 pins			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	3.09		3.43	V
Output Low Voltage	V_{OL}	I_{OL} = 4 mA	0.03		0.04	V
Nominal Output Impedance	Z_O			14		Ω
Operating Supply Current						
5P83904	IDD	Outputs On, 25MHz with No Load		12.1		mA
5P83905		Outputs On, 25MHz with No Load		12.2		
5P83908		Outputs On, 25MHz with No Load		12.3		

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{MAX}	Input Frequency Crystal	8		40	MHz
		Input Frequency Clock	DC		200	
Delay for Output Enable / Disable Time ENABLEx to BCLKn	t_{EN} / t_{DIS}				3	cycles
Duty Cycle	t_{DC}		45		55	ns
Output to Output Skew	$t_{SKEWO-O}$			25	65	ps
Phase Noise	Φnoise	f_{OUT} = 25 MHz 100 Hz off Carrier		-121.1974		dBc/Hz
		f_{OUT} = 25 MHz 1 kHz off Carrier		-132.1742		
		f_{OUT} = 25 MHz 10 kHz off Carrier		-143.8058		
		f_{OUT} = 25 MHz 100 kHz off Carrier		-155.2978		
RMS Phase Jitter	t_{JIT}(Φ)	25MHz carrier, Integration Range: 12kHz-20MHz		0.279		ps
Output Rise/Fall Time	t_R / t_F	20% to 80%			0.95	ns
Device to Device Skew					200	ps
Propagation Delay		freq, LVCMOS INPUT	2.5	3.1	6	ns

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

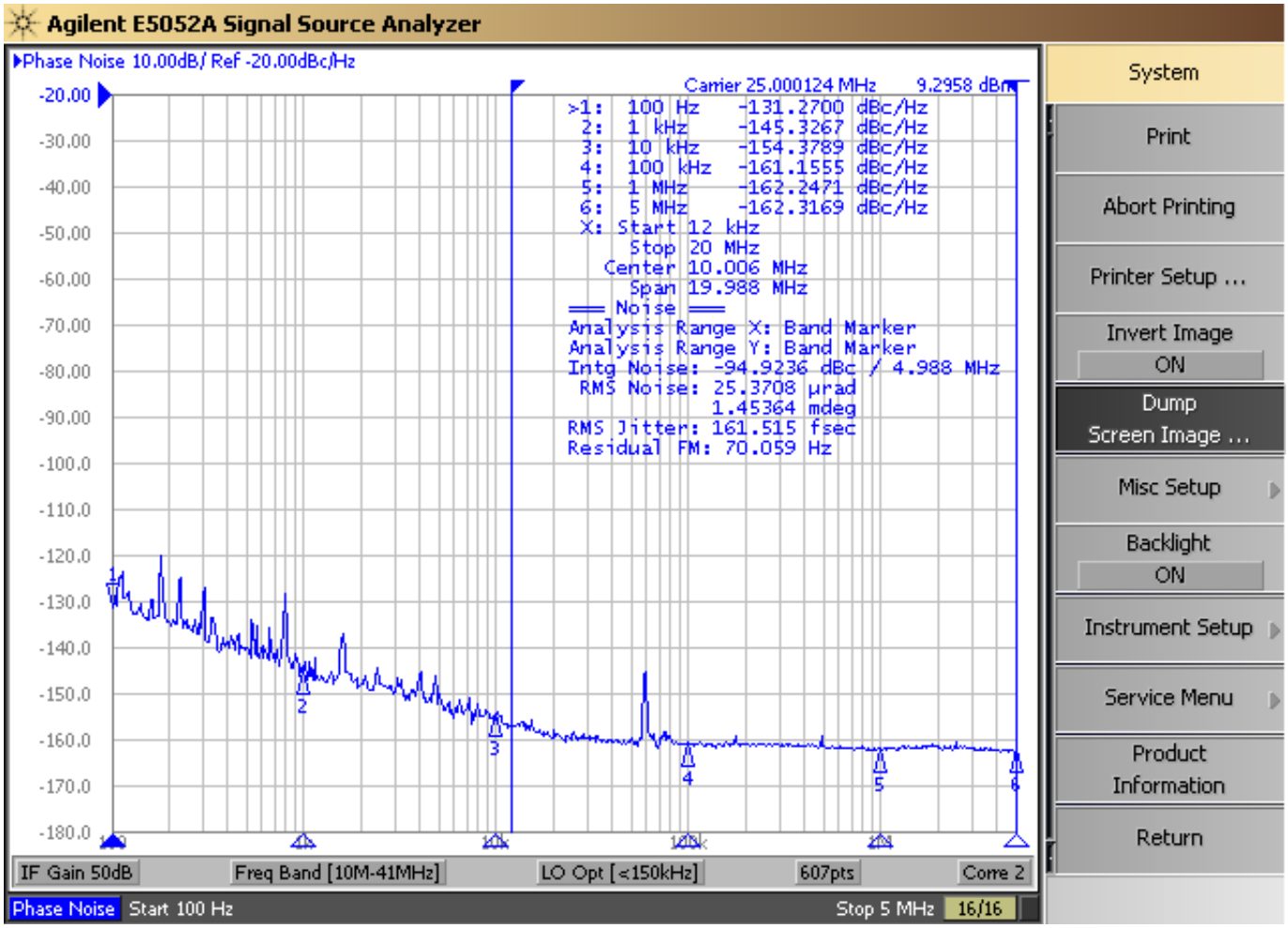
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{MAX}	Input Frequency Crystal	8		40	MHz
		Input Frequency Clock	DC		200	
Delay for Output Enable / Disable Time ENABLEx to BCLKn	t_{EN} / t_{DIS}				3	cycles
Duty Cycle	t_{DC}		45		55	ns
Output to Output Skew	$t_{SKEWO-O}$			25	65	ps
Phase Noise	Φnoise	f_{OUT} = 25 MHz 100 Hz off Carrier		-131.26		dBc/Hz
		f_{OUT} = 25 MHz 1 kHz off Carrier		-139.2177		
		f_{OUT} = 25 MHz 10 kHz off Carrier		-149.5185		
		f_{OUT} = 25 MHz 100 kHz off Carrier		-158.7531		
RMS Phase Jitter	t_{JIT}(Φ)	25MHz carrier, Integration Range: 12kHz-20MHz		0.2		ps
Output Rise/Fall Time	t_R / t_F	20% to 80%			0.9	ns
Device to Device Skew					200	ps
Propagation Delay		freq, LVCMOS INPUT	2.5	3.6	6	ns

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{MAX}	Input Frequency Crystal	8		40	MHz
		Input Frequency Clock	DC		200	
Delay for Output Enable / Disable Time ENABLEx to BCLKn	t_{EN} / t_{DIS}				3	cycles
Duty Cycle	t_{DC}		45		55	ns
Output to Output Skew	$t_{SKEWO-O}$			25	65	ps

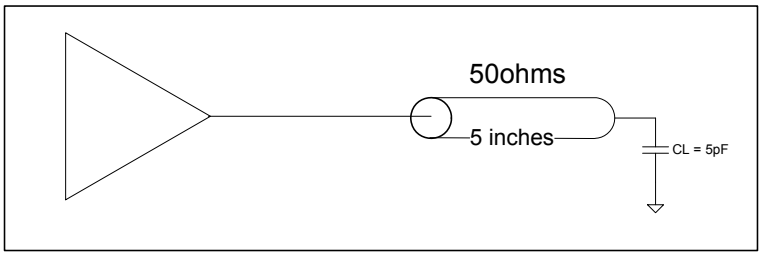
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Phase Noise	Φnoise	f_{OUT} = 25 MHz 100 Hz off Carrier		-131.27		dBc/Hz
		f_{OUT} = 25 MHz 1 kHz off Carrier		-145.3267		
		f_{OUT} = 25 MHz 10 kHz off Carrier		-154.3789		
		f_{OUT} = 25 MHz 100 kHz off Carrier		-161.1555		
RMS Phase Jitter	$t_{JIT}(\Phi)$	25MHz carrier, Integration Range: 12kHz-20MHz		0.16		ps
Output Rise/Fall Time	t_R / t_F	20% to 80%			0.85	ns
Device to Device Skew					200	ps
Propagation Delay		freq, LVCMOS INPUT	2.5	2.9	6	ns

Phase Noise Plots

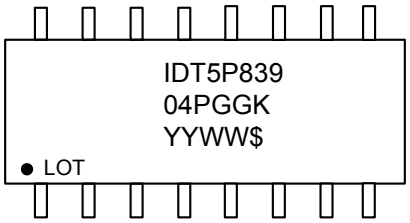


The phase noise plots above show the low Additive Jitter of the 5P8390x high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 58.9fs of RMS phase jitter while the output of 5P8390x has about 70.9fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 39fs.

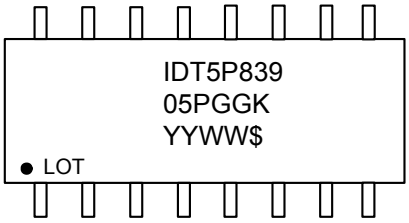
Test Load and Circuit



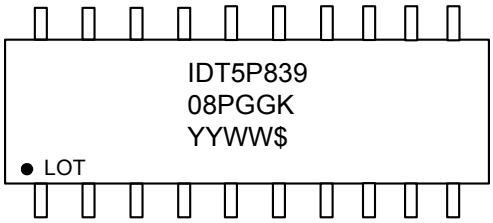
Marking Diagrams



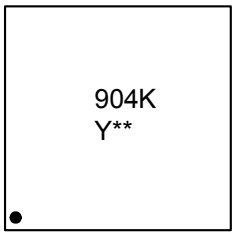
16-pin TSSOP



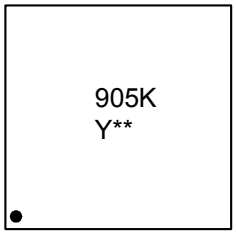
16-pin TSSOP



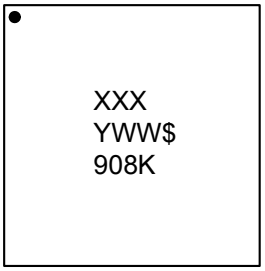
20-pin TSSOP



16-pin QFN



16-pin QFN

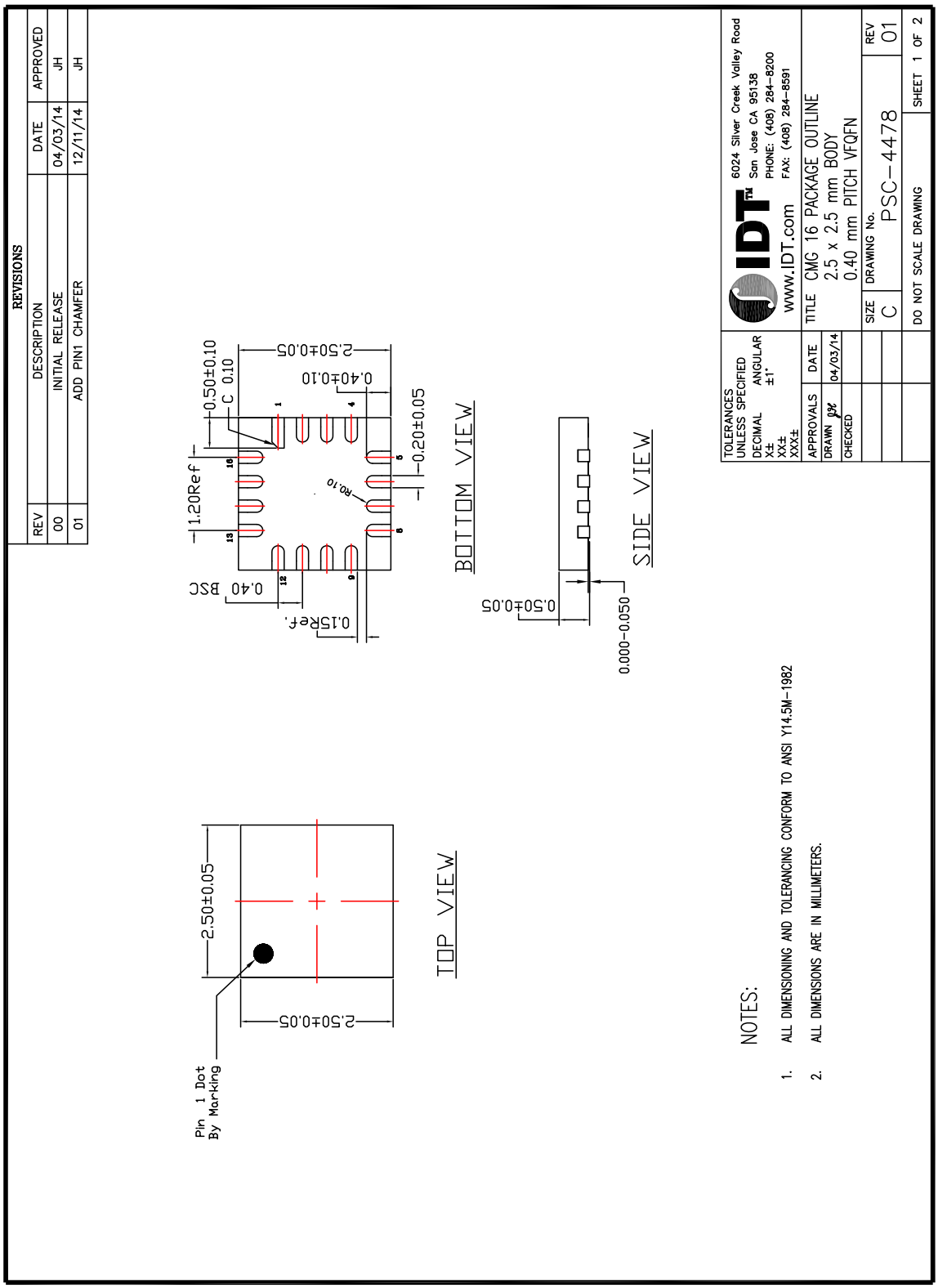


20-pin QFN

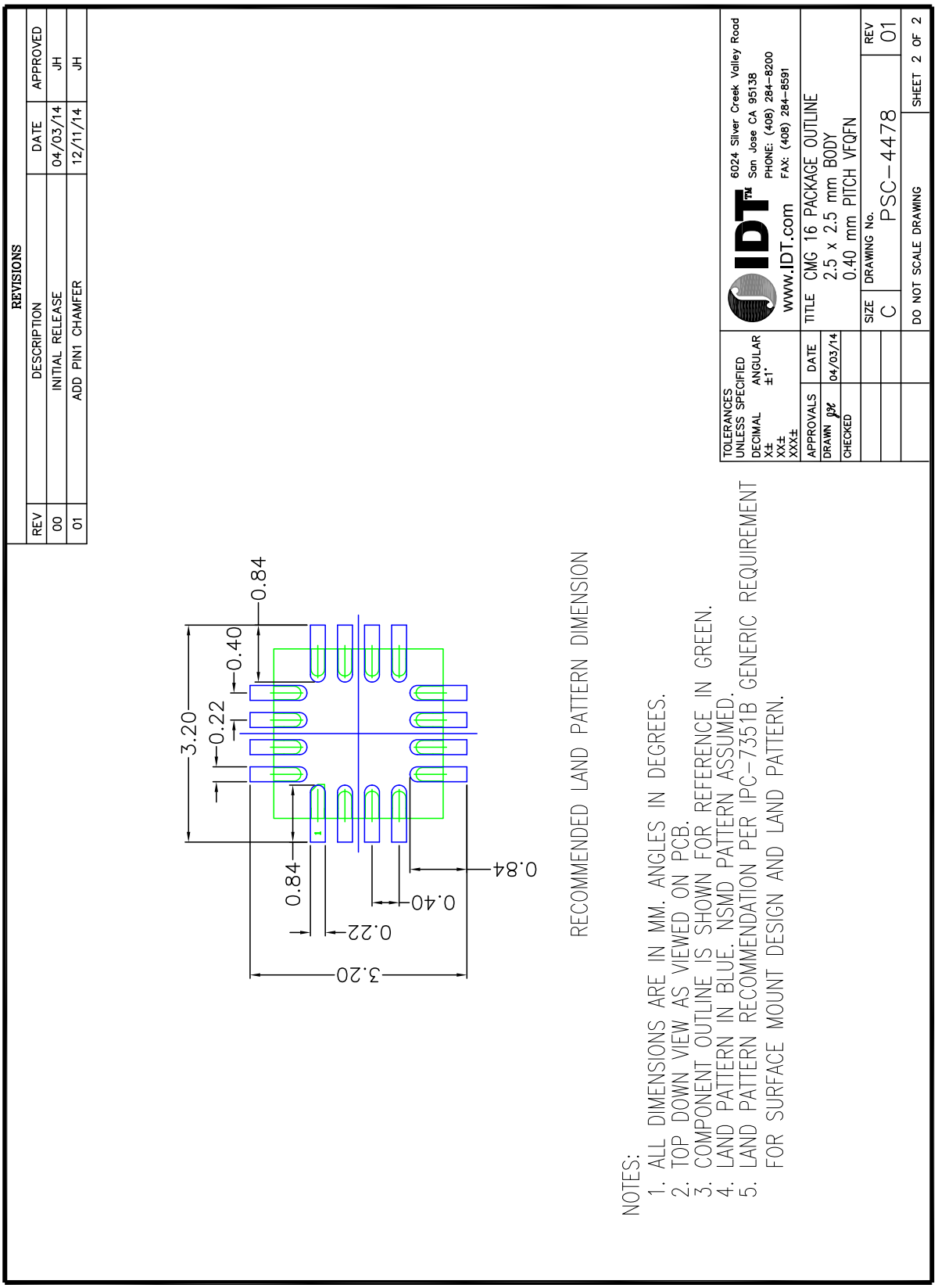
Notes:

1. "**" is the lot sequence.
2. "XXX" denotes the last three characters of the Asm lot (20-pin QFN only).
3. "YYWW", "YWW", "YW", or "Y" is the last digit(s) of the year and week that the part was assembled.
4. "$" denotes the mark code.
5. "LOT" denotes lot number.
6. "G" after the two-letter package code denotes RoHS compliant package.
7. "I" denotes extended temperature range device.
8. Bottom marking: country of origin (TSSOP only).

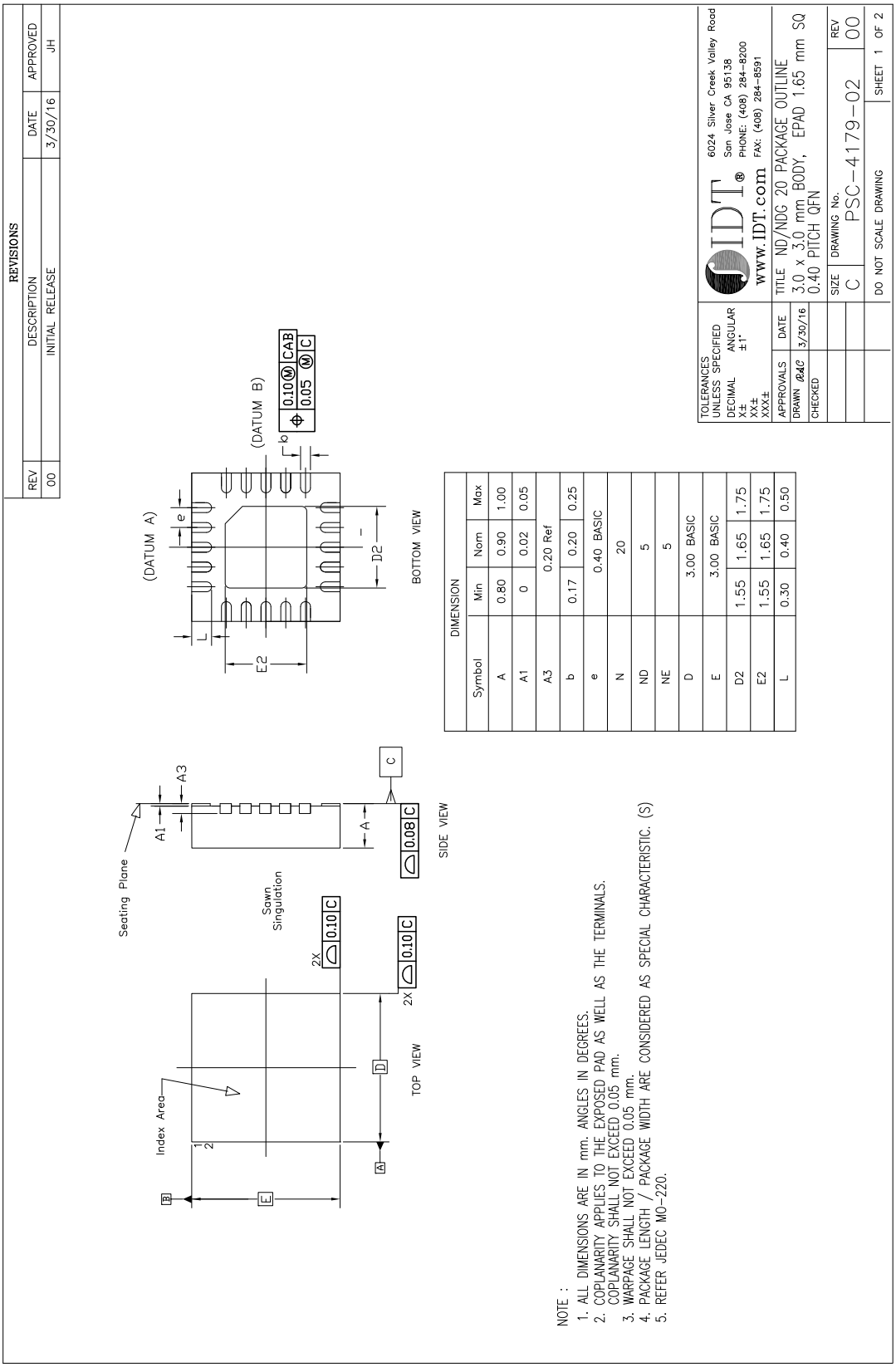
Package Outline and Package Dimensions (16-pin QFN, 2.5mm x 2.5mm Body, 0.4mm pitch)



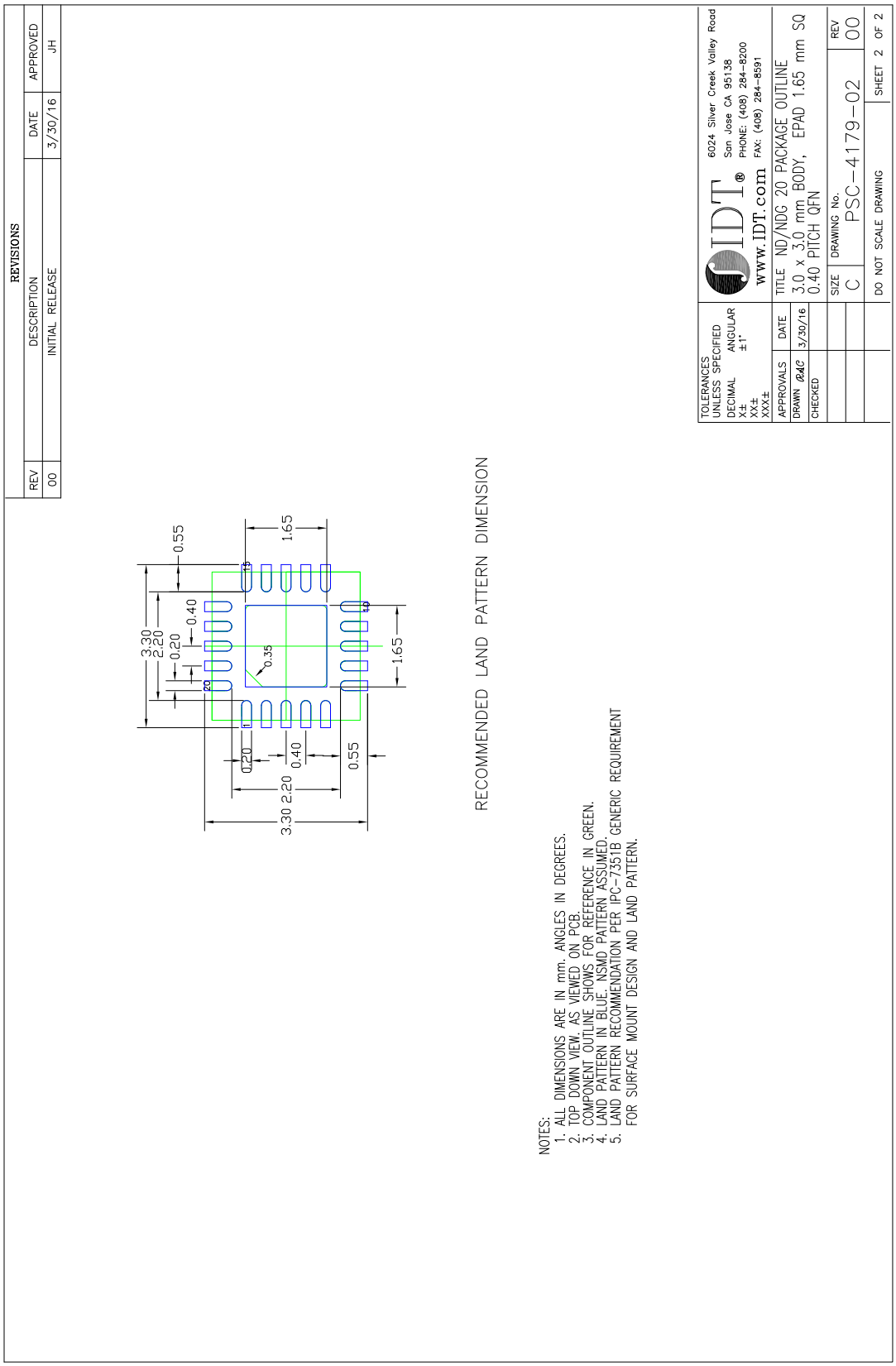
Package Outline and Package Dimensions, cont. (16-pin QFN, 2.5mm x 2.5mm Body, 0.4mm pitch)



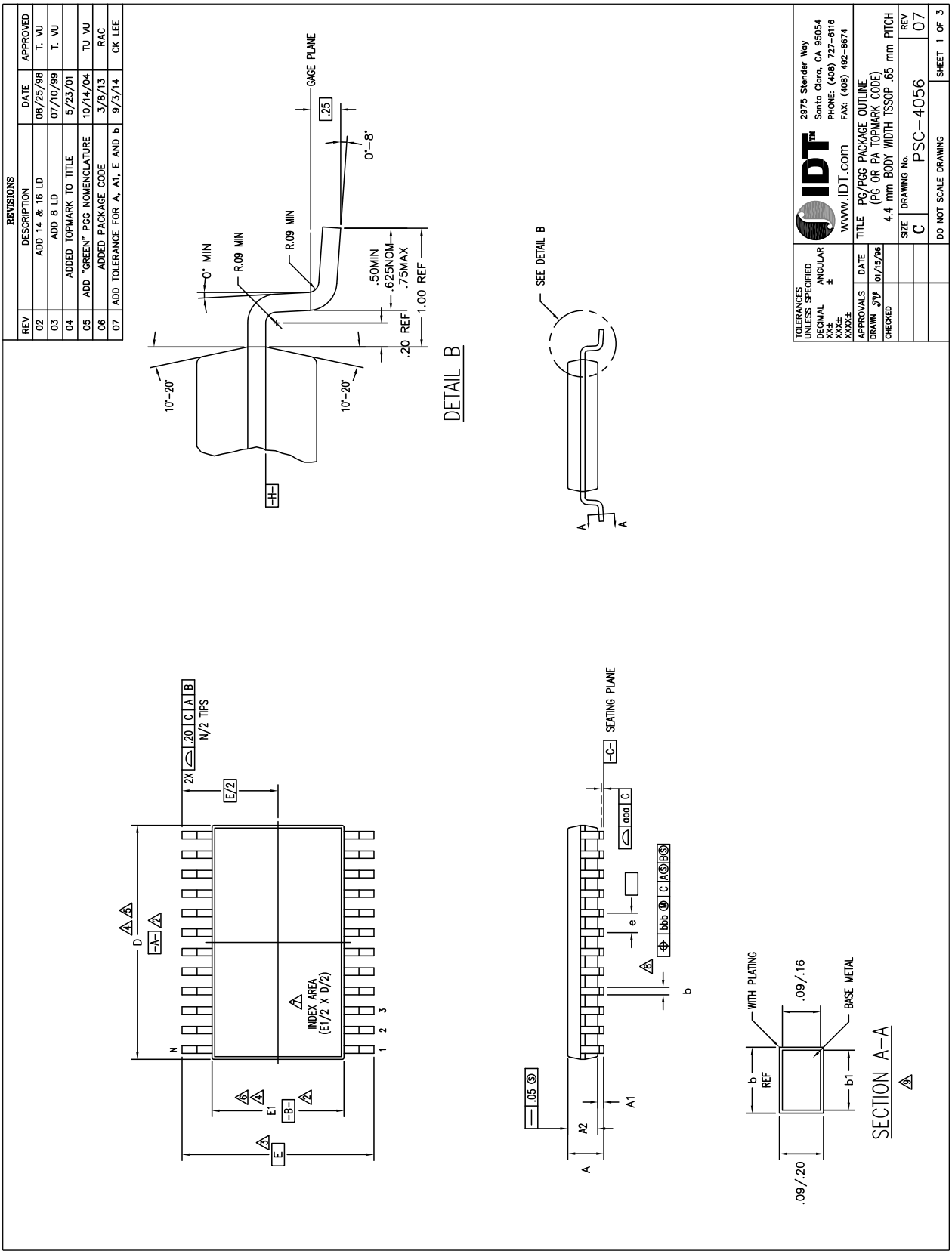
Package Outline and Package Dimensions (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)



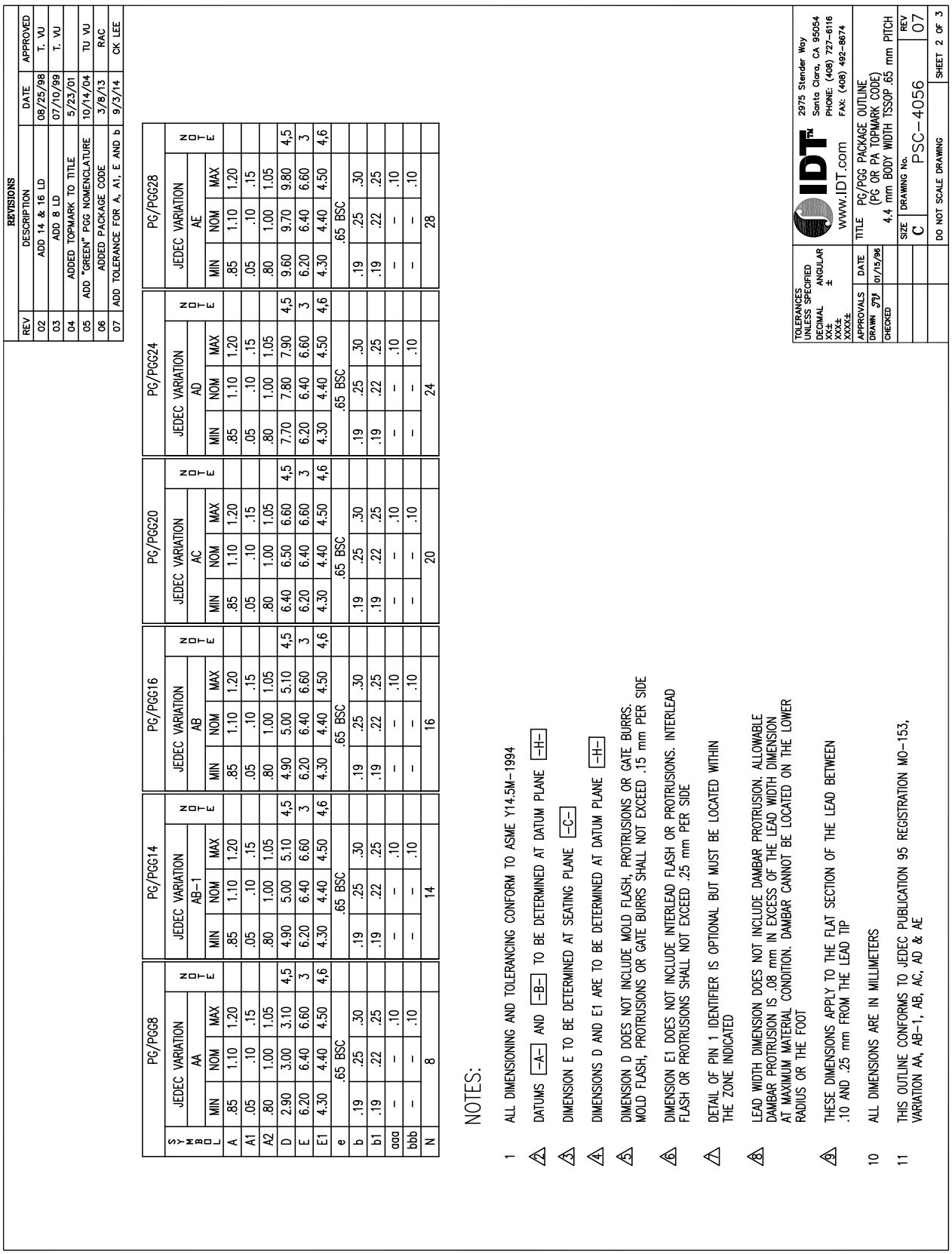
Package Outline and Package Dimensions, cont. (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)



Package Outline and Package Dimensions (8-, 14-, 16-, 20-pin TSSOP)



Package Outline and Package Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD 14 & 16 LD	08/25/98	T. VU
03	ADD 8 LD	07/10/99	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	
05	ADD "GREEN" PGG NOMENCLATURE	10/14/04	TU VU
06	ADDED PACKAGE CODE	3/8/13	RAC
07	ADD TOLERANCE FOR A, A1, E AND b	9/3/14	CK LEE

SYMBOL	PG/PGG8				PG/PGG14				PG/PGG16				PG/PGG20				PG/PGG24				PG/PGG28			
	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB-1			NOTE	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05	
D	2.90	3.00	3.10	4,5	4.90	5.00	5.10	4,5	4.90	5.00	5.10	4,5	6.40	6.50	6.60	4,5	7.70	7.80	7.90	4,5	9.60	9.70	9.80	4,5
E	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3
E1	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6
e	.65 BSC				.65 BSC				.65 BSC				.65 BSC				.65 BSC				.65 BSC			
b	.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30	
b1	.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25	
aaa	–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10	
bbb	–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10	
N	8				14				16				20				24				28			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±

APPROVALS DATE
DRAWN 01/15/96
CHECKED

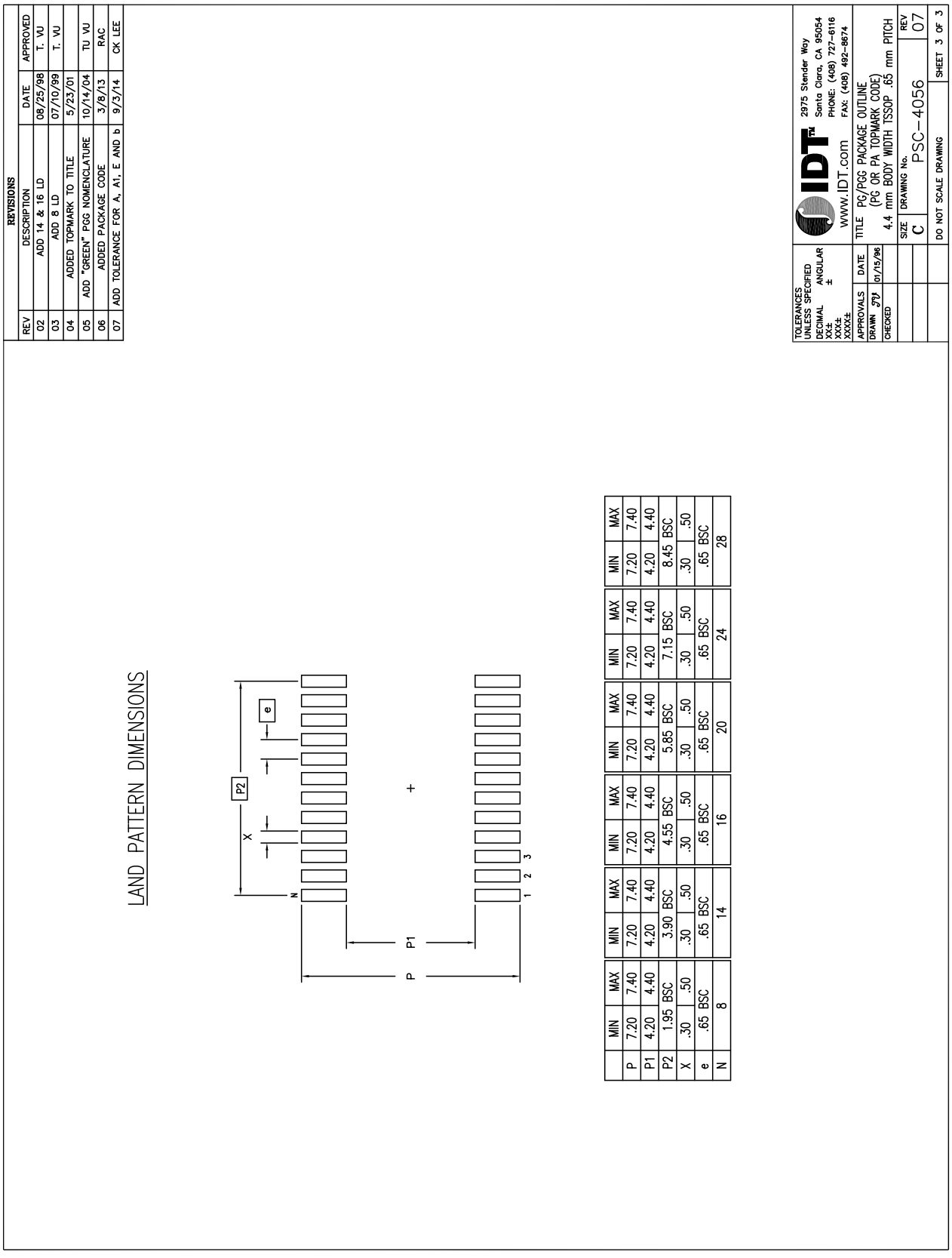
IDT™ www.IDT.com
2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674

TITLE PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE C | DRAWING No. PSC-4056 | REV 07

DO NOT SCALE DRAWING | SHEET 2 OF 3

Package Outline and Package Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P83904PGGK	see page 9	Tubes	16-pin TSSOP	-40° to +105°C
5P83904PGGK8		Tape and Reel	16-pin TSSOP	-40° to +105°C
5P83904CMGK		Cut Tape	16-pin QFN	-40° to +105°C
5P83904CMGK8		Tape and Reel	16-pin QFN	-40° to +105°C
5P83905PGGK		Tubes	16-pin TSSOP	-40° to +105°C
5P83905PGGK8		Tape and Reel	16-pin TSSOP	-40° to +105°C
5P83905CMGK		Cut Tape	16-pin QFN	-40° to +105°C
5P83905CMGK8		Tape and Reel	16-pin QFN	-40° to +105°C
5P83908PGGK		Tubes	20-pin TSSOP	-40° to +105°C
5P83908PGGK8		Tape and Reel	20-pin TSSOP	-40° to +105°C
5P83908NDGK		Tubes	20-pin QFN	-40° to +105°C
5P83908NDGK8		Tape and Reel	20-pin QFN	-40° to +105°C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.
“K” denotes extended temperature range.

Revision History

Rev.	Date	Originator	Description of Change
A	07/11/16	H.G.	Release to final.
B	10/05/16	Y.G.	1. Update "Propagation Delay" typical values per latest characterization data. 2. Update "Output Rise/Fall" maximum values per latest characterization data.

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