Description

The 8T79S308 is a fully integrated signal fanout buffer for high-performance, low additive phase noise applications. The main function of the device is the distribution and fanout of high-frequency clocks or low-frequency synchronization signals.

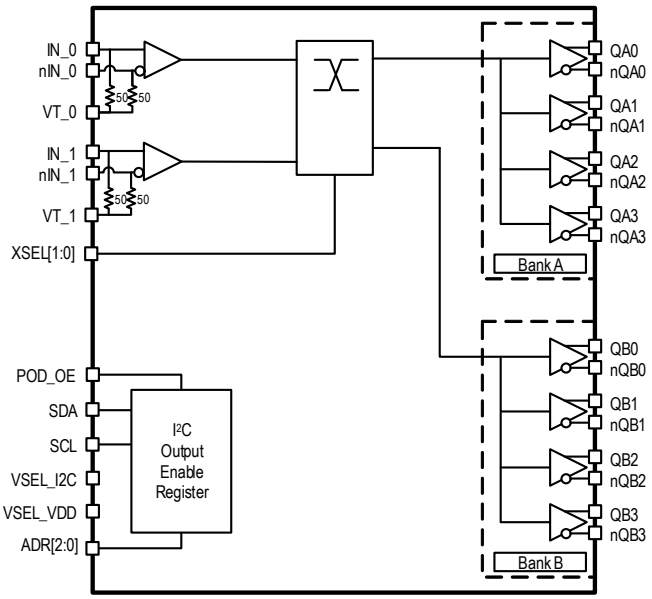
The 8T79S308 is optimized to deliver very low phase noise clocks and precise, low-skew outputs, low device-to-device skew characteristics and fast output rise/fall times help the system design to achieve deterministic clock phase relationship across devices.

The device distributes the input signals (IN_0, IN_1) to two fanout banks. A input select logic allows the device to operate as 1:8 buffer, dual 1:4 buffers, and to cross the input signals.

The propagation delay in both outputs banks is designed for equal delay to support fixed phase relationships between both banks. All outputs are very flexible in LVPECL/LVDS output style configuration, output signal termination, and allow both DC and AC coupling. Outputs can be individually disabled through a serial interface.

The device is packaged in a lead-free (RoHS 6) 40-VFQFPN package. The extended temperature range supports wireless infrastructure, telecommunication, and networking end equipment requirements. The 8T79S308 is a member of the high-performance clock family from IDT.

Block Diagram



Features

- High-performance, flexible clock/data/1PPS fanout buffer
- Low phase noise floor: -160dBc/Hz (156.256MHz clock)
- Integrated phase noise of < 65fs RMS typical (12kHz–20MHz)
- Flexible input selection
  - 1:8 Fanout modes
  - Dual 1:4 Buffer fanout modes
- Eight differential outputs, organized in two banks of four outputs
- Low-power LVPECL/LVDS outputs support DC and AC coupling and LVPECL, LVDS line terminations techniques
- Individually configured outputs through an I^2C interface
  - LVPECL/LVDS output style, HCSL compatible (AC-coupled)
  - Output amplitude
  - Output enable
- Supported clock frequency range: 0 to 3GHz
- Core and output supply voltage modes:
  - 3.3V core, 3.3V, 2.5V, and 1.8V output supply
  - 2.5V core, 2.5V, and 1.8V output supply
- Selectable I^2C I/O interface voltage: 1.8V and VDD
- Integrated low dropout regulators (LDOs) for excellent power supply noise rejection
- Package: 6 × 6 mm 40-VFQFPN
- Temperature range: -40°C to +105°C

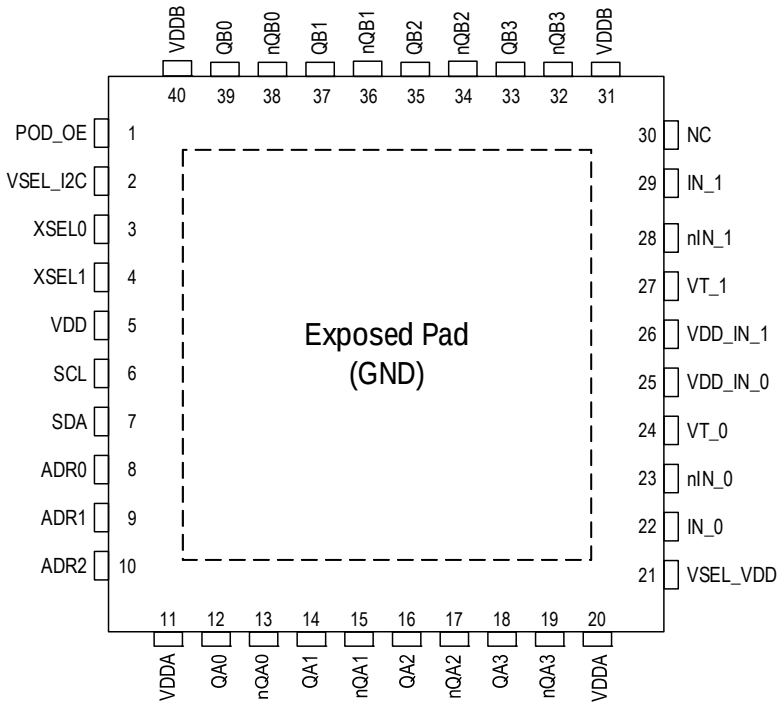
Typical Applications

- Wireless infrastructure applications: GSM, WCDMA, LTE, LTE-A
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Low phase noise clock generation
- Ethernet line cards
- Radar and imaging
- Instrumentation and medical

Contents

Pin Assignments

Figure 1. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions[a]

Pin	Name	Type[b]		Description
Signal Input Pins				
22	IN_0	Input		Device clock 0 inverting and non-inverting differential clock input. Internally terminated 50Ω to VT_0. Compatible with LVPECL, LVDS signals.
23	nIN_0			
24	VT_0	Termination		Input for termination. Both IN_0 and nIN_0 inputs are internally terminated 50Ω to this pin.
29	IN_1	Input		Device clock 1 inverting and non-inverting differential clock input. Internally terminated 50Ω to VT_1. Compatible with LVPECL, LVDS signals.
28	nIN_1			
27	VT_1	Termination		Input for termination. Both IN_1 and nIN_1 inputs are internally terminated 50Ω to this pin.
Signal Output Pins				
12, 13	QA0, nQA0	Output		Differential clock output A0 (Bank A). Configurable LVPECL/LVDS style.
14, 15	QA1, nQA1	Output		Differential clock output A1 (Bank A). Configurable LVPECL/LVDS style.
16, 17	QA2, nQA2	Output		Differential clock output A2 (Bank A). Configurable LVPECL/LVDS style.

Table 1. Pin Descriptions[a] (Cont.)

Pin	Name	Type[b]		Description
18, 19	QA3, nQA3	Output		Differential clock output A3 (Bank A). Configurable LVPECL/LVDS style.
39, 38	QB0, nQB0	Output		Differential clock output B0 (Bank B). Configurable LVPECL/LVDS style.
37, 36	QB1, nQB1	Output		Differential clock output B1 (Bank B). Configurable LVPECL/LVDS style.
35, 34	QB2, nQB2	Output		Differential clock output B2 (Bank B). Configurable LVPECL/LVDS style.
33, 32	QB3, nQB3	Output		Differential clock output B3 (Bank B). Configurable LVPECL/LVDS style.
I^{2}C Serial Interface Pins				
6	SCL	Input		Serial Control Port I^{2}C Clock Input. Interface voltage is selected by the VSEL_I2C pin. Input has hysteresis. Use an external pull-up resistor to the serial interface supply voltage.
7	SDA	Input/ Output		Serial Control Port I^{2}C data I/O. Interface voltage is selected by the VSEL_I2C pin. Input has hysteresis (when input). For output: open collector, use an external pull-up resistor to the selected serial interface supply voltage
LVCMOS Control Function Pins				
8	ADR0	Input	PD	Serial Control Port/I^{2}C Address Bit 0, 1 and 2. LVCMOS interface levels are determined by V_{DD_V} voltage.
9	ADR1	Input	PD	
10	ADR2	Input	PD	
3	XSEL_0	Input	PD	Signal distribution select pins 0 and 1. LVCMOS interface levels are determined by V_{DD_V} voltage.
4	XSEL_1	Input	PD	
2	VSEL_I2C	Input	PD	Interface voltage select for the I^{2}C interface pins. LVCMOS interface levels are determined by V_{DD_V} voltage.
21	VSEL_VDD	Input	PD	Core supply voltage select. Set this pin to 0 or 1 according to the applied core voltage (2.5V or 3.3V) of the device. LVCMOS interface levels.
30	NC	-		No connect.
1	POD_OE	Input	PD	Power-on default output-enable state. LVCMOS interface levels are determined by V_{DD_V} voltage.
Power Pins and Exposed Pad Connection				
25	VDD_IN_0	Power		Positive supply voltage (3.3V, 2.5V) for the IN_0/nIN_0 input.
26	VDD_IN_1	Power		Positive supply voltage (3.3V, 2.5V) for the IN_1/nIN_1 input.
11, 20	VDDA	Power		Positive supply voltage (3.3V, 2.5V, 1.8V) for the QA[3:0] outputs.
31, 40	VDDB	Power		Positive supply voltage (3.3V, 2.5V, 1.8V) for the QB[3:0] outputs.
5	VDD	Power		Positive supply voltage (3.3V, 2.5V) for the device core functions.
—	GND	Power		Exposed pad: Ground supply voltage (GND) and ground return path. Connect to board GND (0V).

[a] For essential information on power supply filtering, see Application Information.

[b] PU (pull-up) and PD (pull-down) indicate internal input resistors (for values, see Figure 13).

Principles of Operation

Overview

The 8T79S308 is designed for low phase noise and skew critical differential clock distribution systems and supports clock frequencies from 1PPS up to 3GHz. An input-to-output cross-connect, individually configurable LVPECL/LVDS outputs, amplitude settings and output enable make this device very flexible. The power-up default output enable state can be set by an dedicated control input. An I^2C interface is available for individual output configurations. The signal voltage level of the I^2C interface pins is configurable to 1.8V and 2.5V/3.3V voltage supply. The configurable I^2C slave address pins are available to allow up to eight devices on the same I^2C bus.

Signal flow: The device can be configured as single 1:8 or dual 1:4 buffer with selectable IN_0 and IN_1 inputs as signal source, controlled by the XSEL[1:0] configuration input.

The output style state of each individual differential output Q, nQ can be set by the content the I^2C register 0x10 (see Table 10). A logic zero to an I^2C bit in register 0x10 sets corresponding differential output to LVPECL, while a logic one sets the differential output to LVDS (see Table 11). Register 0x10 resets to logic 0 (all outputs: LVPECL) at each power-up. Setting and changing the output style through the I^2C interface is asynchronous to the input reference clock.

The output amplitude of each individual differential output Q, nQ can be set by the content of the I^2C registers 0x11–0x12 (see Table 11). For LVPECL outputs, the device supports amplitude settings of 500mV and 750mV; for LVDS outputs, 350mV and 500mV are supported. Register 0x11-0x12 reset to logic 0 (LVPECL standard amplitude) at each power-up. Setting and changing the output style through the I^2C interface is asynchronous to the input reference clock. For LVPECL, the output termination has to be adjusted for the selected amplitude.

The output enable/disable state of each individual differential output Q, nQ can be set by the content of I^2C register 0x13 (see Table 11). A logic zero to an I^2C bit in register 0x02 disables the corresponding differential output in high-impedance state, while a logic one enables the differential output (see Table 11). After each power cycle, the device copies the state of the POD_OE input into all eight bits (D7-0) of register 0x13 to: If pin POD_OE = 0 or open, the device powers up with all outputs disabled in high-impedance state, if pin POD_OE=1, the device powers up with all outputs enabled. After the first valid I^2C write, the output enable state is controlled by the I^2C register 0x13. Setting and changing the output enable state through the I^2C interface is asynchronous to the input reference clock.

Voltage Supply

Table 2. Supported Voltage Supply Operations

Core Supply V_{DD_V} [a][b]	Output Supply V_{DD_O} [c][d]
3.3V	3.3V, 2.5V, 1.8V
2.5V	2.5V, 1.8V

[a] V_{DD_V} denominates V_{DD}, $V_{DD\_IN\_1}$, $V_{DD\_IN\_0}$. I^2C interface levels are configured by the VSEL_I2C pin.

[b] V_{DD_V} core supply voltages must be equal: $V_{DD} = V_{DD\_IN\_0} = V_{DD\_IN\_1}$.

[c] V_{DD_O} denominates V_{DDA} and V_{DDB}. $V_{DD\_V} \geq V_{DD\_O}$.

[d] $V_{DDA} = V_{DDB}$ and $V_{DDA} \neq V_{DDB}$ are both supported voltage operations.

Pin Controlled Settings

Table 3. Output State Power-On Default Setting

POD_OE	Operation
0 (default)	After power-up and before the first I^2C access, the outputs Qn, nQn are disabled in high impedance state.
1	After power-up and before the first I^2C access, the outputs Qn, nQn are enabled.

Table 4. I^2C Interface Voltage Select

VSEL_I2C	Operation
0 (default)	I^2C Interface voltage (SDA, SCL) is 1.8V. The 1.8V voltage supply is regulated internally and is independent on the V_{DD_V} voltage.
1	I^2C Interface voltage (SDA, SCL) is equal to the voltage supplied to V_{DD_V} (2.5V or 3.3V).

Table 5. Core Voltage Supply Select

VSEL_VDD	Operation
0 (default)	V_{DD_V} core voltage is 2.5V.
1	V_{DD_V} core voltage is 3.3V.

Input Signal Selection

Table 6. Input Signal and Buffer Signal Flow Selection

XSEL_1	XSEL_0	Signal Flow	Description
0 (default)	0 (default)	IN_0 → QA0-3 and QB0-3	1:8 Buffer
0	1	IN_0 → QA0-3 IN_1 → QB0-3	Dual 1:4 Buffer
1	0	IN_0 → QB0-3 IN_1 → QA0-3	Dual 1:4 Buffer, crossed signals
1	1	IN_1 → QA0-3 and QB0-3	1:8 Buffer (from IN_1)

Configuration Registers

Table 7. Configuration Registers

Register Address	Register Description
0x00-0x02	Reserved
0x03	Device Type
0x04	Device ID
0x05	Device ID
0x06	Device Version
0x07-0x0B	Reserved
0x0C	Vendor ID
0x0D	Vendor ID
0x0E	I^2C Address
0x0F	Reserved
0x10	Output Style
0x11	Output Amplitude
0x12	Output Amplitude
0x13	Output Enable
0x14-0x1F	Reserved

Device Information Registers

Table 8. Device Information Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x03	DEV_TYPE[7:0]							
0x04	DEV_ID[7:0]							
0x05	DEV_ID[15:8]							
0x06	DEV_VER[7:0]							
0x0C	VENDOR_ID[7:0]							
0x0D	VENDOR_ID[15:8]							
0x0E	Reserved	I2C_ADR						

Table 9. Device Information Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
DEV_TYPE[7:0]	R only	0x07	Device (Chip) Type Reads 0x07 (RF-Buffer) after power-up and reset.
DEV_ID[15:0]	R only	0x04: 0100 0011 0x05: 0000 0000 Value: 0x0043	Device ID Device is composed of registers 0x05 (high byte) and register 0x04 (low byte). Reads 0x0043 after power-up and reset.
DEV_VER[7:0]	R only	0x00 Value: 0x00	Device Version 0x00. Reads 0x00 (First silicon revision) after power-up and reset.
VENDOR_ID	R only	0x0C: 0010 0110 0x0D: 0000 0100 Value: 0x0426	Vendor ID 0x0426 (Integrated Device Technology, IDT). Reads 0x0426 (IDT) after power-up and reset.

Table 9. Device Information Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
I2C_ADR[6:0]	R	1101 [ADR2] [ADR1] [ADR0]	I^2C Device address This read-only register stores the binary I^2C device address: 1101[ADR2][ADR1][ADR0]. Bit D2 is equal to the logic state of the ADR2 pin Bit D1 is equal to the logic state of the ADR1 pin Bit D0 is equal to the logic state of the ADR0 pin. This register cannot be used to change the device address.

Device Configuration Registers

Table 10. Device Configuration Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x10	STYLE_QB3	STYLE_QB2	STYLE_QB1	STYLE_QB0	STYLE_QA3	STYLE_QA2	STYLE_QA1	STYLE_QA0
0x11	A_QB3		A_QB2		A_QB1		A_QB0	
0x12	A_QA3		A_QA2		A_QA1		A_QA0	
0x13	OE_QB3	OE_QB2	OE_QB1	OE_QB0	OE_QA3	OE_QA2	OE_QA1	OE_QA0

Table 11. Device Configuration Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
STYLE_Qn	R/W	0	0 = Output is LVPECL. 1 = Output is LVDS.

Table 11. Device Configuration Register Descriptions

<table>
<tr><th colspan="5">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">A_Qn</td><td rowspan="6">R/W</td><td rowspan="6">00</td><td colspan="2">Output Amplitude</td></tr>
<tr><td>A_Qn[1:0]</td><td>Amplitude if Output is LVPECL</td><td>Amplitude if Output is LVDS</td></tr>
<tr><td>00</td><td>750mV (standard LVPECL)
Output termination: see Figure</td><td rowspan="2">500mV amplitude (high-amplitude LVDS)
Output termination: 100Ω between Q, nQ; see Figure 7, Figure 8, Figure 9.</td></tr>
<tr><td>01</td><td>500mV (low-amplitude LVPECL)
Output termination: see Figure</td></tr>
<tr><td>10</td><td>Reserved</td><td>350mV amplitude (standard LVDS)
Output termination: 100Ω between Q, nQ; see Figure 7, Figure 8, Figure 9.</td></tr>
<tr><td>11</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td colspan="3">V_{DD_O} = 1.8V: output amplitudes of 350mV and 500mV are available, 750mV is not available.</td></tr>
<tr><td>OE_Qn</td><td>R/W</td><td>POD_OE pin state</td><td colspan="2">Output Enable
0 = Output Qn, nQn is disabled in the high-impedance state.
1 = Output Qn, nQn is enabled.
After each power cycle, the device copies the state of the POD_OE input to all eight bits (D7-0) of this register. If pin POD_OE = 1 or open, the device powers up with all outputs enabled, if pin POD_OE=0, the device powers up with all outputs disabled in high-impedance state. After the first valid I^2C write, the output enable state is controlled by this register.</td></tr>
</table>

Serial Interface

The 8T79S308 supports an I^2C configuration interface.

I^2C Interface

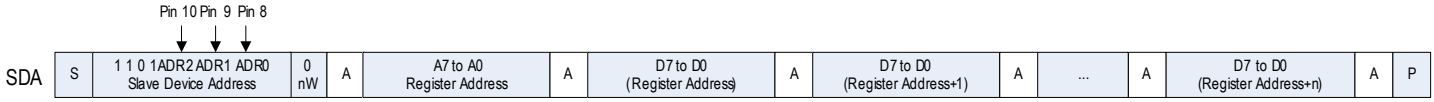
The device will respond as a slave in an I^2C compatible configuration at a base address of 1101[ADR2, ADR1, ADR0]b, to allow access to any of the internal registers for device programming or examination of internal status. The ADR[2:0] bits of the I^2C interface address are set by the logic state of the ADR2 (pin 10), ADR1 (pin 9) and ADR0 (pin 8) inputs. If more than one 8T79S308 device is connected to the same I^2C bus, set ADR[2:0] to different states on each device to avoid address conflicts.

The I^2C interface is designed to fully support v1.2 of the I^2C Specification for Normal and Fast mode operation. The device acts as a slave device on the I^2C bus at 100kHz or 400kHz using a fixed base address of 1101[ADR2, ADR1, ADR0]b. The interface accepts byte-oriented block write and block read operations. One address byte specifies the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data is moved into the registers byte by byte and before a STOP bit is received.

The device implements registers in the address range 0x00 to 0x1F. Write access to the address range 0x20-0xFF has no effect, read access to this range will return 0x00.

For full electrical I^{2}C compliance, it is recommended to use external pull-up resistors for SDA and SCL. The internal pull-up resistors have a size of 51kΩ typical.

Figure 2. I^{2}C Write Data (Master Transmit, Slave Receive) from any Register Address



Write to slave to the specified register address A [7:0]. The slave auto -increments the register address and data is written sequentially .

S Start (Master)

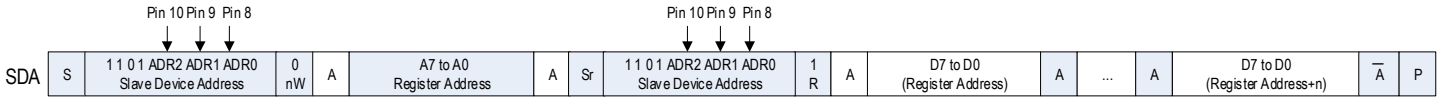
P Stop (Master)

A Acknowledge (Slave to Master)

Master transmit, Slave Receive

Slave transmit, Master Receive

Figure 3. I^{2}C Read Data (Slave Transmit, Master Receive) from any Register Address



Read from slave from the specified register address A[7:0]. Data is transmitted to the master after a change of the transfer direction with a repeated start. The slave auto-increments the register address and transmits register data to the master sequentially.

S Start (Master)

Sr Repeated start (Master)

P Stop (Master)

A Acknowledge (Slave to Master)

A Acknowledge (Master to Slave)

Master transmit, Slave Receive

Slave transmit, Master Receive

$\overline{A}$ No Acknowledge (Master to Slave)

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8T79S308 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 12. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD_V}, V_{DD_O}	3.6V
Inputs	-0.5V to V_{DD_V} + 0.5V
Outputs, V_O (SDA)	-0.5V to V_{DD_O} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 50mA 100mA
Input termination current, I_{VT}	±35mA
Operating Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[a]	2000V
ESD - Charged Device Model[a]	500V

[a] According to JEDEC JS-001-2012/JESD22-C101

Pin Characteristics

Table 13. Pin Characteristics, V_{DD_V} = (3.3V or 2.5V) ±5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ±5%, T_A = -40°C to +105°C (Case)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}[a]	Input Capacitance	IN_0, nIN_0, IN_1, nIN_1.		2	4	pF
		Other inputs.		2	4	pF
R_{PD}	Input Pull-Down Resistor			51		kΩ
R_T	Input Termination Impedance	IN_0, nIN_0 to VT_0. IN_1, nIN_1 to VT_1.		50 50		Ω

[a] Guaranteed by design.

DC Characteristics

Table 14. Power Supply DC Characteristics, V_{DD_V} = (3.3V or 2.5V) ±5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ±5%, T_A = -40°C to +105°C (Case)[a][b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_V}	Core Supply Voltage		2.5 - 5% 3.3 - 5%	2.5 3.3	2.5 + 5% 3.3 + 5%	V
V_{DD_O}	Output Supply Voltage		2.5 - 5% 3.3 - 5% 1.8 - 5%	2.5 3.3 1.8	2.5 + 5% 3.3 + 5% 1.8 + 5%	V
I_{DD_V} + I_{DD_O}	Total Power Supply Current	V_{DD_V} = V_{DD_O} = 2.5V.		395	457	mA
		V_{DD_V} = V_{DD_O} = 3.3V.		406	467	
		V_{DD_V} = 2.5V, V_{DD_O} = 1.8V.		345	395	

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] $V_{DD\_V} \geq V_{DD\_O}$

Table 15. Typical Power Supply DC Current Characteristics, V_{DD_V} = 3.3V, V_{DD_O} = 3.3V, T_A = 25°C[a][b]

Symbol	Supply Pin Current		Test Case 1	Test Case 2	Test Case 3	Test Case 4	Unit
	Qn	Style	LVPECL	LVPECL	LVDS	LVDS	
		State	On	On	On	On	
		Amplitude	500	750	350	500	mV
I_{DD_CA}	Current through VDD pin		4	4	4	4	mA
I_{DD_CB}	Current through VDDA pin		135	160	108	112	mA
I_{DD_CC}	Current through VDDB pin		135	160	108	112	mA
I_{DD_CD}	Current through VDD_IN_0 pin		41	41	40	40	mA
I_{DD_CE}	Current through VDD_IN_1 pin		41	41	40	40	mA
P_{TOT}	Total Device Power Consumption		0.709	0.805	0.99	1.02	W
$P_{TOT, SYS}$	Total System Power Consumption[c]		1.18	1.34	0.99	1.02	W

[a] Configuration: f_{CLK} (input) = 245.76MHz, Qn outputs terminated according to amplitude settings.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Includes total device power consumption and the power dissipated in external output termination components.

Table 16. Typical Power Supply DC Current Characteristics, V_{DD_V} = 2.5V, V_{DD_O} = 2.5V, T_A = 25°C[a][b]

Symbol	Supply Pin Current		Test Case 1	Test Case 2	Test Case 3	Test Case 4	Unit
	Qn	Style	LVPECL	LVPECL	LVDS	LVDS	
		State	On	On	On	On	
		Amplitude	500	750	350	500	mV
I_{DD_CA}	Current through VDD pin		4	4	4	4	mA
I_{DD_CB}	Current through VDDA pin		131	156	107	111	mA
I_{DD_CC}	Current through VDDB pin		131	156	107	111	mA
I_{DD_CD}	Current through VDD_IN_0 pin		40	40	39	39	mA
I_{DD_CE}	Current through VDD_IN_1 pin		40	40	39	39	mA
P_{TOT}	Total Device Power Consumption		0.587	0.672	0.98	1.00	W
$P_{TOT, SYS}$	Total System Power Consumption[c]		1.15	1.31	0.98	1.00	W

[a] Configuration: f_{CLK} (input) = 245.76MHz, Qn outputs terminated according to amplitude settings.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Includes total device power consumption and the power dissipated in external output termination components.

Table 17. LVCMOS Input DC Characteristics, V_{DD_V} = (3.3V or 2.5V) ± 5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ±5%, T_A = -40°C to +105°C (Case)[a][b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD_V} = 2.5V.	1.7		V_{DD_V}	V
			V_{DD_V} = 3.3V.	2		V_{DD_V}	V
V_{IL}	Input Low Voltage			-0.3		0.5	V
I_{IH}	Input High Current	Input with pull-down resistor	V_{DD_V} = 2.5V or 3.3V. V_{IN} = V_{DD_V}			150	µA
I_{IL}	Input Low Current		V_{DD_V} = 2.5V or 3.3V. V_{IN} = 0V.	-5			µA

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVCMOS inputs: ADR[2:0], XSEL[1:0], VSEL_VDD, VSEL_I2C, and POD_OE.

Table 18. I^2C Input/Output DC Characteristics, V_{DD_V} = (3.3V or 2.5V) ± 5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ±5%, T_A = -40°C to +105°C (Case)[a][b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_I	Input Voltage			-0.3		3.3V	V
V_{T+}	Positive-going input threshold voltage		VSEL_I2C = 0. VSEL_I2C = 1, V_{DD_V} = 2.5V. VSEL_I2C = 1, V_{DD_V} = 3.3V.	0.660	 1.10–1.40 1.45–1.75	1.365	V
V_{T-}	Negative-going input threshold voltage		VSEL_I2C = 0. VSEL_I2C = 1, V_{DD_V} = 2.5V. VSEL_I2C = 1, V_{DD_V} = 3.3V.	0.495	0.91 0.65–0.95 0.8–1.1	1.170	V
V_H	Hysteresis Voltage	V_{T+} - V_{T-}	VSEL_I2C = 0. VSEL_I2C = 1, V_{DD_V} = 2.5V. VSEL_I2C = 1, V_{DD_V} = 3.3V.	0.165	0.6 0.15–0.45 0.5–0.8	0.780	V
I_{IH}	Input High Current		V_{DD_V} = 2.5V or 3.3V. V_{IN} = V_{DD_V}			150	µA
I_{IL}	Input Low Current		V_{DD_V} = 2.5V or 3.3V. V_{IN} = 0V.	-5			µA
V_{OL}	Output Low Voltage		VSEL_I2C = 0, I_{OL} = 4mA. VSEL_I2C = 1, I_{OL} = 4mA.		0.292 0.292	0.55	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Valid for inputs/outputs: SCL and SDA. Inputs have hysteresis and tolerate any voltage up to 3.3V.

Table 19. Differential Input DC Characteristics, V_{DD_V} = (3.3V or 2.5V) ± 5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ± 5%, T_A = -40°C to +105°C (Case)[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IN}	Input Voltage Swing	IN_0, IN_1		0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		2.4	V
V_{CMR}	Common Mode Input Voltage			1		V_{DD_V} - (V_{IN}/2)	V
R_T	Input Termination Impedance		IN_0, nIN_0 to VT_0, IN_1, nIN_1 to VT_1.	40	50	60	Ω
R_{T_DIFF}	Differential Input Termination Impedance		IN_0 to nIN_0. IN_0 to nIN_1.	80	100	120	Ω

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 20. LVPECL DC Characteristics (QAn, QBn), V_{DD_V} = (3.3V or 2.5V) ± 5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ± 5%, T_A = -40°C to +105°C (Case)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	Amplitude = 750mV. Amplitude = 500 mV.	V_{DD_O} - 1.04 V_{DD_O} - 0.99	V_{DD_O} - 0.9 V_{DD_O} - 0.89	V_{DD_O} - 0.83 V_{DD_O} - 0.82	V
V_{OL}	Output Low Voltage	Amplitude = 750mV. Amplitude = 500 mV.	V_{DD_O} - 1.73 V_{DD_O} - 1.48	V_{DD_O} - 1.62 V_{DD_O} - 1.38	V_{DD_O} - 1.56 V_{DD_O} - 1.33	V

Table 21. LVDS DC Characteristics (QAn, QBn), V_{DD_V} = (3.3V or 2.5V) ± 5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ± 5%, T_A = -40°C to +105°C (Case)[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OS}	Offset Voltage[b]	V_{DD_O} = 3.3V	500mV Amplitude. 350mV Amplitude.	1.8 1.9	2.3 2.3	2.8 2.9	V
V_{OS}	Offset Voltage[c]	V_{DD_O} = 2.5V	500mV Amplitude. 350mV Amplitude.	1.05 1.10	1.42 1.42	1.75 1.80	V
V_{OS}	Offset Voltage[d]	V_{DD_O} = 1.8V	500mV Amplitude. 350mV Amplitude.	0.40 0.45	0.70 0.78	1.0 1.1	V
ΔV_{OS}	V_{OS} Magnitude Change				10	50	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{OS} changes with V_{DD_O}.

[c] V_{OS} changes with V_{DD_O}.

[d] V_{OS} changes with V_{DD_O}.

AC Characteristics

Table 22. AC Characteristics, V_{DD_V} = (3.3V or 2.5V) ± 5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ± 5%, T_A = -40°C to +105°C (Case)[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Signal Input and Output Frequency			0		3000	MHz
f_{SCL}	I^2C Clock Frequency					400	kHz
V_{IN}	Input Voltage Amplitude[b]	IN_*n*		0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Amplitude[b][c]	IN_*n*		0.3		2.4	V
V_{CMR}	Common Mode Input Voltage			1.0		V_{DD_V} – ($V_{IN\ /\ 2}$)	V
odc	Output Duty Cycle		QAn, QBn (Clock)	45	50	55	%
			QAn, QBn (Clock) > 2.5GHz	40	50	60	
t_R / t_F	Output Rise/Fall Time, Differential		QAn, QBn (Clock), 20% to 80%.		100	200	ps
			QAn, QBn, 20% to 80%.		100	200	ps
$V_{O(PP)}$	LVPECL Output Voltage Swing, Peak-to-peak	750mV	1GHz.	630	730	830	mV
		750mV	2GHz.	640	744	850	mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak	750mV	1GHz.	1260	1460	1660	mV
		750mV	2GHz.	1280	1488	1700	mV
V_{OD}	LVDS Output Voltage Swing, Peak-to-peak	350mV	1GHz.	280	360	420	mV
		350mV	2GHz.	230	360	470	mV
V_{OD}	LVDS Differential Output Voltage Swing, Peak-to-peak	350mV	1GHz.	560	720	840	mV
		350mV	2GHz.	460	720	940	mV
t_{PD}	Propagation delay between any signal input and any QAn, QBn output					750	ps
t_{PDZ}	Output enable and disable time		From active state to disable[d] From disable to active state[e]		1 30	3 50	µs
*t*sk(o)	Output Skew[f][g]		Within one output bank.		10	25	ps
			Any output.		16	35	ps
*t*sk(pp)	Part-to-part Skew[f][g]					200	ps
*t*sk(p)	Output Pulse Skew[g]		Any output.		21	50	ps
L(∞)	Output Noise Floor		QAn, QBn, 156.25MHz. LVDS Outputs		-160	-155	dBc
			QAn, QBn, 156.25MHz. LVPECL Outputs		-160	-157	

Table 22. AC Characteristics, V_{DD_V} = (3.3V or 2.5V) ± 5%, V_{DD_O} = (3.3V or 2.5V or 1.8V) ± 5%, T_A = -40°C to +105°C (Case)[a] (Cont.)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
L	Additive Phase Noise, RMS	QAn, QBn, 156.25MHz (12kHz–20MHz).		60	100	fs
		QAn, QBn, 245.76MHz (12kHz–20MHz).		50	80	fs
		QAn, QBn, 245.76MHz (1kHz–61.44MHz).		95	110	fs
ΔF	Output isolation between any neighboring clock output	f_{OUT} = 125MHz.		80	75	dB
		f_{OUT} = 245.76MHz.		75	70	dB
ΔF	Input isolation between any signal input	f_{IN} = 125MHz.		80	75	dB
		f_{IN} = 245.76MHz.		75	70	dB
CMNR	Common mode noise rejection[h]	f_{IN} = 156.25MHz.		-90		dBc

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD_V}.

[c] Common Mode Input Voltage is defined as the cross-point voltage.

[d] Measured from I^2C slave acknowledge bit to output in high-impedance state. Verified by simulation.

[e] Measured from I^2C slave acknowledge bit to output in active low/high state. Verified by simulation.

[f] This parameter is defined in accordance with JEDEC standard 65.

[g] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

[h] Measured at a differential output using a balun. DC/DC voltage supply as aggressor, ~490kHz switching frequency. Device power supply bypass as shown in example schematics.

Table 23. Typical Qn Output Amplitude, T_A = 25°C[a]

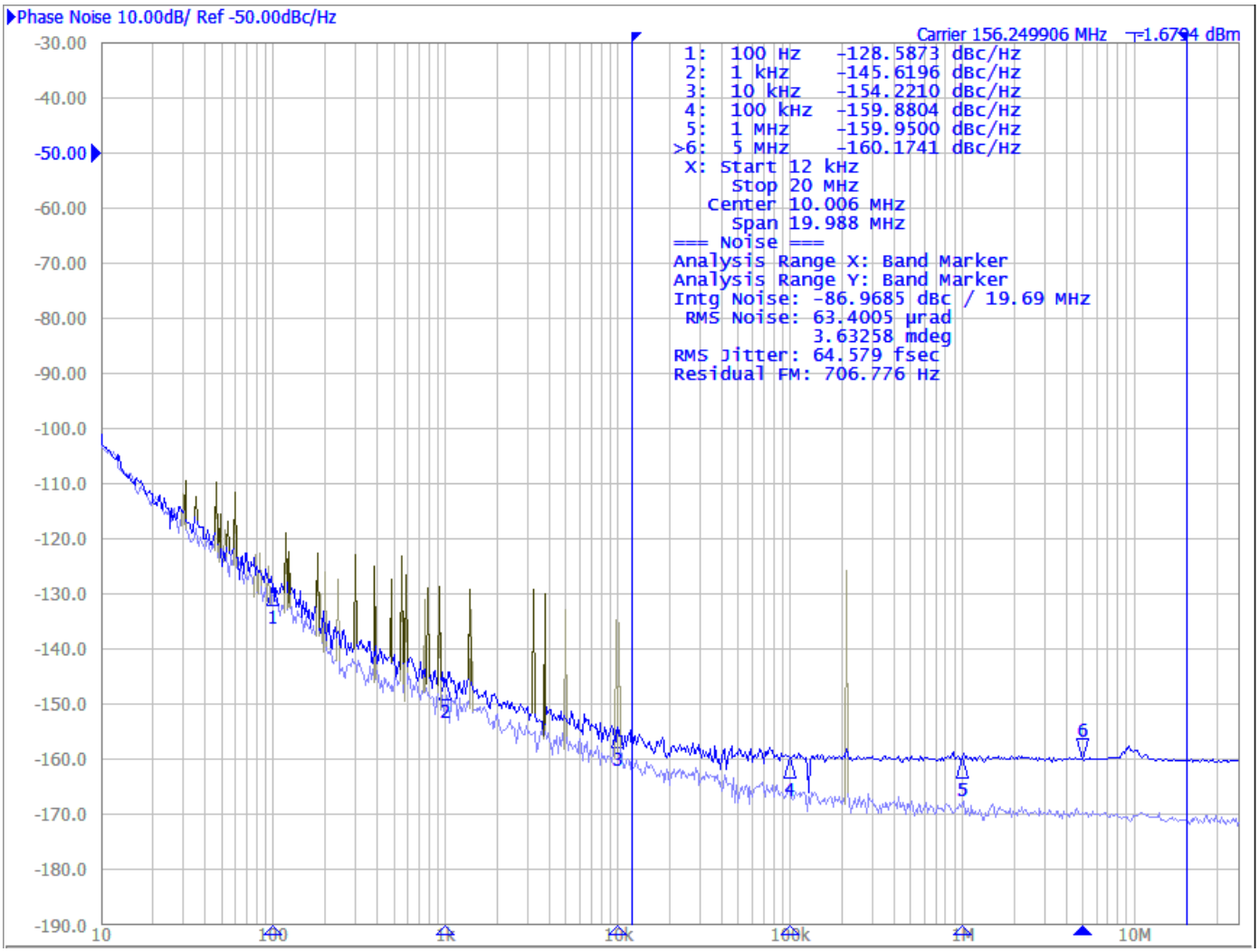
Symbol	Parameter	Test Conditions		Qn Output Frequency in MHz					Units
		Supply voltage	Output Amplitude	245.76	491.52	983.04	1966.08	2949.12	
$V_{O(PP)}$[b]	LVPECL Output Voltage Swing, Peak-to-peak	V_{DD_V} = V_{DD_O} = 3.3V	500mV	540	490	499	499	351	mV
			750mV	783	710	722	720	506	mV
		V_{DD_V} = V_{DD_O} = 2.5V	500mV	538	494	499	518	376	mV
			750mV	773	705	717	732	530	mV
		V_{DD_V} = 2.5 V_{DD_O} = 1.8V	500mV	523	481	489	505	373	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL outputs terminated with 50Ω to V_{DD_V} – 1.75V (500mV amplitude setting), V_{DD_V} – 2.0V (750mV amplitude setting).

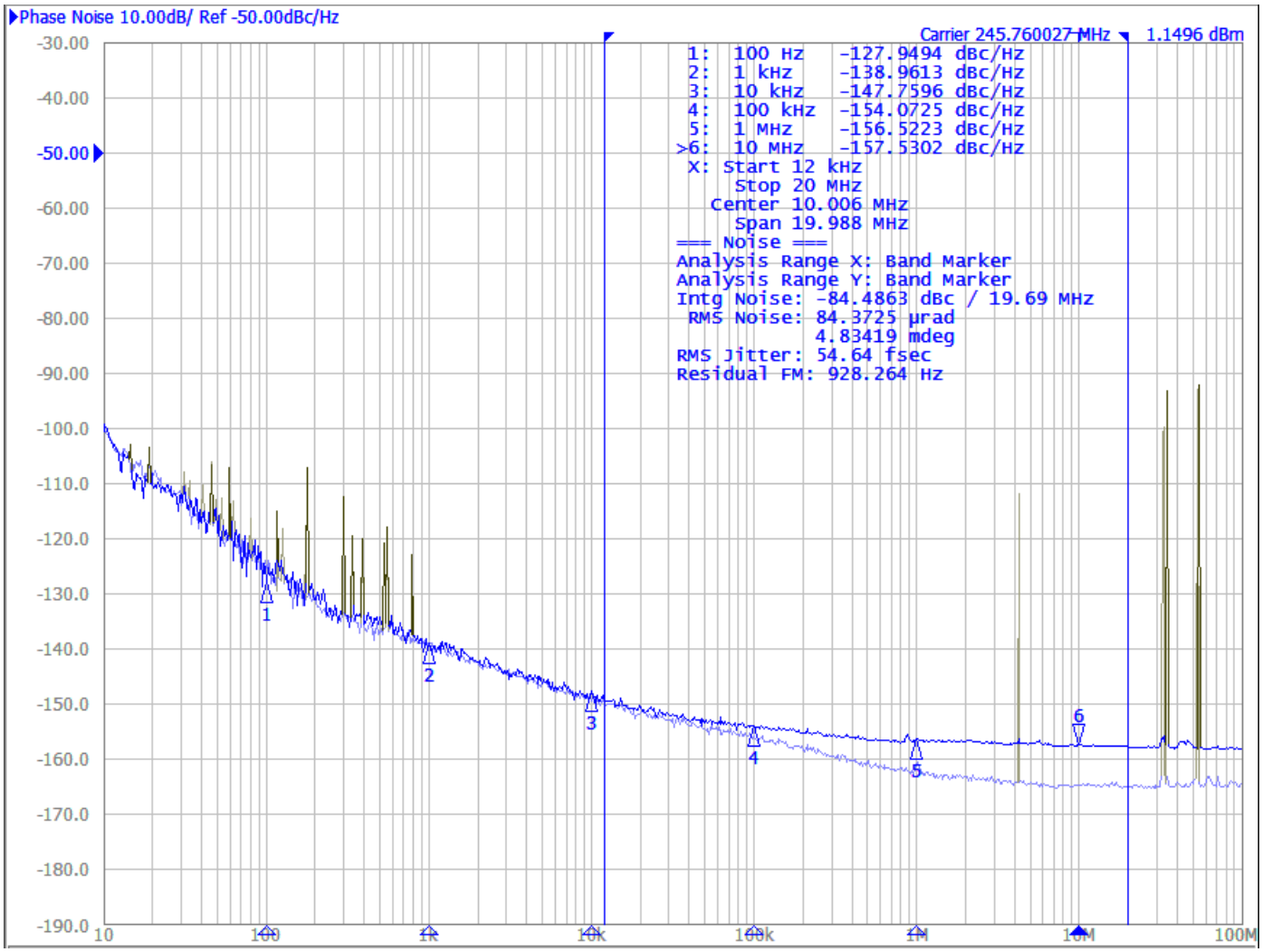
Phase Noise Plots

Figure 4. Typical Phase Noise at 156.25MHz



* Thick line: 8T79S308 output
Thin line: Wenzel oscillator drives 8T79S308 input

Figure 5. Typical Phase Noise at 245.76MHz

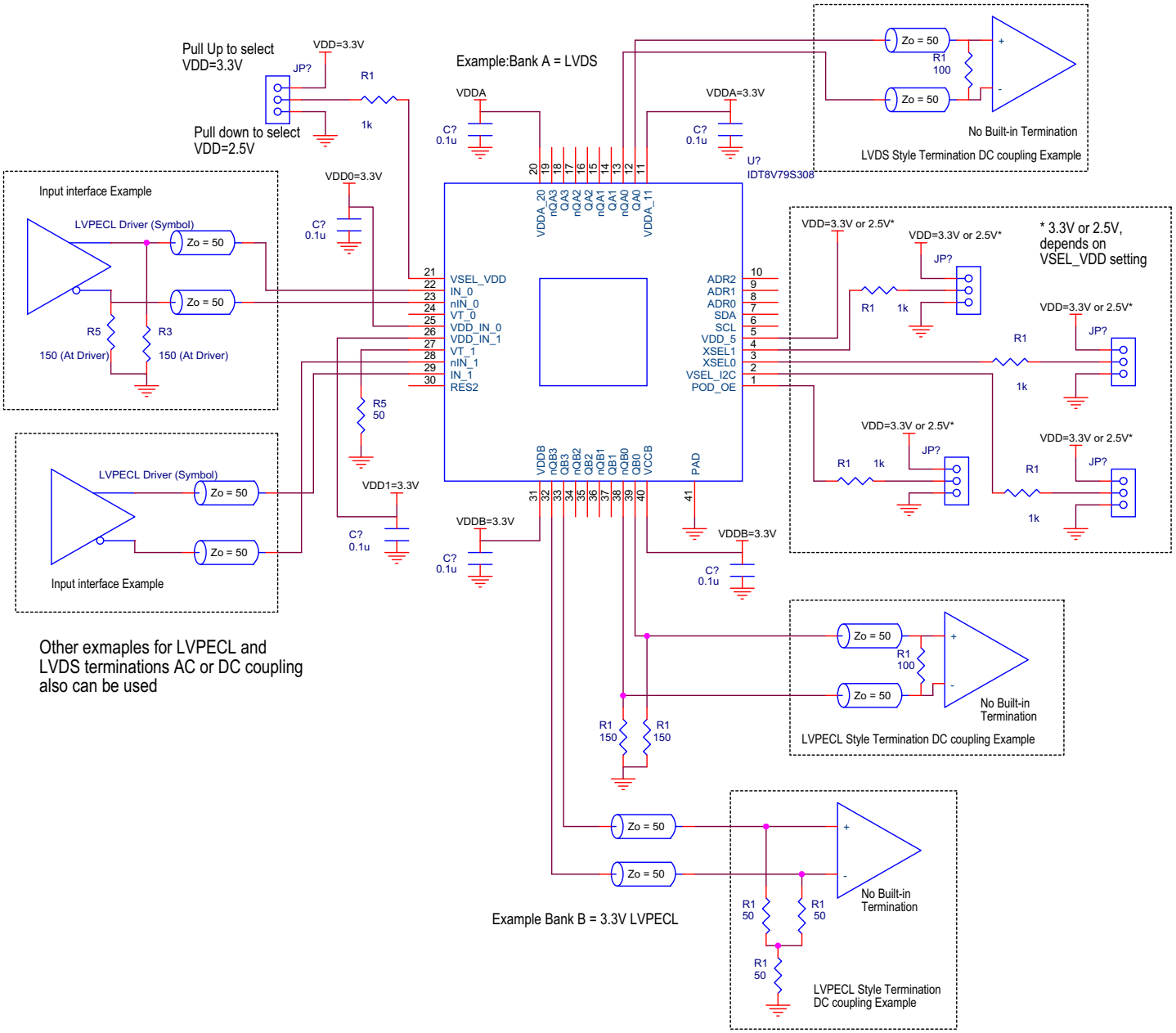


* Thick line: 8T79S308 output
Thin line: Wenzel oscillator drives 8T79S308 input

Application Information

The figure below shows an example schematics. Due to the excellent common-mode noise rejection characteristics, this device uses standard power supply bypass techniques and does not require dedicated, active power supply circuitry for noise rejection purpose.

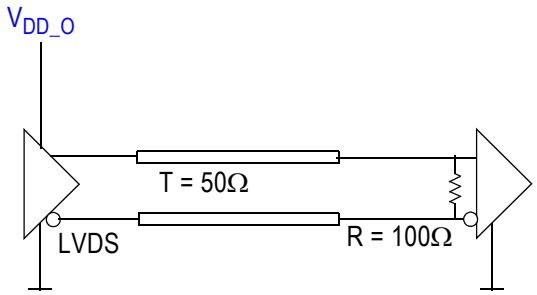
Figure 6. Application Information



Termination for Q, nQ LVDS Outputs

Figure 7 shows an example termination for the Q, nQ LVDS outputs. In this example, the characteristic transmission line impedance is 50Ω. The termination resistor R (100Ω) is matched to the line impedance. The termination resistor must be placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit. The LVDS termination in Figure 7 is applicable for any output amplitude setting specified in Table 9.

Figure 7. LVDS Output Termination



AC Termination for Q, nQ Outputs

Figure 8 and Figure 9 show example AC terminations for the Q, nQ LVDS outputs. In the examples, the characteristic transmission line impedance is 50Ω. In Figure 8, the termination resistor R (100Ω) is placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit, which is shown in Figure 9. The LVDS terminations in both Figure 8 and Figure 9 are applicable for any output amplitude setting specified in Table 9. The receiver input should be re-biased according to its common mode range specifications.

Figure 8. LVDS (STYLE = 0) AC Output Termination

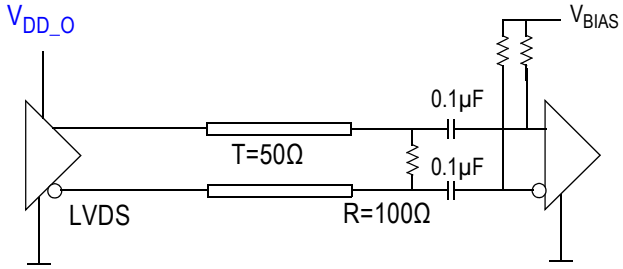
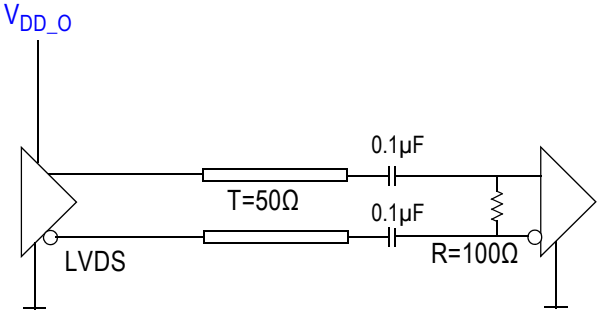


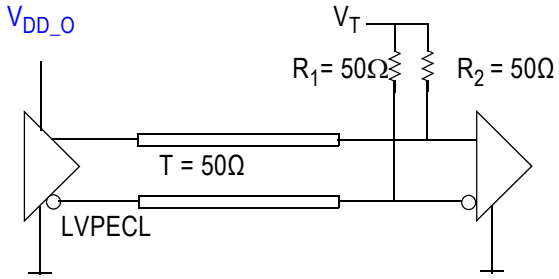
Figure 9. LVDS (STYLE = 0) AC Coupling



Termination for Q, nQ LVPECL Outputs

Figure shows an example termination for the Q, nQ LVPECL outputs. In this example, the characteristic transmission line impedance is 50Ω. The R1 (50Ω) and R2 (50Ω) resistors are matched load terminations. The output is terminated to the termination voltage V_T. V_T must be set according to the output amplitude setting defined in Table 9. The termination resistors must be placed close at the line end.

Figure 10. Output Termination



$V_T = V_{DD\_O}$ - 1.75V (500 mV Amplitude)

$V_T = V_{DD\_O}$ - 2.00V (750mV Amplitude)

Termination for Q, nQ LVPECL Outputs AC-Coupled into HCSL-Receiver

Figure 11. LVPECL Output AC-Coupled into HCSL Receiver

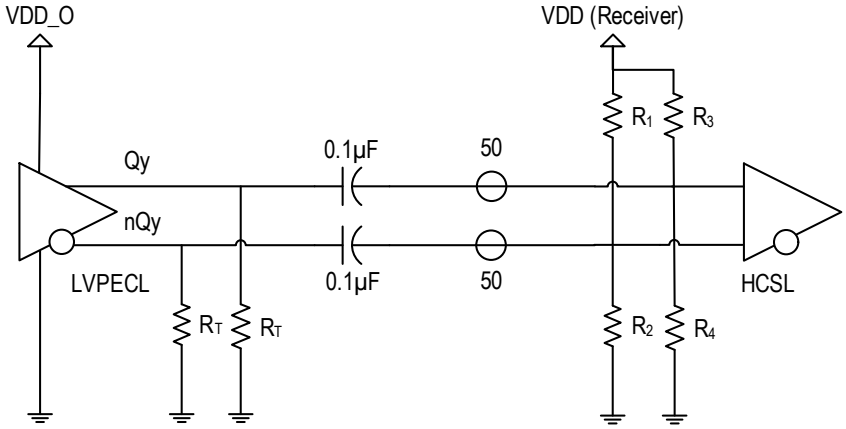


Table 24. Termination Resistors

	V_{DD_O} = 2.5V	V_{DD_O} = 3.3V
R_T	100Ω	180Ω

Table 25. HCSL Receiver Voltage Bias

	V_{DD} = 2.5V	V_{DD} = 3.3V
R_1, R_3	357Ω	470Ω
R_2, R_4	58Ω	56Ω

Input Interface Circuits

Figure 12. LVDS Output Drives 8T79S308 Input (DC-Coupled)

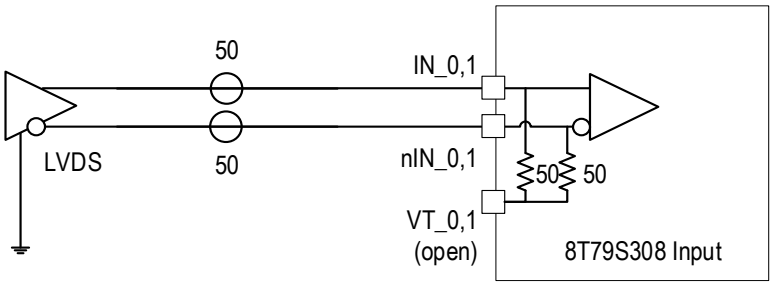
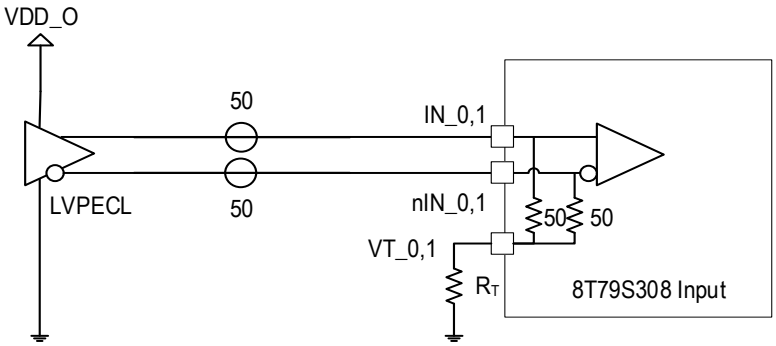
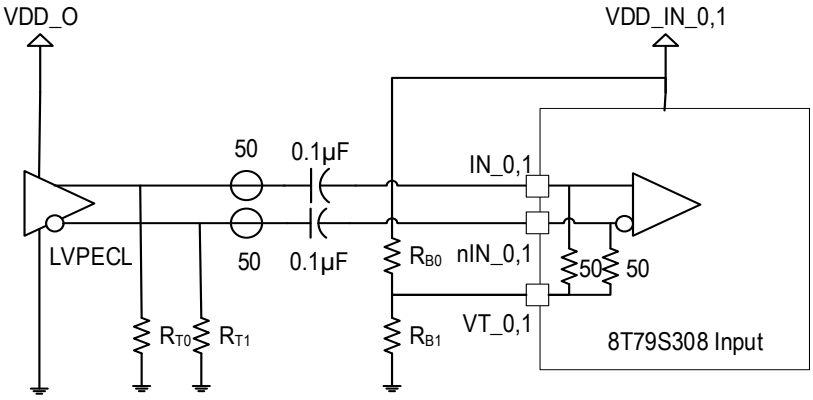


Figure 13. LVPECL Output Drives 8T79S308 Input (DC-Coupled)



	V_{DD_O} = 2.5V	V_{DD_O} = 3.3V
R_T	18Ω	50Ω

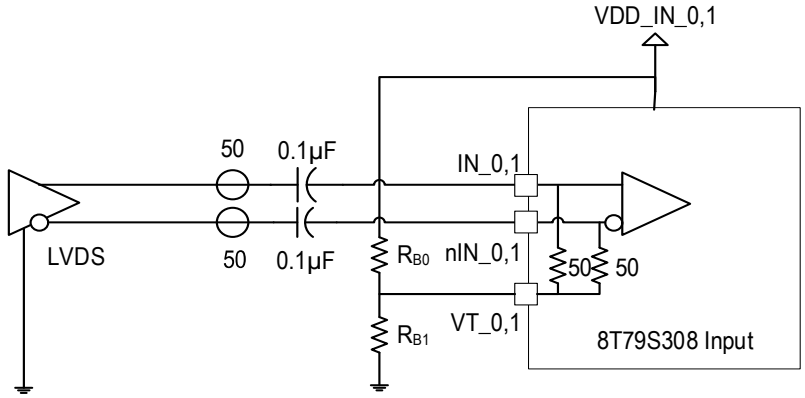
Figure 14. LVPECL Output Drives 8T79S308 Input (AC-Coupled)



	V_{DD_O} = 2.5V	V_{DD_O} = 3.3V
$R_{T0,1}$	56Ω	120–240Ω

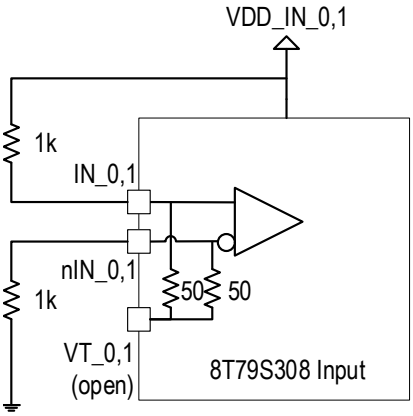
	$V_{DD\_IN0,1}$ = 2.5V	$V_{DD\_IN0,1}$=3.3V
R_{B0}	5.1kΩ	5.1kΩ
R_{B1}	10kΩ	10kΩ

Figure 15. LVDS Output Drives 8T79S308 Input (AC-Coupled)



	$V_{DD\_IN0,1}$ = 2.5V	$V_{DD\_IN0,1}$=3.3V
R_{B0}	5.1kΩ	5.1kΩ
R_{B1}	10kΩ	10kΩ

Figure 16. Unused Input



Thermal Characteristics

Table 26. Thermal Characteristics[a]

Multi-Layer PCB, JEDEC Standard Test Board				
Symbol	Thermal Parameter	Condition	Value	Unit
Θ_{JA}	Junction to ambient	0 m/s air flow	24.6	°C/W
		1 m/s air flow	21.2	
		2 m/s air flow	19.6	
		3 m/s air flow	18.8	
		4 m/s air flow	18.2	
		5 m/s air flow	17.6	
Θ_{JC}	Junction to case	—	21.6	
Θ_{JB}	Junction to board[b]	—	1.2	

[a] Standard JEDEC 2S2P multilayer PCB.

[b] Thermal model where the heat dissipated in the component is conducted through the board. T_B is measured on or near the component lead.

Temperature Considerations

The device supports applications in a natural convection environment as long as the junction temperature does not exceed the specified junction temperature T_J. In applications where the heat dissipates through the PCB, Θ_{JB} is the correct metric to calculate the junction temperature. Θ_{JB} is the right metric in all other applications where the majority of the heat dissipates through the board (80%) and a minority (20%) through the top of the device. The following calculation uses the junction-to-board thermal characterization parameter Θ_{JB} to calculate the junction temperature (T_J). Care must be taken to not exceed the maximum allowed junction temperature T_J of 125 °C.

The junction temperature T_J is calculated using the following equation:

$$T_J = T_B + P_{TOT} \times \Theta_{JB}$$

where:

- T_J is the junction temperature at steady state conditions in °C
- T_B is the board temperature at steady state condition in °C, measured on or near the component lead
- Θ_{JB} is the thermal characterization parameter to report the difference between T_J and T_B
- P_{TOT} is the total device power dissipation

Application power dissipation scenarios: Applications may use device settings that result in a lower power dissipation than the maximum power scenario. The device is a multi-functional, high-speed device that targets a variety of applications. Since this device is highly programmable with a broad range of settings and configurations, the power consumption will vary as settings and configurations are changed. Table 27 and Table 28 show the typical current consumption and total device power consumption along with the junction temperature for the four test cases shown in the tables. The tables also display the maximum board temperature for the Θ_{JB} model.

Table 27. Typical Device Power Dissipation and Junction Temperature, V_{DD_V} = V_{DD_O} = 3.3V

Test Case[a]	Output Configuration	Device		Θ_{JB} Thermal Model	
		I_{DD_TOT}	P_{TOT}	T_J[b]	$T_{B, MAX}$[c]
		mA	W	°C	°C
1	Qn: LVPECL, 500mV	356	0.7174	105.87	124.13
2	Qn: LVPECL, 750mV	406	0.8142	105.98	124.02
3	Qn: LVDS, 350mV	300	0.99	106.19	123.81
4	Qn: LVDS, 500mV	308	1.02	106.23	123.77

[a] See Table 21 and Table 22 for device settings.

[b] Junction temperature at board temperature T_B=105°C.

[c] Maximum board temperature for junction temperature <125°C.

Table 28. Typical Device Power Dissipation and Junction Temperature, V_{DD_V} = V_{DD_O} = 2.5V

Test Case[a]	Output Configuration	Device		Θ_{JB} Thermal Model	
		I_{DD_TOT}	P_{TOT}	T_J[b]	$T_{B, MAX}$[c]
		mA	W	°C	°C
1	Qn: LVPECL, 500mV	346	0.585	105.71	124.29
2	Qn: LVPECL, 750mV	396	0.671	105.81	124.19
3	Qn: LVDS, 350mV	295	0.738	105.89	124.11
4	Qn: LVDS, 750mV	302	0.755	105.91	124.09

[a] See Table 21 and Table 22 for device settings.

[b] Junction temperature at board temperature T_B=105°C.

[c] Maximum board temperature for junction temperature <125°C.

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

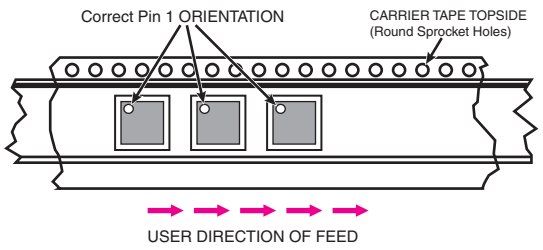
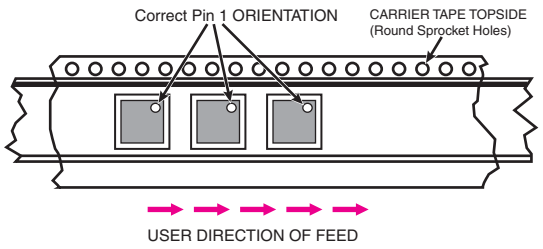
Marking Diagram

1. Lines 1 and 2 indicate the part number.
2. Line 3:
   - "#" denotes stepping.
   - "YY" is the last two digits of the year; "WW" is the work week number that the part was assembled.
   - "$" denotes the mark code.

Ordering Information

Orderable Part Number	Package	Shipping Packaging	Temperature
8T79S308NLGI	RoHS 6/6 40-VFQFPN, 6 × 6 mm	Tray	-40°C to +105°C
8T79S308NLGI8		Tape and Reel, Pin 1 Orientation: EIA-481-C	
8T79S308NLGI/W		Tape and Reel, Pin 1 Orientation: EIA-481-D/E	

Table 29. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D/E)	

Glossary

Abbreviation	Description
Index *n*	Denominates a Q, nQ differential output and associated configuration bits. Range: A0, A1, A2, A4, B0, B1, B2, B3.
V_{DD_V}	Denominates core voltage and input supply pins VDD, VDD_IN_0 and VDD_IN_1. Range: 3.3V, 2.5V.
V_{DD_O}	Denominates output bank voltage pins VDDA and VDDB. Range: 3.3V, 2.5V, 1.8V.
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{…}	List of discrete values.

Revision History

Revision Date	Description of Change
August 10, 2018	▪ Updated the supported frequency range to “0 to 3GHz” in Features ▪ Removed reference to “Design Target Specification” from all electrical characteristics tables ▪ Added a footnote to Figure 4 and Figure 5 ▪ Completed other minor changes throughout
May 31, 2018	Initial release.

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