

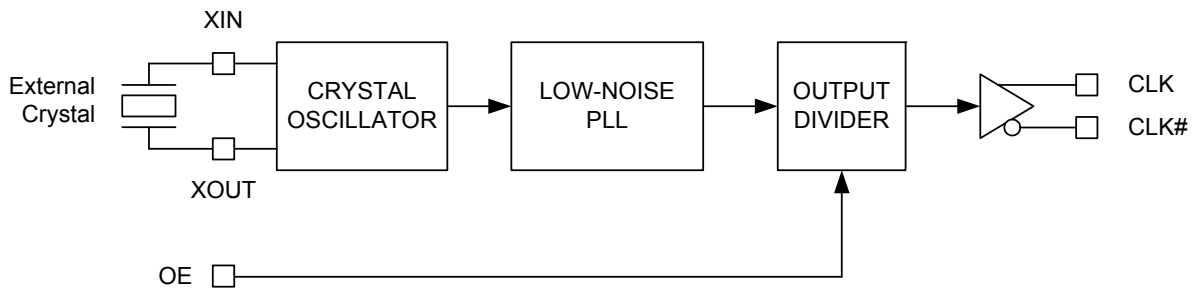
Features

- Output: One low-voltage differential signal (LVDS) output pair
- Output frequency: 125 MHz
- Input: 25-MHz external crystal
- RMS phase jitter:
 - At 125 MHz (12 kHz to 20 MHz offset): 0.65 ps typical
- Package: Pb-free 8-pin thin shrunk small outline package (TSSOP)
- Supply voltage: 3.3 V or 2.5 V
- Temperature range: Commercial or industrial

Functional Description

The CY2XL13 is a phase-locked loop (PLL)-based high-performance clock generator that uses Cypress’s low-noise voltage control oscillator (VCO) technology to achieve less than 1-ps typical RMS phase jitter. The CY2XL13 uses an external crystal reference input to generate one LVDS output pair, which can be asynchronously enabled/disabled with an OE pin. The device operates at 3.3 V or 2.5 V.

Logic Block Diagram

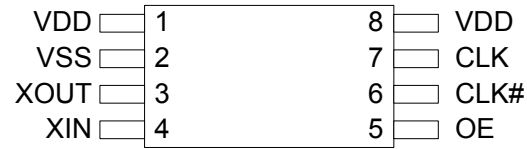


Contents

| | | | |
|--|----------|--|-----------|
| Pinout | 3 | Ordering Information | 10 |
| Pin Definitions | 3 | Ordering Code Definitions | 10 |
| Frequency Table | 3 | Package Drawing and Dimensions | 11 |
| Absolute Maximum Conditions | 4 | Acronyms | 12 |
| Operating Conditions | 4 | Document Conventions | 12 |
| DC Electrical Characteristics | 5 | Units of Measure | 12 |
| AC Electrical Characteristics | 6 | Document History Page | 13 |
| Crystal Characteristics | 6 | Sales, Solutions, and Legal Information | 14 |
| Switching Waveforms | 7 | Worldwide Sales and Design Support | 14 |
| Termination Circuits | 8 | Products | 14 |
| Application Information | 9 | PSoC® Solutions | 14 |
| Power Supply Filtering Techniques | 9 | Cypress Developer Community | 14 |
| Board Layout and OE Pin | 9 | Technical Support | 14 |
| Termination for LVDS Output | 9 | | |
| Crystal Interface | 9 | | |

Pinout

Figure 1. 8-pin TSSOP pinout



Pin Definitions

8-pin TSSOP

| Pin Number | Pin Name | I/O Type | Description |
|------------|-----------|-----------------------|--|
| 1, 8 | VDD | Power | 3.3-V or 2.5-V power supply. All supply current flows through pin 1 |
| 2 | VSS | Power | Ground |
| 3, 4 | XOUT, XIN | XTAL output and input | Parallel resonant crystal interface |
| 5 | OE | CMOS input | Output enable: When high, the output is enabled. When low, the output is high impedance. |
| 6, 7 | CLK#, CLK | LVDS output | Differential clock output |

Frequency Table

| Part Number | Crystal Frequency | Output Frequency | Pin 5 Function | RMS Phase Jitter (Random) | |
|--------------|-------------------|------------------|----------------|---------------------------|------------------|
| | | | | Offset Range | Jitter (Typical) |
| CY2XL13ZXC01 | 25 MHz | 125 MHz | OE | 12 kHz to 20 MHz | 0.65 ps |
| CY2XL13ZXI01 | | | | | |

Absolute Maximum Conditions

| Parameter | Description | Condition | Min | Max | Unit |
|--------------------------------|---|-----------------------------|------|-----------------------|------|
| V _{DD} | Supply voltage | | -0.5 | 4.4 | V |
| V _{IN} ^[1] | Input voltage, DC | Relative to V _{SS} | -0.5 | V _{DD} + 0.5 | V |
| T _S | Temperature, Storage | Non operating | -65 | 150 | °C |
| T _J | Temperature, Junction | | - | 135 | °C |
| ESD _{HBM} | Electrostatic discharge (ESD) protection (human body model) | JEDEC STD 22-A114-B | 2000 | - | V |
| UL-94 | Flammability rating | At 1/8 in. | V-0 | | - |
| Θ _{JA} ^[2] | Thermal resistance, junction to ambient | 0 m/s airflow | 100 | | °C/W |
| | | 1 m/s airflow | 91 | | |
| | | 2.5 m/s airflow | 87 | | |

Operating Conditions

| Parameter | Description | Min | Max | Unit |
|-----------------|---|-------|-------|------|
| V _{DD} | 3.3-V supply voltage | 3.135 | 3.465 | V |
| | 2.5-V supply voltage | 2.375 | 2.625 | V |
| T _A | Ambient temperature, commercial | 0 | 70 | °C |
| | Ambient temperature, industrial | -40 | 85 | °C |
| T _{PU} | Power-up time for all V _{DD} to reach minimum specified voltage (ensure power ramp is monotonic) | 0.05 | 500 | ms |

Notes

1. The voltage on any input or I/O pin cannot exceed the V_{DD} pins during power-up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metallization. No vias are included in the model.

DC Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-----------------------|--|---|---------------------|-----|---------------------|---------------|
| $I_{DD}^{[3]}$ | Power supply current with output terminated | $V_{DD} = 3.465\text{ V}$, $OE = V_{DD}$, output terminated | – | – | 120 | mA |
| | | $V_{DD} = 2.625\text{ V}$, $OE = V_{DD}$, output terminated | – | – | 115 | mA |
| $V_{OD}^{[4]}$ | LVDS differential output voltage | $V_{DD} = 3.3\text{ V}$ or 2.5 V , $R_{TERM} = 100\ \Omega$ between CLK and CLK# | 247 | – | 454 | mV |
| $\Delta V_{OD}^{[4]}$ | Change in V_{OD} between complementary output states | $V_{DD} = 3.3\text{ V}$ or 2.5 V , $R_{TERM} = 100\ \Omega$ between CLK and CLK# | – | – | 50 | mV |
| $V_{OS}^{[5]}$ | LVDS offset output voltage | $V_{DD} = 3.3\text{ V}$ or 2.5 V , $R_{TERM} = 100\ \Omega$ between CLK and CLK# | 1.125 | – | 1.375 | V |
| ΔV_{OS} | Change in V_{OS} between complementary output states | $V_{DD} = 3.3\text{ V}$ or 2.5 V , $R_{TERM} = 100\ \Omega$ between CLK and CLK# | – | – | 50 | mV |
| I_{OZ} | Output leakage current | Three-state output, unterminated, measured on one pin while floating the other pin, $OE = V_{SS}$ | –35 | – | 35 | μA |
| V_{IH} | Input high voltage, pin 5 | | $0.7 \times V_{DD}$ | – | – | V |
| V_{IL} | Input low voltage, pin 5 | | – | – | $0.3 \times V_{DD}$ | V |
| I_{IH} | Input high current, pin 5 | Input = V_{DD} | – | – | 115 | μA |
| I_{IL} | Input low current, pin 5 | Input = V_{SS} | –50 | – | – | μA |
| C_{IN} | Input capacitance, pin 5 | | – | 15 | – | pF |
| C_{INX} | Pin capacitance, XIN and XOUT | | – | 4.5 | – | pF |

Notes

3. I_{DD} includes ~4 mA of current that is dissipated externally in the output termination resistor.
4. Refer to Figure 2 on page 7.
5. Refer to Figure 3 on page 7.

AC Electrical Characteristics

| Parameter ^[6, 7] | Description | Test Conditions | Min | Typ | Max | Unit |
|--|---------------------------|---|------------|-----|-----|------|
| F _{OUT} ^[8] | Output frequency | | See note 8 | | | MHz |
| T _R , T _F ^[9] | Output rise or fall time | 20% to 80% of full output swing | – | 0.5 | 1.0 | ns |
| T _{Jitter(φ)} ^[8, 10] | RMS phase jitter (random) | Offset = 12 kHz to 20 MHz | – | – | 1.0 | ps |
| T _{DC} ^[11] | Duty cycle | Measured at zero crossing point | 45 | – | 55 | % |
| T _{OHZ} ^[12] | Output disable time | Time from falling edge on OE to stopped outputs (asynchronous) | – | – | 100 | ns |
| T _{OE} ^[12] | Output enable time | Time from rising edge on OE to outputs at a valid frequency (asynchronous) | – | – | 120 | ns |
| T _{LOCK} | Startup time | Time for CLK to reach valid frequency measured from the time V _{DD} = V _{DD(min)} . | – | – | 5 | ms |

Crystal Characteristics

| Parameter | Description | Min | Max | Unit |
|------------------|------------------------------|-------------|-----|------|
| MO | Mode of oscillation | Fundamental | | |
| F ^[8] | Frequency | See note 8 | | MHz |
| ESR | Equivalent series resistance | – | 50 | Ω |
| C _S | Shunt capacitance | – | 7 | pF |

Notes

6. Not 100% tested, guaranteed by design and characterization.
7. Outputs are terminated with 100 Ω between CLK and CLK#. Refer to [Figure 8 on page 8](#).
8. Crystal frequency, output frequency, and typical phase jitter are listed in [Frequency Table on page 3](#).
9. Refer to [Figure 4 on page 7](#).
10. Refer to [Figure 7 on page 8](#).
11. Refer to [Figure 5 on page 7](#).
12. Refer to [Figure 6 on page 7](#).

Switching Waveforms

Figure 2. Output Voltage Swing

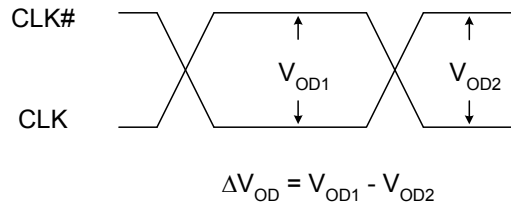


Figure 3. Output Offset Voltage

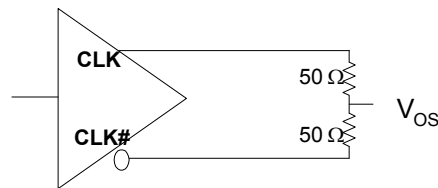


Figure 4. Output Rise or Fall Time

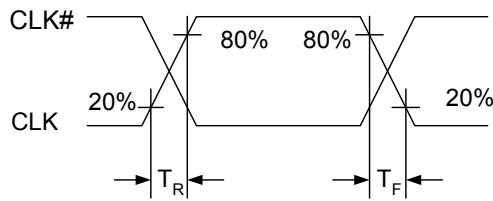


Figure 5. Duty Cycle Timing

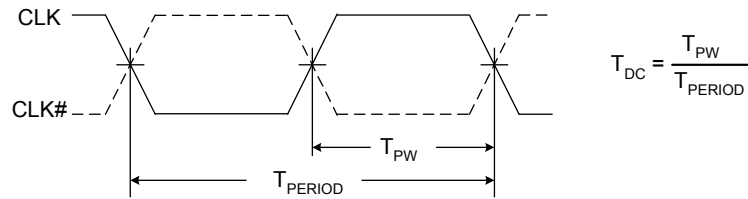
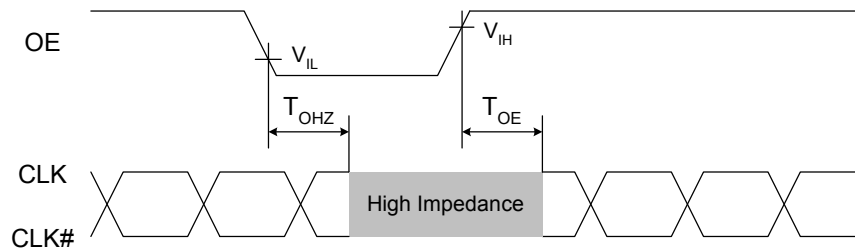
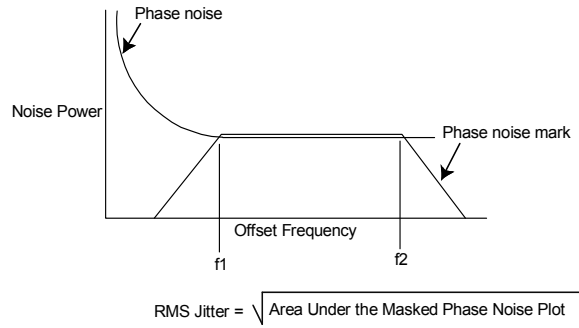


Figure 6. Output Enable and Disable Timing



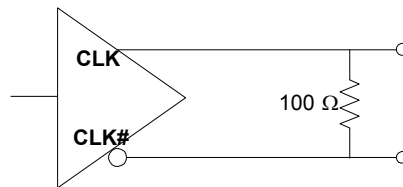
Switching Waveforms (continued)

Figure 7. RMS Phase Jitter



Termination Circuits

Figure 8. LVDS Termination

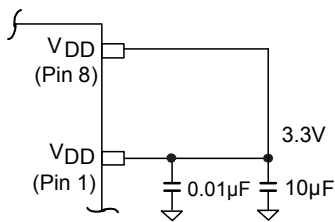


Application Information

Power Supply Filtering Techniques

As in any high-speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power-supply isolation practices. Figure 9 illustrates a typical filtering scheme. Because all the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 μF ceramic chip capacitor is also located close to this pin to provide a short and low-impedance AC path to ground. A 1 to 10 μF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

Figure 9. Power Supply Filtering



Board Layout and OE Pin

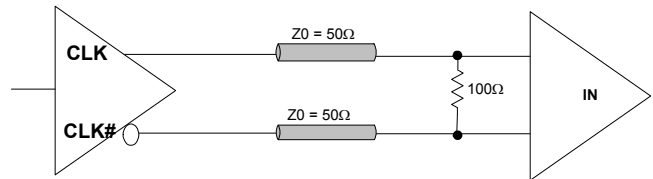
If the Output Enable (OE) function on pin 5 is not needed, it may be connected directly to the V_{DD} plane by a wide trace and multiple vias. This improves heat dissipation. A resistor between OE and V_{DD} is not necessary.

Termination for LVDS Output

The CY2XL13 is designed to drive a standard LVDS load with a 100- Ω termination resistor. Figure 10 shows the standard termination scheme. The termination resistor should always be

located very close to the receiver. To minimize signal reflections from the receiver, the differential impedance (Z_0) of the trace pair should be 100 Ω to match the termination resistor.

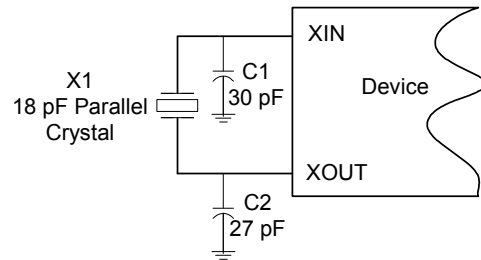
Figure 10. Output Termination



Crystal Interface

The CY2XL13 is characterized with 18 pF parallel resonant crystals. The capacitor values shown in Figure 11 are determined using an 18 pF parallel resonant crystal and are chosen to minimize the ppm error. Note that the optimal values for C1 and C2 depend on the parasitic trace capacitance and are, therefore, layout dependent.

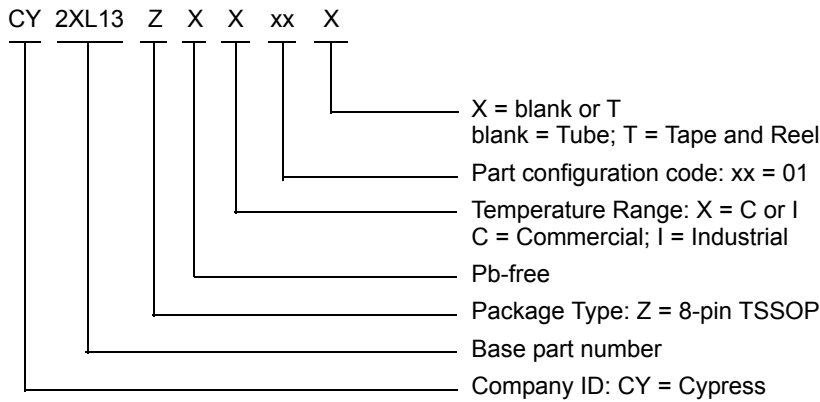
Figure 11. Crystal Input Interface



Ordering Information

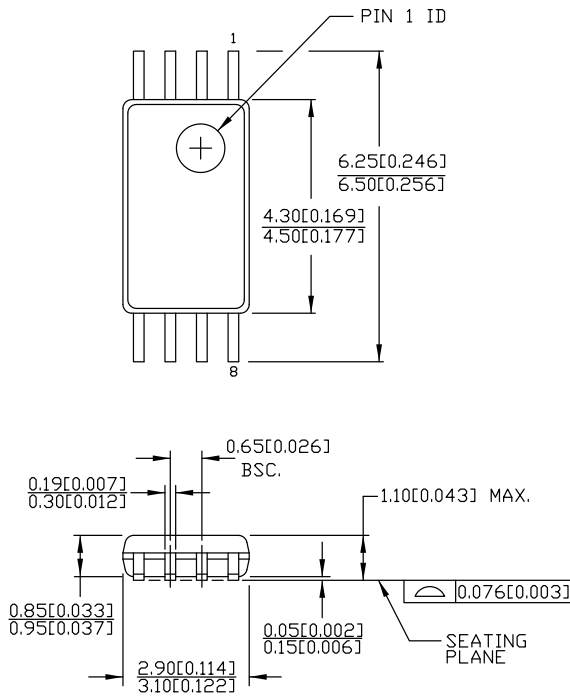
| Part Number | Package Description | Product Flow |
|---------------|-----------------------------|-----------------------------|
| CY2XL13ZXC01 | 8-pin TSSOP | Commercial, 0 °C to 70 °C |
| CY2XL13ZXC01T | 8-pin TSSOP – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY2XL13ZXI01 | 8-pin TSSOP | Industrial, –40 °C to 85 °C |
| CY2XL13ZXI01T | 8-pin TSSOP – Tape and Reel | Industrial, –40 °C to 85 °C |

Ordering Code Definitions



Package Drawing and Dimensions

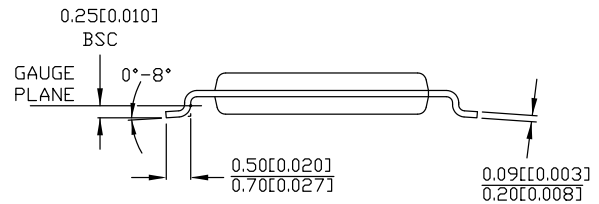
Figure 12. 8-pin TSSOP (4.40 mm Body) Z08.173/ZZ08.173 Package Outline, 51-85093



DIMENSIONS IN MM[INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

| PART # | |
|----------|----------------|
| Z08.173 | STANDARD PKG. |
| ZZ08.173 | LEAD FREE PKG. |



51-85093 *D

Acronyms

| Acronym | Description |
|---------|--|
| ESD | Electrostatic Discharge |
| FAE | Field Application Engineer |
| HBM | Human Body Model |
| JEDEC | Joint Electron Devices Engineering Council |
| LCC | Leadless Chip Carrier |
| LVDS | Low-Voltage Differential Signaling |
| OE | Output Enable |
| PCB | Printed Circuit Board |
| PLL | Phase-Locked Loop |
| RMS | Root Mean Square |
| TSSOP | Thin Shrunk Small Outline Package |
| VCO | Voltage Controlled Oscillator |
| XO | Crystal Oscillator |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY2XL13, Low-Noise LVDS Clock Generator Document Number: 001-63177 | | | | |
|---|---------|-----------------|-----------------|--|
| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
| ** | 2991849 | 07/23/2010 | KVM | New data sheet. |
| *A | 4118896 | 09/10/2013 | CINM | Updated Package Drawing and Dimensions : spec 51-85093 – Changed revision from *C to *D. Updated in new template. Completing Sunset Review. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC[®] Solutions

[psoc.cypress.com/solutions](#)
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2010-2013. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.