

USER CONFIGURABLE DIVIDER

ICS674-01

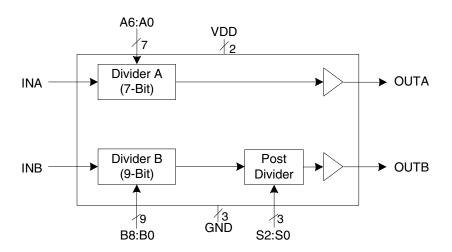
Description

The ICS674-01 consists of two separate configurable dividers. The A Divider is a 7-bit divider and can divide by 3 to 129. The B Divider consists of a 9-bit divider followed by a post divider. The 9-bit divider can divide by 12 to 519. The post divider has eight settings of 1, 2, 4, 5, 6, 7, 8, and 10; giving a maximum total divide of 5190. The A and B Dividers can be cascaded to give a maximum divide of 669510. The ICS674-01 supports the ICS673 PLL Building Block and enables the user to build a full custom PLL synthesizer.

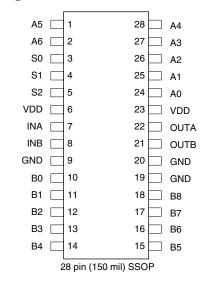
Features

- Packaged in 28-pin SSOP (150 mil body)
- Pb (lead) free package, RoHS compliant
- General purpose programmable divider
- Supports ICS673 PLL Building Block
- User determines the divide by setting input pins
- Pull-ups on all select inputs
- Includes one 7-bit Divider for OUTA
- Includes one 9-bit Divider and one selectable Post Divider for OUTB
- Industrial temperature range available
- 25 mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltage of 3.3 V or 5 V

Block Diagram



Pin Assignment



Post Divider Table

S2 Pin 5	S1 Pin 4	S0 Pin 3	Post Divide
0	0	0	10
0	0	1	2
0	1	0	8
0	1	1	4
1	0	0	5
1	0	1	7
1	1	0	1
1	1	1	6

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1, 2, 24 - 28	A5, A6, A0-A4	Input	Divider A word input pins. Forms a number from 1 to 127. Internal pull-up resistors. See page 3 for details.
3 - 5	S0, S1, S2	Input	Select pins for Post Divider. See table above. Internal pull-up resistors.
6, 23	VDD	Power	Connect to VDD.
7	INA	Input	Divider A input.
8	INB	Input	Divider B input.
9, 19 - 20	GND	Power	Connect to ground.
10 - 18	B0 - B8	Input	Divider B word input pins. Forms a number from 4 to 511. Internal pull-up resistors. See page 3 for details.
21	OUTB	Output	Divider B output.
22	OUTA	Output	Divider A output.

External Components

The ICS674-01 requires a minimum number of external components for proper operation. A $0.01\mu F$ decoupling capacitor should be connected between each VDD and GND as close to the device as possible. A series termination resistor of 33Ω should be used in series with OUTA and OUTB pins.

Determining (setting) the Divider

The user has full control in setting the desired divide. The user should connect the appropriate divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout, ensuring that the ICS674-01 will automatically produce the correct divide when all components are soldered. It is also possible to connect the inputs to parallel I/O ports in order to change divides. The divides of the ICS674-01 can be determined by the following equations:

Divide A = DAW + 2

Where Divider A Word (DAW) = 1 to 127 (0 is not permitted)

Divide $B = (DBW+8) \times PD$

Where Divider B Word (DBW) = 4 to 511 (0, 1, 2, 3 are not permitted)

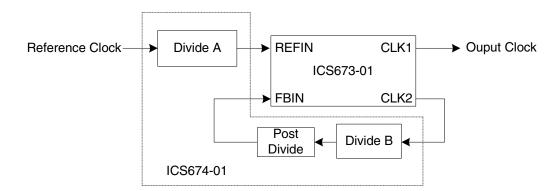
Post Divider (PD) = values on page 2

For example, suppose Divide A is desired to be 61 and Divide B is desired to be 284, then DAW = 59, DBW = 276, and PD = 1. This means A6:A0 is 0111011, B8:B0 is 100010100 and S2:S0 is 110. Since all inputs have pull-ups, it is only necessary to ground the zero pins, namely A6, A2, B7, B6, B5, B1, B0, and S0.

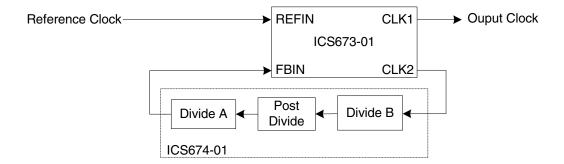
These configuration pins can be changed at any time during operation.

Using the ICS674-01 with the ICS673-01:

The ICS674-01 may be used with the ICS673-01 to build a frequency synthesizer. The following example shows a typical application when the reference clock is in the MHz range:



If the reference is in the kHz range, for example 8 kHz, the following configuration may be more typical:



Note that in both examples, Divide B is connected to the output of the ICS673. This is because Divide B has a higher operating frequency than Divide A.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS674-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
CLKIN and FBIN inputs	-0.5 V to 5.5 V
Electrostatic Discharge	2000 V
Ambient Operating Temperature	0 to +70° C
Ambient Operating Temperature (I version)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Тур.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=5 V ±10%, Ambient temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V _{IH}	All A, B, and S pins	2			V
Input Low Voltage	V _{IL}	All A, B, and S pins			0.8	V
Input High Voltage	V _{IH}	INA and INB only	(VDD/2)+1	VDD/2		V
Input Low Voltage	V _{IL}	INA and INB only		VDD/2	(VDD/2)-1	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.4	V
Operating Supply Current	IDD	No load, f _{in} =100 MHz 3.3 V		3		mA
DivA=DivB=20		No load, f _{in} =100 MHz 5 V		5		mA

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Short Circuit Current	Ios	Each output		±70		mA
On-Chip Pull-up Resistor	R _{PU}	A, B, S select pins		270		kΩ
Input Capacitance	C _{IN}	A, B, S select pins		5		pF

AC Electrical Characteristics

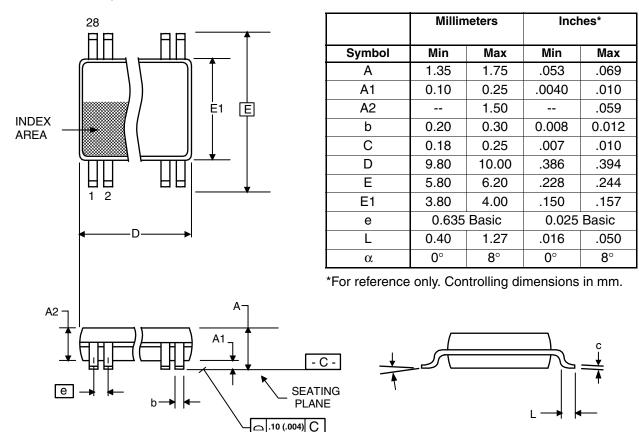
VDD = 5 V, Ambient Temperature -40 to +85 $^{\circ}$ C, C_{LOAD} at CLK = 15 pF, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Input Frequency, Divider A	f _{IN}	3.3 V	0		135	MHz
Input Frequency, Divider B		3.3 V	0		180	MHz
Input Frequency, Divider A		5 V	0		200	MHz
Input Frequency, Divider B		5 V	0		235	MHz
Input Frequency, Divider A (Industrial temperature)	f _{IN}	at 3.3 V, +85° C	0		125	MHz
Input Frequency, Divider B (Industrial temperature)		at 3.3 V, +85° C	0		170	MHz
Input Frequency, Divider A (Industrial temperature)		at 5 V, +85° C	0		190	MHz
Input Frequency, Divider B (Industrial temperature)		at 5 V, +85° C	0		220	MHz
Output Rise Time	t _{OR}	20% to 80%		1.5		ns
Output Fall Time	t _{OF}	80% to 20%		1.5		ns
OUTB Clock Duty Cycle ¹	t _{DC}	at VDD/2	45	49 to 51	55	%
OUTB Clock Duty Cycle odd post dividers		at VDD/2, except PD=1	40		60	%
OUTA Clock Duty Cycle ¹		at VDD/2	20		98.5	%
Peak-to-Peak Jitter		15 pF			400	ps
Cycle-to-Cycle Jitter		30 pF loads			300	ps
Propagation Delay,	T _{PA}	VDD = 3.3 V, +25° C		6.5		ns
Divider A		VDD = 5.0 V, +25° C		4.5		ns
Propagation Delay,	T _{PB}	VDD = 3.3 V, +25° C		20		ns
Divider B + Post Divider		VDD = 5.0 V, +25° C		13		ns

¹ The duty cycle of OUTA is dependent on the selected divide. This because OUTA goes low for 1 input clock cycles on INA. For example, if a divide of 20 is selected, the duty cycle will be 90%. Simlarly, if PD=1 is selected for OUTB, the duty cycle will be dependent on the selected divide. In this case, OUTB goes high for approximately 8 input clock cycles on INB.

Package Outline and Package Dimensions (28-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
674R-01LF	674R-01LF	Tubes	28-pin SSOP	0 to +70° C
674R-01LFT	674R-01LF	Tape and Reel	28-pin SSOP	0 to +70° C
674R-01ILF	674R-01ILF	Tubes	28-pin SSOP	-40 to 85° C
674R-01ILFT	674R-01ILF	Tape and Reel	28-pin SSOP	-40 to 85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high-reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

CLOCK DIVIDER

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.