

## Features

- 36MHz, general purpose PLL
- $4F_{SC}$  based timing (use the EL4585 for  $8F_{SC}$ )
- Compatible w/EL4583 Sync Separator
- VCXO, Xtal, or LC tank oscillator
- <2ns jitter (VCXO)
- User controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed TV scan rate clock divisors
- Selectable external divide for custom ratios
- Single 5V, low current operation

## Applications

- Pixel Clock regeneration
- Video compression engine (MPEG) clock generator
- Video capture or digitization
- PIP (Picture in Picture) timing generator
- Text or graphics overlay timing
- HDTV Low Jitter  $F_{SC}$

## Ordering Information [1]

Part No.	Package	Tape & Reel	Outline #
EL4584CN	PDIP-16	-	MDP0031
EL4584CS	SO-16	-	MDP0027
EL4584CS-T7	SO-16	7 in	MDP0027
EL4584CS-T13	SO-16	13 in	MDP0027

1. For  $6F_{SC}$  and  $8F_{SC}$  clock frequencies, see EL4585 datasheet.

## Demo Board

A demo PCB is available for this product. Request "EL4584C/5C Demo Board".

## General Description

The EL4584C is a PLL (Phase Lock Loop) sub system, designed for video applications but also suitable for general purpose use up to 36MHz. In a video application this device generates a TTL/CMOS compatible Pixel Clock (Clk Out) which is a multiple of the TV Horizontal scan rate, and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications where periodic disturbances are present in the reference video timing such as VCR head switching. The Lock detector output indicates correct lock.

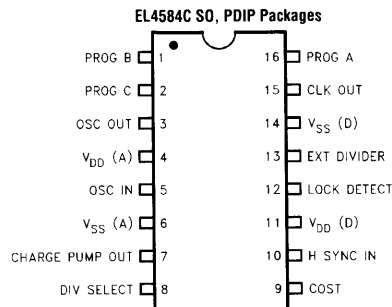
The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including  $4F_{SC}$ ,  $3F_{SC}$ , 13.5MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate  $8F_{SC}$ ,  $6F_{SC}$ , 27MHz (CCIR 601 format) etc. use the EL4585, which includes an additional divide by 2 stage.

For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be bypassed and an external divider chain used.

FREQUENCIES and DIVISORS				
Function	$3F_{SC}$ [1]	CCIR 601 [2]	Square [3]	$4F_{SC}$
Divisor	851	864	944	1135
PAL Fosc (MHz)	13.301	13.5	14.75	17.73
Divisor	682	858	780	910
NTSC Fosc (MHz)	10.738	13.5	12.273	14.318

1.  $3F_{SC}$  numbers do not yield integer divisors.
2. CCIR 601 Divisors yield 720 pixels in the portion of each line for NTSC and PAL.
3. Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL in the active portion.

## Connection Diagrams



**EL4584C****Horizontal Genlock, 4 FSC****Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

$V_{CC}$ Supply	7V	Lead Temperature	260°C
Operating Junction Temp	125°C	Oscillator Frequency	36MHz
Storage Temperature	-65°C to +150°C	Pin Voltages	-0.5V to $V_{CC}+0.5V$
Power Dissipation	400mW	Operating Ambient Temperature Range	-40°C to +85°C

**Important Note:**

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**DC Electrical Characteristics**

( $V_{DD} = 5V$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Units
$I_{DD}$	$V_{DD} = 5V$ <sup>[1]</sup>	25°C		2	4	mA
$V_{IL}$ Input Low Voltage		25°C			1.5	V
$V_{IH}$ Input High Voltage		25°C	3.5			V
$I_{IL}$ Input Low Current	All inputs except COAST, $V_{IN} = 1.5V$	25°C	-100			nA
$I_{IH}$ Input High Current	All inputs except COAST, $V_{IN} = 3.5V$	25°C			100	nA
$I_{IL}$ Input Low Current	COAST pin, $V_{IN} = 1.5V$	25°C	-100	-60		μA
$I_{IH}$ Input High Current	COAST pin, $V_{IN} = 3.5V$	25°C		60	100	μA
$V_{OL}$ Output Low Voltage	Lock Det, $I_{OL} = 1.6mA$	25°C			0.4	V
$V_{OH}$ Output High Voltage	Lock Det, $I_{OH} = -1.6mA$	25°C	2.4			V
$V_{OL}$ Output Low Voltage	CLK, $I_{OL} = 3.2mA$	25°C			0.4	V
$V_{OH}$ Output High Voltage	CLK, $I_{OH} = -3.2mA$	25°C	2.4			V
$V_{OL}$ Output Low Voltage	OSC Out, $I_{OL} = 200\mu A$	25°C			0.4	V
$V_{OH}$ Output High Voltage	OSC Out, $I_{OH} = -200\mu A$	25°C	2.4			V
$I_{OL}$ Output Low Current	Filter Out, $V_{OUT} = 2.5V$	25°C	200	300		μA
$I_{OH}$ Output High Current	Filter Out, $V_{OUT} = 2.5V$	25°C		-300	-200	μA
$I_{OL}/I_{OH}$ Current Ratio	Filter Out, $V_{OUT} = 2.5V$	25°C	1.05	1.0	0.95	
$I_{LEAK}$ Filter Out	Coast Mode, $V_{DD} > V_{OUT} > 0V$	25°C	-100	±1	100	nA

1. All inputs to 0V, COAST floating.

## AC Electrical Characteristics

( $V_{DD} = 5V$ ,  $T_A = 25^\circ C$  unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Units
VCO Gain @ 20MHz	Test Circuit 1	25°C		15.5		dB
H-sync S/N Ratio	$V_{DD} = 5V$ <sup>[1]</sup>	25°C	35			dB
Jitter	VCXO Oscillator	25°C		1		ns
Jitter	LC Oscillator (Typ)	25°C		10		ns

1. Noisy video signal input to EL4583C, H-Sync input to EL4584C. Test for positive signal lock.

## Pin Description

Pin No.	Pin Name	Function
16,1,2	Prog A,B,C	Digital inputs to select ÷ N value for internal counter. See table below for values.
3	Osc/VCO Out	Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.
4	$V_{DD}$ (A)	Analog positive supply for oscillator, PLL circuits.
5	Osc/VCO In	Input from external VCO.
6	$V_{SS}$ (A)	Analog ground for oscillator, PLL circuits.
7	Charge Pump Out	Connect to loop filter. If the H-sync phase is leading or H-sync frequency > CLK÷N, current is pumped into the filter capacitor to increase VCO frequency. If H-sync phase is lagging or frequency < CLK÷N, current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, charge pump goes to a high impedance state.
8	Div Select	Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting CLK ÷ N. When low, the internal divider is disabled and EXT DIV is an input from an external ÷ N.
9	Coast	Tri-state logic input. Low (<1/3* $V_{CC}$ ) = normal mode, Hi Z (or 1/3 to 2/3* $V_{CC}$ ) = fast lock mode, High (>2/3* $V_{CC}$ ) = coast mode.
10	H-sync In	Horizontal sync pulse (CMOS level) input.
11	$V_{DD}$ (D)	Positive supply for digital, I/O circuits.
12	Lock Det	Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.
13	Ext Div	External Divide input when DIV SEL is low, internal ÷ N output when DIV SEL is high.
14	$V_{SS}$ (D)	Ground for digital, I/O circuits.
15	CLK Out	Buffered output of the VCO.

VCO Divisors Table 1

Prog A Pin 16	Prog B Pin 1	Prog C Pin 2	Div Value N
0	0	0	851
0	0	1	864
0	1	0	944
0	1	1	1135
1	0	0	682
1	0	1	858
1	1	0	780
1	1	1	910

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Horizontal Genlock, 4 FSC

## Timing Diagrams

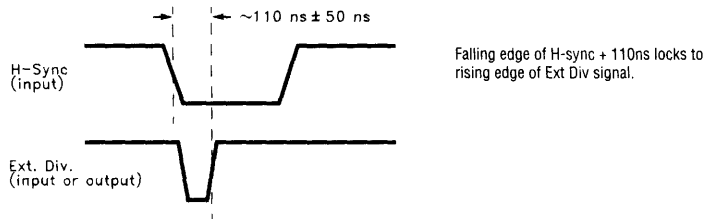


Figure 1. PLL Locked Condition (Phase Error = 0)

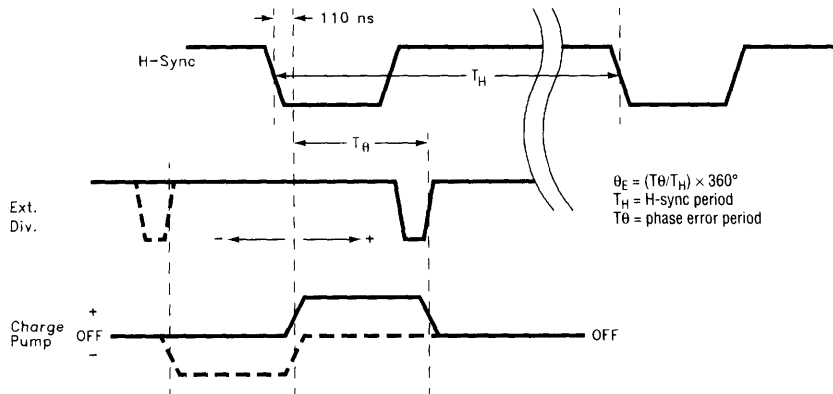


Figure 2. Out of Lock Condition

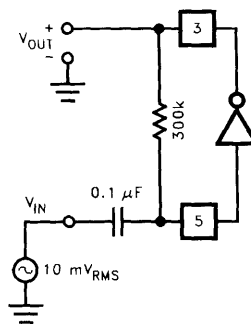
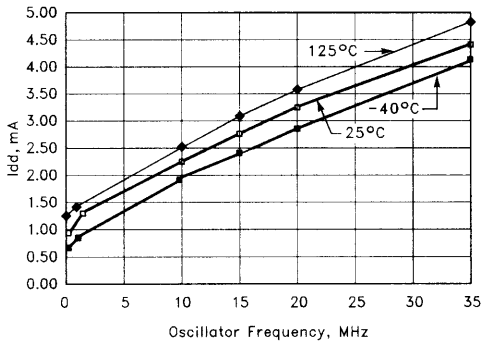


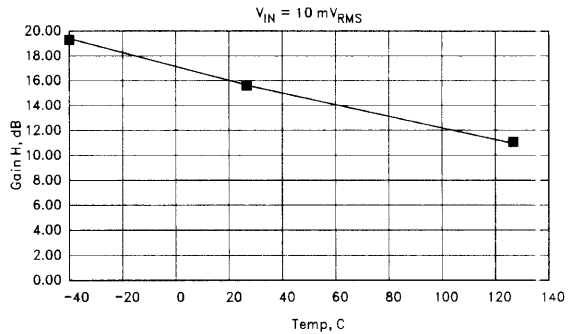
Figure 3. Test Circuit 1

## Typical Performance Curves

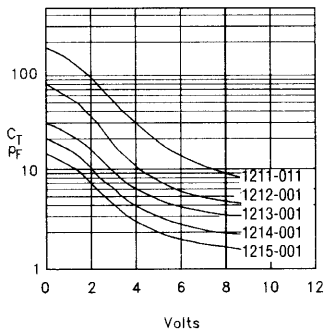
I<sub>dd</sub> vs F<sub>osc</sub>



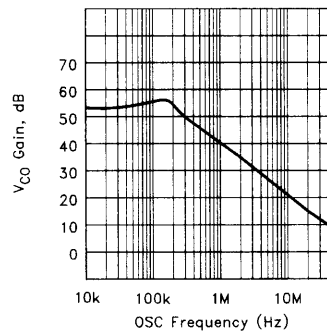
4584 OSC Gain @ 20 MHz vs Temp



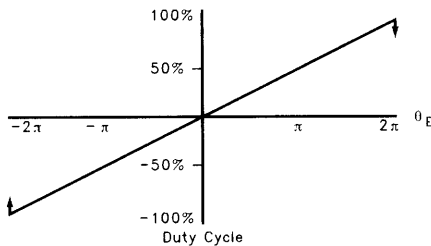
Typical Varactor



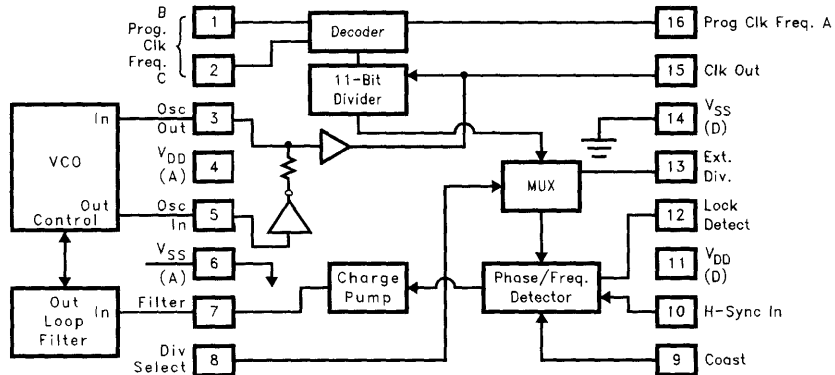
OSC Gain vs Fosc



Charge Pump Duty Cycle vs  $\theta_E$



Video

**EL4584C***Horizontal Genlock, 4 FSC***Block Diagram**

## Description Of Operation

The horizontal sync signal (CMOS level, falling leading edge) is input to H-sync input (pin 10). This signal is delayed about 110ns, the falling edge of which becomes the reference to which the clock output will be locked. (See timing diagrams.) The clock is generated by the signal on pin 5, OSC in. There are 2 general types of VCO that can be used with the EL4584C, LC and crystal controlled. Additionally, each type can be either built up using discrete components, including a varactor as the frequency controlling element, or complete, self contained modules can be purchased with everything inside a metal can. The modules are very forgiving of PCB layout, but cost more than discrete solutions. The VCO or VCXO is used to generate the clock. An LC tank resonator has greater "pull" than a crystal controlled circuit, but will also be more likely to drift over time, and thus will generate more jitter. The "pullability" of the circuit refers to the ability to "pull" the frequency of oscillation away from its center frequency by modulating the voltage on the control pin of a VCO module or varactor, and is a function of the slope and range of the capacitance-voltage curve of the varactor or VCO module used. The VCO signal is sent to a divide by N counter, and to the CLK out pin. The divisor N is determined by the state of pins 1, 2, and 16 and is described in table 1 above. The divided signal is sent, along with the delayed Hsync input, to the phase/frequency detector, which compares the two signals for phase and frequency differences. Any phase difference is converted to a current at the charge pump output FILTER (pin 7). A VCO with positive frequency deviation with control voltage must be used. Varactors have negative capacitance slope with voltage, resulting in positive frequency deviation with control voltage for the oscillators in Figure 4 and Figure 5 below.

### VCO

The VCO should be tuned so its frequency of oscillation is very close to the required clock output frequency when the voltage on the varactor is 2.5 volts. VCXO and VCO modules are already tuned to the desired frequency, so this step is not necessary if using one of these units. The range of the charge pump output (pin 7) is 0 to 5 volts and it can source or sink a maximum of about 300 $\mu$ A, so all frequency control must be accomplished with variable capacitance from the varactor within this

range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the h-sync signal experiences frequency variations of greater than about 300ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H-SYNC input frequency is greater than CLK frequency  $\div$  N, charge pump output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, which lowers its capacitance, thus tending to increase VCO frequency. Conversely, filter output pulls current from the filter capacitor when H-SYNC frequency is less than CLK  $\div$  N, forcing the VCO frequency lower. An external VCXO may be used to drive Osc In pin 5 where the rising edge will trigger the counter and have a delay of about 27ns to the falling edge of the Ext Div pin 13 output. This delay is effected by the capacitance on Pin 3 so it should have no connection to it. An external VCXO should have 30nA or less leakage on it's frequency control input to prevent excess phase delay so the lock detect output can function.

### Loop Filter

The loop filter controls how fast the VCO will respond to a change in filter output stimulus. Its components may be chosen so that fast lock can be achieved, yet with a minimum of VCO "hunting", preferably in one to two oscillations of charge pump output, assuming the VCO frequency starts within capture range. If the filter is under-damped, the VCO will over and under-shoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can't respond fast enough to perturbations in VCO frequency. A severely over damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and

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error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviation from these values is not out of the ordinary.

### External Divide

DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

### Normal Mode

Normal mode is enabled by pulling COAST (pin 9) low (below  $1/3 * V_{CC}$ ). If H-sync and  $CLK \div N$  have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of  $CLK \div N$  exactly match the H-sync input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the H-sync input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low.

### Fast Lock Mode

Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between  $1/3$  and  $2/3 * V_{CC}$ ). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a "fast" lock of the signals.

Forcing the clock to be synchronized to the H-sync input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, charge pump output should be very close to its lock-on value and plac-

ing the device into normal mode should result in a normal lock very quickly. Fast Lock mode is intended to be used where H-sync becomes irregular, until a stable signal is again obtained.

### Coast Mode

Coast mode is enabled by pulling COAST (pin 9) high (above  $2/3 * V_{CC}$ ). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant as possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

### Lock Detect

Lock detect (pin 12) will go low when lock is established. Any DC current path from charge pump out will skew EXT DIV relative to HSYNC in, tending to offset or add to the 110ns internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If the part stabilizes in a locked mode, and lock detect is not low, is an indication that there is excess leakage to the charge pump line. This may be caused by leakage on the board which should be less than 30nA. Some digital type boards may exceed this amount of leakage so clean boards must be used. When an external VCO or VCXO are used the frequency control voltage input may have excessive leakage so they should be selected to have less than 30nA bias current. This leakage can not be compensated as it is undefined in value and may have a tempco. A low bias current amp (low BW) may be used to buffer an external VCO or VCXO if needed. When the EL4584C/5C oscillator is used then adjusting C1 will set the phase delay and the nominal charge pump control voltage to 2.5V. The goal is to put the rising edge of EXT DIV in sync with the falling edge of H-SYNC + 110ns. (See timing diagrams. Phase error is positive when EXT DIV lags HSYNC.)



## Applications Information

### Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 14.31818MHz, with an H-sync frequency of 15.734kHz.
2. Choose a reasonable inductor value (10–20μH works well). We choose 15μH.
3. Calculate  $C_T$  needed to produce  $F_{OSC}$ :

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{1}{4\pi^2 F^2 L} = \frac{1}{4\pi^2 (14.318e6)^2 (15e-6)} = 8.2pF$$

4. From the varactor data sheet find  $C_V$  @ 2.5V, the desired lock voltage.  $C_V=23$  pF for our SMV1204-12, for example.
5.  $C_2$  should be about  $10C_V$ , so we choose  $C_2=220$  pF for our example.
6. Calculate  $C_1$ . Since

$$C_T = \frac{C_1 C_2 C_V}{(C_1 C_2) + (C_1 C_V) + (C_2 C_V)}$$

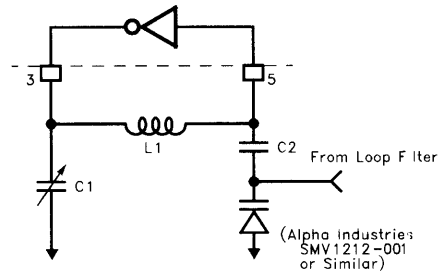
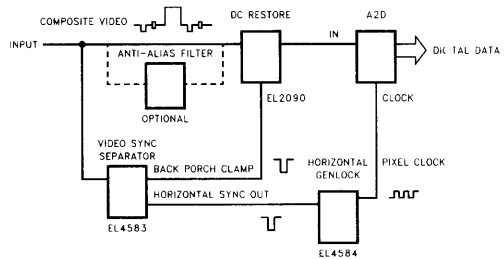
then

$$C_1 = \frac{C_2 C_T C_V}{(C_2 C_V) - (C_2 C_T) - (C_T C_V)}$$

For our example,  $C_1=14pF$ . (A trim cap may be used for fine tuning.) Examples for each frequency using the internal divider follow.

### Typical Application

Horizontal genlock provides clock for an analog to digital converter, digitizing analog video.



**Figure 4. Typical LC VCO**

**LC VCO Component Values (Approximate) [1]**

Frequency (MHz)	L1 (μH)	C1 (pF)	C2 (pF)
13.301	15	18	220
13.5	15	17	220
14.75	12	18	220
17.734	12	10	220
10.738	22	20	220
12.273	18	17	220
14.318	15	14	220

1. Use shielded inductors for optimum performance.

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Horizontal Genlock, 4 FSC

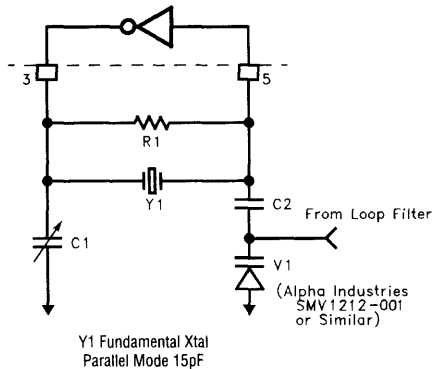


Figure 5. Typical Xtal VCO

**Xtal VCO Component Values (Approximate)**

Frequency (MHz)	R1 (kΩ)	C1 (pF)	C2 (μF)
13.301	300	15	.001
13.5	300	15	.001
14.75	300	15	.001
17.734	300	15	.001
10.738	300	15	.001
12.273	300	15	.001
14.318	300	15	.001

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

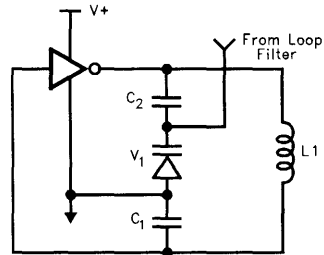


Figure 6. Colpitts Oscillator

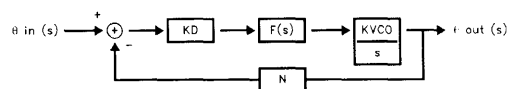
C<sub>1</sub> is to adjust the center frequency, C<sub>2</sub> DC isolates the control from the oscillator, and V<sub>1</sub> is the primary control device. C<sub>2</sub> should be much larger than C<sub>V</sub> so that V<sub>1</sub> has maximum modulation capability. The frequency of oscillation is given by:

$$F = \frac{1}{12\pi\sqrt{LC_T}}$$

$$C_T = \frac{C_1 C_2 C_V}{(C_1 C_2) + (C_1 C_V) + (C_2 C_V)}$$

### Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:



Where:

- K<sub>d</sub>=phase detector gain in A/rad
- F(s)=loop filter impedance in V/A
- K<sub>VCO</sub>=VCO gain in rad/s/V
- N=internal or external divisor

It can be shown that for the loop filter shown below:

$$C_3 = \frac{K_d K_{VCO}}{N \omega_n^2}, C_4 = \frac{C_3}{10}, R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}}$$

Where ω<sub>n</sub> = loop filter bandwidth, and ζ = loop filter damping factor.

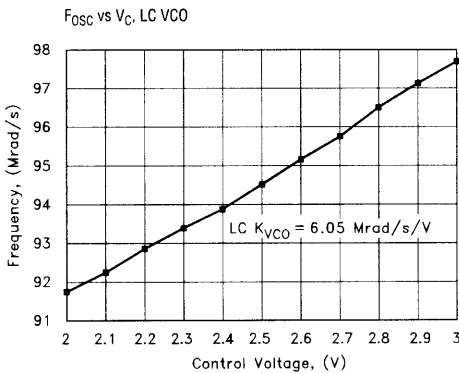
1. K<sub>d</sub> = 300μA/2πrad = 4.77e-5A/rad for the EL4584C.

2. The loop bandwidth should be about H-sync frequency/20, and the damping ratio should be 1 for optimum performance. For our example,  
 $\omega_n = 15.734\text{kHz}/20 = 787\text{Hz} \approx 5000 \text{ rad/S.}$

3.  $N=910$  from table 1.

$$N = \frac{\text{VCOfrequency}}{\text{H-SYNCfrequency}} = \frac{14.31818\text{M}}{15.73426\text{k}} = 910$$

4.  $K_{VCO}$  represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably isn't) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor transfer function  $C_v=F(V_C)$ , where  $V_C$  is the reverse bias control voltage, and  $C_V$  is varactor capacitance. Since  $F(V_C)$  is nonlinear, it is probably best to build the VCO and measure  $K_{VCO}$  about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals  $K_{VCO}$ . For our example,  
 $K_{VCO} = 6.05\text{Mrad/S/V.}$



5. Now we can solve for  $C_3$ ,  $C_4$ , and  $R_3$ .

$$C_3 = \frac{K_d K_{VCO}}{N \omega_n^2} = \frac{(4.77e-5)(6.05e6)}{(910)(5000)^2} = 0.01 \mu\text{F}$$

$$C_4 = \frac{C_3}{10} = 0.0001 \mu\text{F}$$

$$R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} = \frac{(2)(910)(1)(5000)}{(4.77e-5)(6.05e6)} = 31.5\text{k}\Omega$$

We choose  $R_3 = 30\text{k}\Omega$  for convenience.

6. Notice  $R_2$  has little effect on the loop filter design.  $R_2$  should be large, around 100k, and is used to isolate the loop filter from the varactor.  $R_3$  may be reduced or eliminated if VCXO is used.  $C_1$  in the crystal oscillator is set for LDET to be low at lock,  $|T\theta| < 50\text{ns}$ .  $C_4$  is used mainly to attenuate high frequency noise from the charge pump.
7. Sample is for  $LC_{VCO}$ .  $K_{VCO}$  for  $X_{VCO}$  will be much smaller.

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## Horizontal Genlock, 4 FSC

### Lock Time

Let  $\tau = R_3 C_3$ . As  $T$  increases, damping increases, but so does lock time. Decreasing  $T$  decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping ( $\zeta=1$ ) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly overdamped ( $\zeta>1$ ), trading lock time for increased stability.

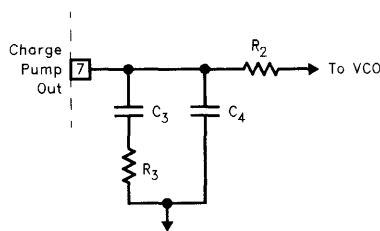


Figure 7. Typical Loop Filter

#### LC Loop Filter Components (Approximate)

Frequency (MHz)	R2 (k $\Omega$ )	R3 (k $\Omega$ )	C3 ( $\mu$ F)	C4 ( $\mu$ F)
13.301	100	30	0.01	0.001
13.5	100	30	0.01	0.001
14.75	100	33	0.01	0.001
17.734	100	39	0.01	0.001
10.738	100	22	0.01	0.001
12.273	100	27	0.01	0.001
14.318	100	30	0.01	0.001

#### Xtal Loop Filter Components (Approximate), R2 = 100k $\Omega$

Jitter (ns)	Lock Time (ms)	R3 (M $\Omega$ )	C3 (pF)	C4 (pF)
13.301 $\pm$ 6	<20	4.3	68	6.8
13.5 $\pm$ 1	<55	4.3	6800	680
14.75 $\pm$ .25	<305	9k	2.2 $\mu$ F	.22 $\mu$ F

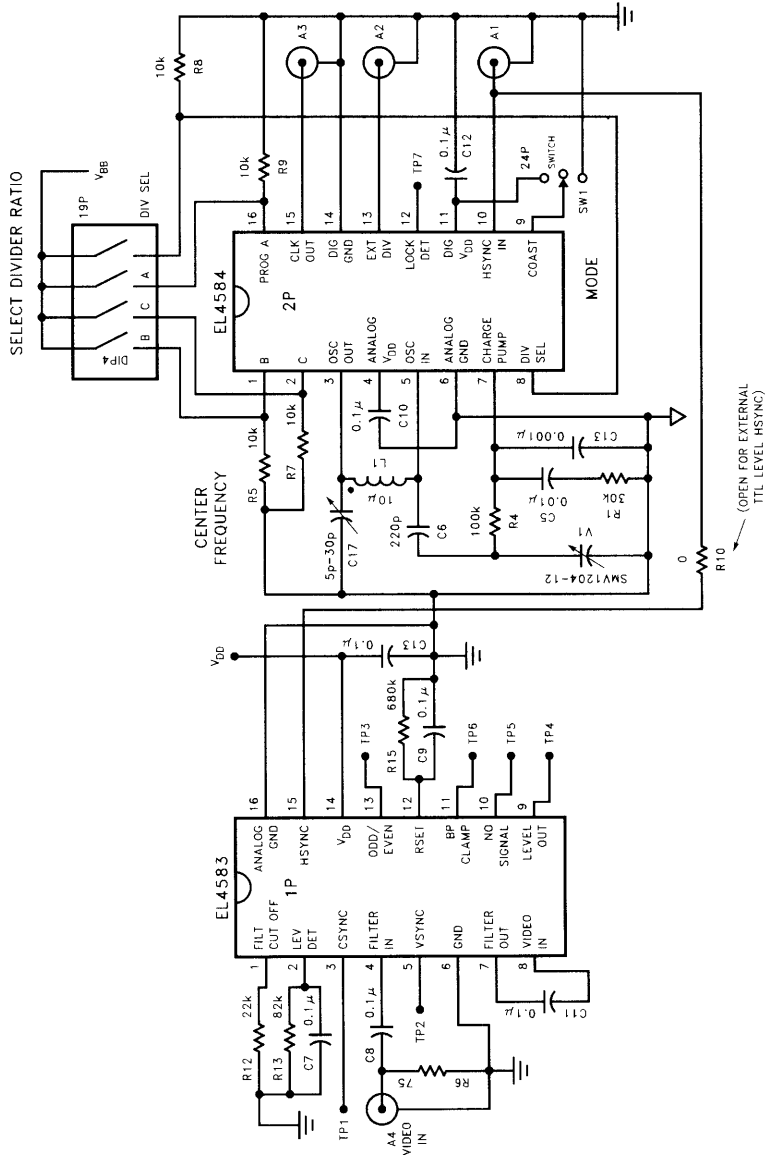
### HDTV

The EL4584C/5C may be used for HDTV where an external counter may be used and the loop filter will have a very low bandwidth. The jitter can be less than 0.5ns but the lock time will be quite long. The loop filter may be single pole or an active filter.

### PCB Layout Considerations

It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to "handwaving" influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.

## Demo Board

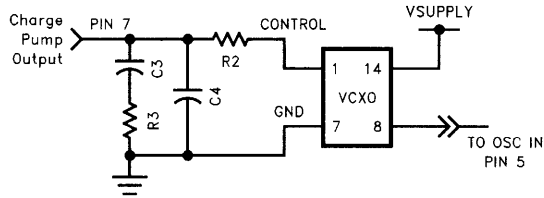


(OPEN FOR EXTERNAL TTL LEVEL HSYNC)

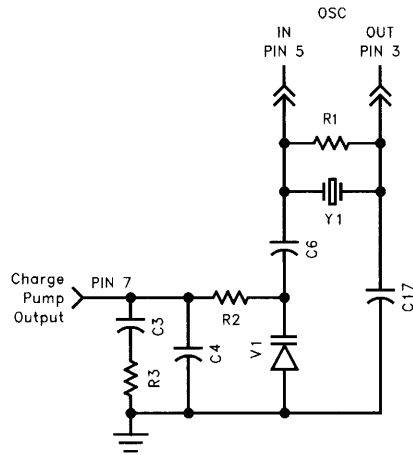
# EL4584C

## Horizontal Genlock, 4 FSC

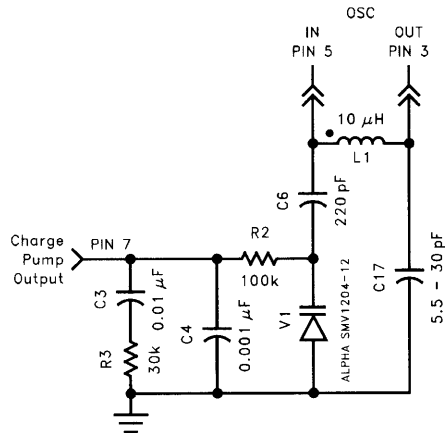
The VCO and loop filter section of the EL4583/4/5 demo board can be implemented in the following configurations:



(1) VCXO



(2) XTAL



(3) LC Tank

## Component Sources

### Inductors

- Dale Electronics  
E. Highway 50  
PO Box 180  
Yankton, SD 57078-0180  
(605) 665-9301

### Crystals, VCXO, VCO Modules

- Connor-Winfield  
2111 Comprehensive Drive  
Aurora, IL 60606  
(708) 851-4722
- Ecliptek Corporation  
3545 Cadillac Ave  
Costa Mesa, CA 92626  
(714) 433-1200
- Reeves-Hoffman  
400 West North Street  
Carlisle, PA 17013  
(717) 243-5929

- SaRonix  
151 Laura Lane  
Palo Alto, CA 94043  
(415) 856-6900
- Standard Crystal  
9940 Baldwin Place  
El Monte, CA 91731  
(818) 443-2121

### Varactors

- Alpha Industries  
20 Sylvan Road  
Woburn, MA 01801  
(617) 935-5150
- Motorola Semiconductor Products  
2100 E. Elliot  
Tempe, AZ 85284  
(602) 244-6900

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