

Shanghai Siproin Microelectronics Co.,Ltd.

Built-in Clock, Calibration Free, Single Phase Energy Meter IC with Integrated Oscillator

SSP1840 Datasheet



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Catalog

1. General Description	
2. Features	3
3. Order specification	4
4. Block Diagram	4
5. Pin Assignment	4
6. Absolute Maximum Ratings	5
7. Electrical Characteristics	5
8. Internal Register Description	7
8.1 Register list	7
8.2 Special Register Description	7
8.2.1 User mode selection register	7
8.2.2 Temperature mode control register	8
9. Theory of Operation	9
9.1 Current and voltage transient waveform measurement	9
9.2 Channel offset correction	10
9.3 Active Power	10
9.4 Active power offset correction	11
9.5 Active power anti-creep	11
9.6 Energy Measurement	11
9.7 Current and Voltage RMS	12
9.8 RMS offset calibration of current and voltage	13
9.9 Leakage/Over-current Detection	13
9.10 Phase Angle Calculation	15
9.11 Zero Crossing Detection	16
9.12 Temperature Measurement	16
10. Communication Interface	17
10.1 SPI	17
10.1.1 Operation Mode	18
10.1.2 Frame Structure	18
10.1.3 Write Operation Timing	19
10.1.4 Read Operation Timing	19
10.1.5 Fault-tolerant mechanism of SPI interface	19
10.2 UART Communication methods	19
10.2.1 Summarize	19
10.2.2 Description	20
10.2.3 Byte Formation	20
10.2.4 Write Timing	20
10.2.5 Read Timing	20
10.2.6 Packet sending mode	21
10.2.7 Protection mechanism of UART interface	22
11. Package Information (TSSOP14)	22
12. Special Instructions	23
Version Change Description	23



1. General Description

SSP1840 is a built-in clock and calibration-free energy metering IC, suitable for single-phase multifunctional electricity meter, smart socket, smart home appliances, electric bicycle charging pile and other applications with better cost performance.

SSP1840 integrates 2 high-precision sigma-delta ADC to measure current and voltage simultaneously. Reference voltage, power management and other analog circuit modules, and processing active power, current and voltage RMS electrical parameters digital signal processing circuit.

SSP1840 can measure electric parameters such as current and voltage RMS, active power, active energy, fast current RMS (for leakage detection/over-current protection), and temperature detection, waveform output and so on. SSP1840 output data through the UART/SPI interface. It is available for the smart socket, smart appliances, single-phase multi-function power meter, electric bicycle charging pile and information requirement of data acquisition in electricity applications.

SSP1840 has a patented anti-creep design, which can be combined with reasonable external hardware design to ensure that the noise energy cannot be calculated in the energy pulse when there is no load.



- 2 high-precision sigma-delta ADC for current and voltage measuring
- The range of current (10mA~35A) @1mohm
- The range of Active energy (1w~7700w) @1mohm@220V
- Measure RMS Voltage and Current, fast current RMS, Active Power, Active Energy
- The gain error is less than 1%, calibration-free when peripheral components meet certain conditions.
- The current channel support electric leakage/over-current monitoring function, the threshold and response time can be configured
- Voltage zero-Crossing logic output
- Built-in waveform register for load type analysis, Waveform data can be output for load type analysis
- Built-in temperature sensor, Meet the requirements of the product itself, such as over-temperature monitoring, high current node preset temperature alarm, room temperature measurement
- SPI (≤900KHz) /UART (4800bps)
- On-chip power supply monitoring, IC reset when VDD is lower than 2.7V(typical).
- On-chip voltage reference of 1.218V
- On-chip 4MHz oscillator circuit
- Power supply 3.3V, low power consumption 10mW (typical)
- Package: TSSOP14





3. Order specification

Part No	Package	Manner of Packing	Devices per bag/reel
SSP1840	TSSOP14	Reel	3000PCS

4. Block Diagram

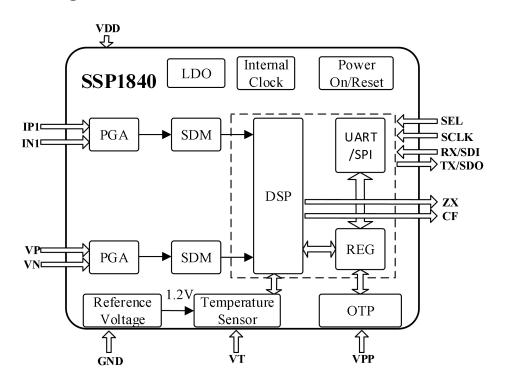


Figure 1 Internal block diagram

5. Pin Assignment

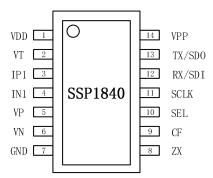


Figure 2 TSSOP14

Pin No.	Pin Name	Description
1	VDD	Power Supply (+3.3V).
2	VT	External temperature sensor(NTC) signal input.
3,4	IP1,IN1	Analog input of current channel, maximum differential voltage has a maximum input range of $\pm 50 \text{mV} (35 \text{mV RMS})$.
5,6	VP,VN	Analog input for voltage channel, this differential input has a maximum input range of $\pm 100 \text{mV} (70 \text{mV RMS})$.



7	GND	GND
8	ZX	Voltage channel zero-crossing output pin
9	CF	Energy pulse output, multiplex function refer to MODE register description
10	SEL	Interface select pin (0: UART 1: SPI), pull-down resistance inside, disconnect is low-level (UART), connected to VDD is high-level (SPI)
11	SCLK	SPI clock input. If using UART interface, this pin doesn't need be connected.
12	RX/SDI	Data input for SPI interface/Receive line for UART interface
13	TX/SDO	Data output for SPI interface/Transmit line for UART interface, this pin require external pull-up resistor.
14	VPP	Reserved, not connected.

6. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power Voltage VDD	VDD	-0.3~+4	V
Analog Input Voltage to GND	IP1,VP	-4~+4	V
Digital Input Voltage to GND	UART_SEL,RX/SDI	-0.3∼VDD+0.3	V
Digital Output Voltage to GND	CF,TX/SDO	-0.3∼VDD+0.3	V
Operating Temperature Range	T	- 40∼+85	$^{\circ}$
Storage Temperature Range	Tstg	- 40~+85	$^{\circ}$ C

Note: Unless specified otherwise, Tamb= 25°C

7. Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Power Supply	VDD		3.0		3.6	V
Power Dissipation	Iop	VDD=3.3V		3		mA
Maranina		4000:1 Input dynamic				
Measuring range		range				
Active energy measurement		35A~100mA Input@		0.2		%
accuracy (large signal)		1mohm sampling resistor		0.2		70
Active energy measurement		100mA~50mA Input@		0.4		0/
accuracy (small signal)		1mohm sampling resistor		0.4		%
Active energy measurement		50mA~10mA Input@		0.6		%
accuracy (tiny signal)		1mohm sampling resistor		0.6		70
RMS measurement		35A~100mA Input@		0.2		%
accuracy(large signal)		1mohm sampling resistor		0.2		70
RMS measurement		100mA~50mA Input@		2		0/
accuracy(small signal)		1mohm sampling resistor		2		%
RMS measurement		50mA~10mA Input@		6		%
accuracy(tiny signal)		1mohm sampling resistor		0		70
East DMS response time	50Hz	Can be set to cycle/half	10		40	mS
Fast RMS response time	60Hz	cycle	8.3		33	mS



SSP1837

Zero-crossing signal output delay				571		uS
Measurement error caused by phase angle between channels (capacitance)	PF08err	Phase advance 37 ° (PF=0.8)			0.5	%
Measurement error caused by phase angle between channels (sensibility)	PF05err	Phase delay 60 ° (PF=0.5)			0.5	%
AC power suppression (output frequency amplitude variation)	ACPSRR	IP/N=100mV			0.1	%
DC power suppression (output frequency amplitude variation)	DCPSRR	VP/N=100mV			0.1	%
Analog input level (current)		Differential current input (peak)			50	mV
Analog input level (voltage)		Differential voltage input (peak)			200	mV
Analog input impedance				370		kΩ
SEL pull-down resistor		SEL (pull-down)		56.9		kΩ
Analog input bandwidth		(-3dB)		3.5		kHz
Internal voltage reference	Vref			1.218		V
Logic input high-level		VDD= $3.3V \pm 5\%$	2.6			V
Logic input low-level		VDD=3.3V±5%			0.8	V
Logic output high-level		VDD=3.3V±5% IOH=5mA	VDD -0.5			V
Logic output low-level		VDD=3.3V±5% IOL=5mA			0.5	V

Note: Unless specified otherwise, Tamb= 25°C

All voltage values take GND terminal potential as reference point.

Test conditions VDD=3.3V, Built-in crystal oscillator, electric energy is measured by CF output.



8. Internal Register Description

8.1 Register list

Address	egister list Symbol	External R/W	Internal R/W	Bits	Default	Description
		Е	lectrical para	ameter r	egister (read o	only)
0x00	IA_FAST_R MS	R	W	24	0x000000	Fast current RMS, unsigned
0x01	IA_WAVE	R	W	20	0x00000	Current waveform register, signed
0x03	V_WAVE	R	W	20	0x00000	Voltage waveform register, signed
0x04	IA_RMS	R	W	24	0x000000	Current RMS register, unsigned
0x06	V_RMS	R	W	24	0x000000	Voltage RMS register, unsigned
0x08	A_WATT	R	W	24	0x000000	Active power register, signed
0x0A	CFA_CNT	R	W	24	0x000000	Active energy pulse count, unsigned
0x0C	A_CORNER	R	W	16	0x0000	Current voltage waveform phase angle register
0x0E	TPS1	R	W	10	0x000	Internal temperature register, unsigned
0x0F	TPS2	R	W	10	0x000	External temperature register, unsigned
		J	Jser operated	d registe	r (read and wi	rite)
0x10	IA_FAST_R MS_CTRL	R/W	R	16	0xFFFF	Fast current RMS control register
0x11	IA_CHOS	R/W	R	8	0x00	Current DC offset correction
0x13	IA_RMSOS	R/W	R	8	0x00	Current RMS offset adjust register
0x15	A_WATTOS	R/W	R	8	0x00	Active power offset adjust register
0x17	WA_CREEP	R/W	R	8	0x0B	Active power no-load threshold register
0x18	MODE	R/W	R	16	0x0000	User mode selection register
0x19	SOFT_RES ET	R/W	R	24	0x000000	When 0x5A5A5A is written, the user area register is reset to default
0x1A	USR_WRPR OT	R/W	R	8	0x00	Write protection register. After writing 0x55, the user operation register can be written. Write other values, user operated register area is not writable
0x1B	TPS_CTRL	R/W	R	16	0x07FF	Temperature mode control register
0x1C	TPS2_A	R/W	R	8	0x0000	External temperature sensor gain coefficient adjust register
0x1D	TPS2_B	R/W	R	8	0x0000	External temperature sensor offset coefficient adjust register

8.2 Special Register Description

8.2.1 User mode selection register (Note: X indicates either 0 or 1)

0x18	MODE	User mode selection register				
No.	name	default value description				
[1:0]	IA_F_SEL	0b00	Current waveform selection	0X: High pass, AC		





			through filter	measurement
				10: Low pass, DC
				measurement
				11: Full wave, AC/DC
				measurement
2~3	reserved	0b00		reserved
				0X: High pass, AC
				measurement
[5.4]	V E CEI	0b00	Voltage waveform selection	10: Low pass, DC
[5:4]	V_F_SEL	UBUU	through filter	measurement
				11: Full wave, AC/DC
				measurement
			Fast effective value selection	0: High pass filter front output
6	L_F_SEL	0b0		1: High pass filter behind
			through filter	output
7	reserved	0b00	rese	erved
0	RMS_UPDATE	01-0	DMC	0: 400ms
8	_SEL	0b0	RMS register update rate	1: 800ms
0	AC EDEO CEL	01-0	A C for many 1 - 4	0: 50Hz
9	AC_FREQ_SEL	0b0	AC frequency select	1: 60Hz
10	Reserved	0b0	rese	erved
11	Reserved	0b0	reserved	
				0: reserved
12	CE INIADIE	01.0	CE	1: Over-current alarm function
12	CF_UNABLE	0b0	CF output function selection	enable by TPS_CTRL[14]
				configured
13~15	Reserved	3b000	reserved	

8.2.2 Temperature mode control register

0x1B	TPS_CTRL	Temperature mode control register			
No.	name	default value	description		
			[15] Temperature switch, default 0b0,Open the temperature measurement	0: on 1: off	
			[14] Alarm switch, default 0b0,	Temperature alarm on Over-current and leakage alarm on	
0x1B	TPS_CTRL	0x07FF	[13:12]] Temperature measurement selection, default 0b00 Automatic temperature measurement	00: Automatic temperature measurement 01: the same as 00 10: Internal temperature measurement 11: External temperature measurement	



[11:10]Temperature measurement interval defau 0b01 100ms	00: 50ms 01: 100ms 10: 200ms 11: 400ms
[9:0] External temperature measurement alarm threshold setting, default 0x3FF,not alarm	

9. Theory of Operation

SSP1840 is composed of analog signal processing module and digital signal processing module. The analog module includes two-channel PGA, two-channel sigma-delta ADC, internal clock, power on/reset monitor, temperature sensor and other related analog modules. The digital module is digital signal processing module (DSP).

9.1 Current and voltage transient waveform measurement

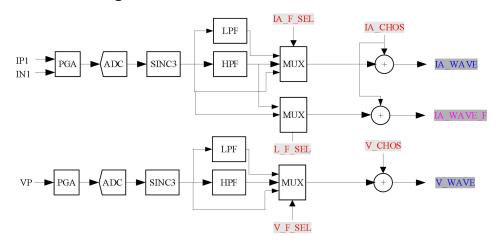


Figure 4

As shown in the figure above, the current and voltage pass through the analog module amplifier (PGA) and the high-precision analog-to-digital conversion (ADC) respectively to get two channels of 1bit PDM to the digital module. The digital module passes through the SINC3 filter (SINC3), optional high-pass filter (HPF) or low-pass filter (LPF) and channel offset correction modules. Obtain the required current waveform data and voltage waveform data (IA_WAVE, V_WAVE).

HPF and LPF are optional for the two channels. HPF is an AC measurement mode, LPF is a DC measurement mode, and full-wave measurement mode is a full-wave measurement mode if neither of them is passed. Set through user MODE register MODE[5:0].

The current and voltage waveform data are updated at a rate of 7.8k. Each sampled data is 20bit signed value, which are saved in waveform registers (I_WAVE, V_WAVE). The waveform value can be read continuously when the SPI rate is greater than 375Kbps.



Adduses	Cromb al	External	Internal	D:4a	Default	Description	
Address	Symbol	R/W	R/W	Bits	Default	Description	
0x01	IA_WAVE	R	R W 20 0x00000 Current wavefo		Current waveform register		
0x03	V_WAVE	R	W			Voltage waveform register	

9.2 Channel offset correction

The SSP1840 contains an 8-bit calibration register (IA_CHOS) with a default value of 00H. They eliminate the deviation caused by the analog-to-digital conversion of the current channel and the voltage channel respectively by the data in the form of the complement of 2. The deviation here may be due to the offset generated by the input and the ANALOG-to-digital conversion circuit itself. The offset correction allows the waveform offset to be 0 without load.

Adduses	Cymhol	External	Internal	D:4a	Dofoult	Description	
Address	Symbol	R/W	R/W	Bits	Default	Description	
0x11	IA_CHOS	R/W	R	8	0x00	Current channel DC offset correction	

These registers are used for DC measurement mode, IA/V LPF SEL=1.

Correction formula: CHOS =
$$\frac{\text{WAVE-WAVE0}}{2^4}$$

WAVE is the corrected waveform value, WAVE0 is the uncorrected waveform value;

Corresponding RMS value: RMS = RMS0 +
$$\frac{3125 * CHOS}{4}$$

RMS is the corrected valid value, RMS0 is the uncorrected valid value.

9.3 Active Power

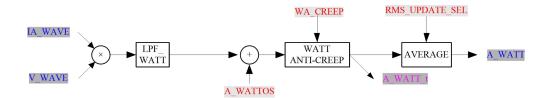


Figure 5

Address	Symbol	External	Internal	Bits	Default	Description	
Audress	Symbol	R/W	R/W	Dits	Delault		
0x08	A_WATT	R	W	24	0x000000	Active power register	

Formula for calculating active power: A_WATT =
$$\frac{4046*I(A)*V(V)*COS (\phi)}{Vref^2}$$

I(A) and V(V) are the voltage RMS of analog input PIN(IP&IN, VP&GND), Φ is the phase angle between I(A) and V(V) (AC signal), Vref is the on-chip reference voltage, the typical value is 1.218V.

This register indicates whether the active power is positive or negative. Bit[23] is the symbol Bit. Bit[23]=0 means the current power is positive and Bit[23]=1 means the current power is negative, in

complement form.

9.4 Active power offset correction

SSP1840 has one 8-bit active power offset adjust register (A_WATTOS), default value is 00H. It eliminate the offset of active power in the measurement of electric energy with the data in the form of complement of 2. Bit[7] is the symbol Bit. The offset may come from board level noise or crosstalk. Offset adjustment can make the values in the active power register close to 0 with no load.

Address	Symbol	External R/W	Internal R/W	Bits	Default	Description
0x15	A_WATTOS	R/W	R	8	0x00	Active power offset adjust register

$$WATTOS = \frac{WATT - WATTO}{8 \times 3.05172}$$

WATT is the active power after adjustment, and WATT0 is the active power before adjustment.

9.5 Active power anti-creep

SSP1840 has the patented power anti-creep function, which ensures that the power of board level noise will not accumulate when there is no load.

This active power no-load threshold register(WA_CREEP) is 8bit unsigned data, default value is 0BH. The corresponding relationship between this value and the active power register value is shown in the following formula. When the absolute value of the input active power signal is less than this value, the output active power is set to 0. This can make the value of the active power register is 0 and the energy does not accumulate in the case of no load, even if there is a tiny noise signal.

Address	Symbol	External	Internal	Bits	Default	Description	
110011000	~J 1112 01	R/W	R/W	2100	20111111	_ = ==================================	
0x17	WA_CREEP	R/W	R	8	0x0B	Active power no-load threshold register	

Set WA_CREEP based on the value of the power register A_WATT, their corresponding relationship as below:

$$WA_CREEP = \frac{WATT}{3.0517578125*8}$$

When the channel is in the anti-creep state, the RMS current register of this channel is also set to 0.

9.6 Energy Measurement

SSP1840 provides energy pulse measurement. The active instantaneous power is integrated by time to get active energy and output calibration pulse CF in proportion. CFA_CNT register saves the count of output energy pulse.

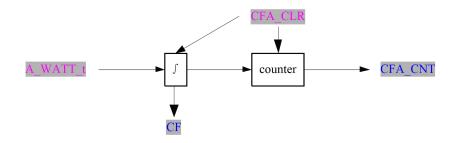


Figure 6

Address	Symbol	External R/W	Internal R/W	Bits	Default	Description
0x0A	CFA_CNT	R	W	24	0x000000	Active energy pulse count, unsigned

The count of active energy pulses corresponds to the consumption of electricity. The count of pulses can be counted directly from the CF pin through I/O interruption. When the period of CF is less than 180ms, the pulse is 50% duty cycle. When it is greater than or equal to 180ms, the fixed pulse width of high-level is 90ms.

Note: CFA_CNT is pulse algebraic sum accumulation. It means that pulse plus at positive energy and minus at negative energy.

The cumulative time of each CF pulse: $t_{CF} = \frac{1638.4*256}{WATT}$

WATT is the corresponding active power register value (A WATT)

9.7 Current and Voltage RMS

The RMS of these channels is shown in the figure below. After the square circuit (X^2) , the low-pass filter (LPF_RMS) and the ROOT circuit (ROOT), the instantaneous value RMS_t of RMS is calculated, and then the average value of the two channels (A RMS, V RMS) is calculated.

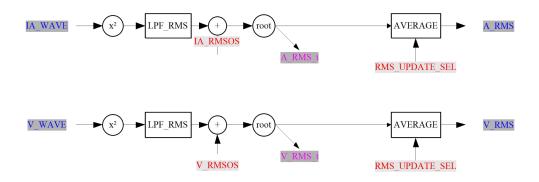


Figure 7



Addmoss	Cymbol	External	Internal	nal Bits Default		Description	
Address	Symbol	R/W	R/W	Bits	Delault	Description	
0x04	IA_RMS	R	W	24	0x000000	Current RMS register, unsigned	
0x06	V RMS	R	W	24	0x000000	Voltage RMS register, unsigned	

0x18	MODE	User mode selection register		
No.	name	default value	description	
8	RMS_UPDATE_SEL	060	RMS register update rate	0: 400ms 1: 800ms

Set MODE[8].RMS_UPDAT_SEL, the average refresh time of RMS can be selected as 400ms or 800ms, and the default value is 400ms. When a current channel is in anti-creep state, the RMS of the current channel is 0.

The current RMS conversion formula: IA_RMS =
$$\frac{324004*I(A)}{Vref}$$

The voltage RMS conversion formula:
$$V_RMS = \frac{79931*V(V)}{V_{ref}}$$

Vref is the reference voltage, the typical value is 1.218V.

I(A) is the input signal between IP1 and IN1 pins (mV), and V(V) is the input signal of VP pins (mV).

9.8 RMS offset calibration of current and voltage

SSP1840 has one 8-bit RMS offset register (IA_RMSOS), whose default value is 00H. It is used to calibrate the deviation in RMS with the complement form of 2. Bit[7] is the sign Bit, This deviation may come from the input noise. Because there is a square operation in calculating the RMS, this may introduce DC offset caused by noise. The deviation calibration can make the value in the RMS register close to 0 without load.

A ddwass	Symbol	External	Internal	Bits	Default	lt Description	
Address	Symbol	R/W	R/W	Dits	its Default		
0x13	IA_RMSOS	R/W	R	8	0x00	Current RMS offset adjust register	

Calibration formula: RMSOS =
$$\frac{RMS^2 - RMS0^2}{9.3132 \times 2^{15}}$$

RMS0 is the RMS current value before correcting and RMS is the RMS current value after correcting.

9.9 Leakage/Over-current Detection

SSP1840 has a fast RMS register, which can detect half cycle or cycle RMS. This function can be used for leakage or over-current detection. The source of waveform L WAVE is shown below.

HPF can be passed or not passed, HPF is not passed by default, can get the absolute value of IA_WAVE_F accumulate by half-cycle or one cycle time, which is selected by FAST_RMS_CTRL[15]. Cycle accumulation is selected by default, The maximum response time is 40ms (50Hz) or 33mS (60Hz), Note that the runout of IA_FAST_RMS register is relatively large when half cycle wave accumulation

occurs. Distinguish between 50Hz and 60Hz half-cycle time (AC_FREQ_SEL).

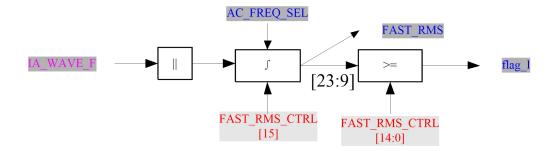


Figure 8

	A ddwass	Symbol	External	Internal	Bits	Default	Description	
	Address	Symbol	R/W	R/W	Dits	Delault		
Ī	0x10	IA_FAST_RMS_C	R/W	D	16	0xFFFF	Fast current RMS control	
	UXIU	TRL	IV W	K	10	UXITIT	register	

Set the refresh time to half-cycle or cycle by IA_FAST_RMS_CTRL, and set the fast RMS threshold (Leakage or over-current threshold).

0x10	MODE	Fast RMS register				
No.	name	default value	description			
	IA EAST DMC CTD		[15]East DMS refresh time	0: half-cycle		
0x10	IA_FAST_RMS_CTR L	0xFFFF	[15]Fast RMS refresh time	1: cycle		
			[14:0]Fast RMS threshold			

Set AC frequency by MODE[9].

0x18	MODE	User mode selection register					
No.	name	default value	description				
0	AC EDEO CEI	01-0	AC frequency	0: 50Hz			
9	AC_FREQ_SEL	0b0	selection	1: 60Hz			

Refresh the 24-bit unsigned RMS register according to one cycle or half cycle, Bit[23:9] of the FAST_RMS register compare with the leakage/over-current threshold FAST_RMS_CTRL [14:0], if the value is greater than or equal to the set threshold, then leakage/over-current alarm output pin will be high level.

A ddwagg	Symbol	External			Default	Description	
Address	Symbol	R/W	R/W	Dits	Default	Description	
0x00	IA_FAST_RMS	R	W	24	0x000000	Fast current RMS, unsigned	

Leakage/over-current alarm output indicator pin is CF, set MODE[12]=1 and TPS_CTRL[14]=1 before use it.

0x18	MODE	User mode selection register					
No.	name	default value	description				
12	CF_UNABLE	0b0	CF output function selection	0: energy pulse, enable by MODE[11] configured			



		1: Temperature
		measurement/Leakage alarm,
		enable by TPS[14] configured

0x1B	TPS_CTRL	Temperature mode control register				
No.	name	default value	description			
	ALERT_CTRL		Alarm	0: Temperature alarm on		
14		0b0	selection	1: Leakage/over-current alarm on		

Since the fast effective values are updated by cycle or half-cycle, the interrupt response time is up to 2 cycles or 2 half-cycles.

9.10 Phase Angle Calculation

SSP1840 has phase angle measurement function. The reactive quadrant can be indicated by the angle of current and voltage respectively by calculating the positive zero-crossing time difference between current and voltage. It is updated to the register CORNER_A when the current is positive zero crossing. The register is a 16-bit unsigned number.

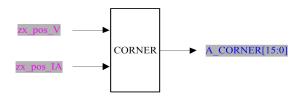


Figure 9

Address	Symbol	External R/W	Internal R/W	Bits	Default	Description
0x0C	A CORNER	R	W	16	0x0000	Current voltage waveform phase
UXUC	A_CORNER	K	VV	10	00000	angle register

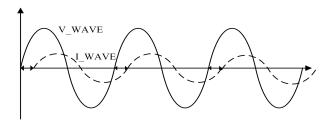


Figure 10

Phase Angle conversion formula: $2*pi*A_CORNER*\frac{f_c}{f_0}$ The unit is radian

Among them, f_c is the frequency of the AC signal source, the default value is 50Hz. f_0 is the sampling frequency, the typical value is 1MHz.



9.11 Zero Crossing Detection

SSP1840 has the voltage zero-crossing detection function, and the zero-crossing signal is directly output by pin ZX. When ZX=0, it indicates the positive half cycle of the waveform, and when ZX=1, it indicates the negative half cycle of the waveform. The delay between the zero-crossing signal and the actual input signal is about 570us.

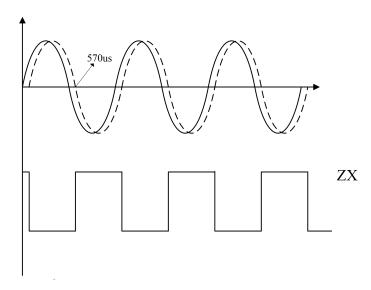


Figure 11

9.12 Temperature Measurement

SSP1840 supports internal temperature measurement and external temperature measurement.

External temperature measurement, optional output alarm indicator, Turn on the alarm function, CF pin selection output alarm signal, the CF pin will output high-level if the TPS2 is greater than or equal to the alarm threshold, Temperature indicator alarm. when the temperature value is lower than the alarm value or the alarm function is turned off, Exit alarm indicator.

0x1B	TPS_CTRL		Temperature mode control reg	ister		
No.	name	default value	description	n		
			[15] Temperature measurement switch, default 0b0,Open the temperature measurement [14] Alarm selection, default 0b0,	0: on 1: off 0: Temperature alarm on 1: Leakage/over-current		
0x1B	TPS_CTRL	0x07FF	[13:12]Temperature measurement selection, default 0b00 Automatic temperature measurement	alarm on 00: Automatic temperature measurement 01: the same as 00 10: internal temperature measurement 11: external temperature measurement		
			[11:10]Temperature measurement	00: 50ms		



interval selection , default 0b01 100ms	01: 100ms 10: 200ms 11: 400ms
[9:0]External temperature alarm threshold, default 0x3FF	

First set MODE[12]=1, and then set TPS_CTRL[14]=0, then CF pin is turned on to output external temperature alarm indicator.

0x18	MODE	User mode selection register						
No.	name	default value description						
12	CF_UNABLE	0ь0	CF output function selection	0: energy pulse, enable by MODE[11] configured 1: Temperature measurement alarm, enable by TPS[14] configured				

The external and internal temperature values are saved in the TPS2 and TPS1 registers respectively.

Address	Symbol	External R/W	Internal R/W	Bits	Default	Description
0x0E	TPS1	R	W	10	0x0000	Internal temperature register, unsigned
0x0F	TPS2	R	W	10	0x0000	External temperature register, unsigned

Internal temperature measurement formula: Tx=(170/448)(TB/2-32)-45

TB is the value in TPS1

The external temperature is measured by SAR ADC. The maximum input signal of the VT pin is 0.55*VDD~(V), The TPS2 register value is the corresponding AD sampling value, full scale is 1024.

Address	Symbol	External	Internal	D:4-	D - 6 14	Description
		R/W	R/W	Bits	Default Description	
0x1C	TPS2 A	R/W	R	8	0x00	External temperature sensor gain
UXIC	1F32_A	IV W	K	0	UXUU	coefficient correction A register
0 _v ,1D	TDC2 D	D /W/	D	0	000	External temperature sensor offset
0x1D	TPS2_B	R/W	R	8	0x00	coefficient correction B register

10. Communication Interface

Register data are sent as 3 bytes (24bit). The data is fixed 3 bytes, if valid data bytes are less than 3 bytes, invalid bits are filled with 0.

10.1 SPI

- Select by pin UART SELL, multiplex with UART
- Slave mode
- Half-duplex communication, the communication rate can be configured, the maximum communication rate is 900khz
- 8-bit data transmission, MSB first, LSB last
- Clock polarity / phase (CPOL = 0, CPHA = 1)



10.1.1 Operation Mode

The master device works in Mode1: CPOL=0, CPHA=1, In idle state, SCLK is at low-level. Data is transmitted on the first edge, which is the transition from low level to high level of SCLK, so data is received on the falling edge and data is sent on the rising edge.

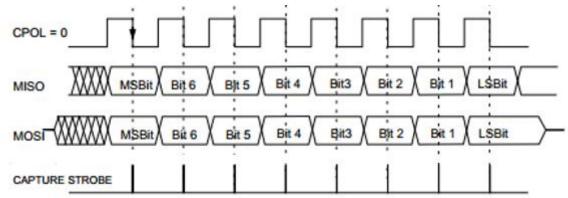


Figure 12

10.1.2 Frame Structure

In SPI communication mode, MCU send 8-bit identification byte (0x58) or (0x58) is the read operation identification byte and (0xA8) is the write operation identification byte. Then send the address byte of the register will be accessed (refer to SSP1840 register list). The below figure shows the data transfer sequence for read and write operations respectively. After one frame of data is transmitted, SSP1840 re-enters the communication mode. The number of SCLK pulses required for each reading and writing operation is 48 bits.

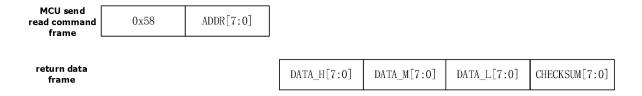
There are two types of frame structures, which are explained as follows:

1) Write operation frame

Write operation frame	0xA8	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]	
--------------------------	------	-----------	-------------	-------------	-------------	---------------	--

The checksum byte is ((0xA8 + ADDR + DATA_H + DATA_M+ DATA_L) & 0xFF) and then bitwise inverted.

2) Read operation frame



The checksum byte is $(0x58 + ADDR + DATA_H + DATA_M + DATA_L) & 0xFF)$ and then bitwise inverted.



10.1.3 Write Operation Timing

The serial write timing is performed as follows. The frame identification byte {0xA8} indicates that the data communication operation is data writing. The MCU need make the data ready before the lower edge of SCLK, and shift the data at the lower edge of this clock. All remaining bits of the data are also shifted left on the lower edge of this SCLK (Figure 13) $_{\circ}$

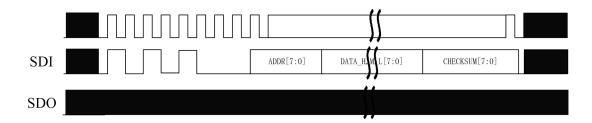


Figure 13

10.1.4 Read Operation Timing

During the data read operation, SSP1840 shifts the corresponding data to the DOUT pin on the rising edge of SCLK. DOUT keeps unchanged during SCLK =1.MCU can sample DOUT value before the next falling edge. MCU must send a read command frame first before read operation.



Figure 14

When SSP1840 is in communication mode, the frame identification byte {0x58} indicates that the data communication operation is data reading. After receiving the register address, SSP1840 starts to shift out the data in the register on the rising edge of SCLK (Figure 14). All remaining bits of the register data are shifted out on subsequent rising SCLK edges. Therefore, On the falling edge of SCLK, an external device can sample the output data of the SPI. Once the read operation is completed, SPI re-enters the communication mode. SDO enters a high-impedance state on the falling edge of the last SCLK signal.

10.1.5 Fault-tolerant mechanism of SPI interface

SPI supports soft reset function, reset SPI interface individually by sending 6bytes of 0xFF.

10.2 UART Communication methods

10.2.1 Summarize

SSP1840 supports UART communication. The UART interface only requires two low speed optocouplers to achieve isolated communication.

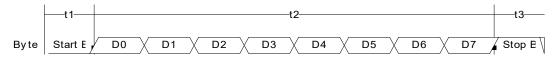
Baud rate: 4800bps Check bits: None Data bits: 8 Stop bits: 1.5 Slave mode, half-duplex communication



10.2.2 Description

UART port Settings: Communication baud rate is 4800bps, no parity, stop bit 1.5.

10.2.3 Byte Formation

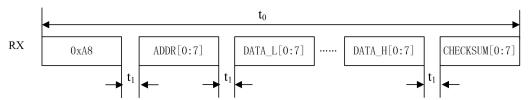


Start bit low duration: t1=208us;

Valid data bit duration: t2=208*8=1664us Stop bit high duration: t3=208us+104us

10.2.4 Write Timing

The data write sequence of the host UART is shown in the figure below. The host sends command bytes (0xA8) first, then write address bytes (ADDR), then sends data bytes in sequence, and finally checksum bytes.

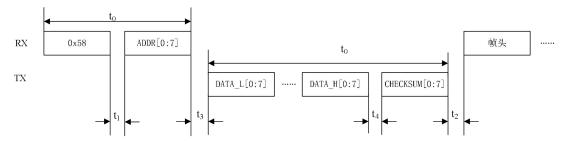


(0xA8)is the frame identification byte for the write operation. ADDR is the internal target register in SSP1840 corresponding to the write operation.

The checksum byte is ((0xA8+ADDR+Data L+Data M+Data H) & 0xFF) and then bitwise inverted.

10.2.5 Read Timing

The timing of reading data is shown below. MCU first sends the command byte (0x58) and the address of the target register (ADDR), and then SSP1840 sends data bytes in sequence. Finally sends the checksum byte.



(0x58) is the frame identification byte for the read operation. ADDR is the internal target register in SSP1840 corresponding to the read operation.

The checksum byte is ((0x58+ADDR+Data L+Data M+Data H) & 0xFF) and then bitwise inverted.



Timing Description:

	Description	Min	Type	Max	Unit
t1	Interval between MCU sending bytes	0		20	mS
t2	Frame interval	0.5			uS
t3	Interval between the end of MCU sending register address and SSP1840		72		uS
	sending byte during read operation				
t4	Interval between SSP1840 sending bytes		116		uS

10.2.6 Packet sending mode

After received the command "(0x58) + 0xAA", SSP1840 will return a full electrical parameter data packet. The returned data packet has a total of 35 bytes, and 4800bps takes 77ms. The specific format is: Frame head (1byte head) \rightarrow Current A fast effective value (3byte IA_FAST_RMS) \rightarrow Current A effective value (3byte IA_RMS) \rightarrow reserved (3byte) \rightarrow Effective voltage (3byte V_RMS) \rightarrow reserved (3byte) \rightarrow Channel A power value (3byte A_WATT) \rightarrow reserved (3byte) \rightarrow Channel A pulse meter value (3byte CFA_CNT) \rightarrow reserved (3byte) \rightarrow Internal thermometer value (2byte TPS1 + 1byte 0) \rightarrow External thermometer value (2byte TPS2 + 1byte 0) \rightarrow Checksum value (1byte CHECKSUM).

Full electrical parameter data packet format:

Name	No.	Value	Name	No.	Value
Frame head	0	Head (0x55)		19	reserved
IA_FAST_RMS	1	IA_FAST_RMS_1	reserved	20	reserved
	2	IA_FAST_RMS_m		21	reserved
	3	IA_FAST_RMS_h		22	CFA_CNT_1
IA_RMS	4	IA_RMS_1	CFA_CNT	23	CFA_CNT_m
	5	IA_RMS_m		24	CFA_CNT_h
	6	IA_RMS_h		25	reserved
reserved	7	reserved	reserved	26	reserved
	8	reserved		27	reserved
	9	reserved		28	TPS1_1
V_RMS	10	V_RMS_1	TPS1	29	TPS1_m
	11	V_RMS_m		30	0x00
	12	V_RMS_h		31	TPS2_1
reserved	13	reserved	TPS2	32	TPS2_m
	14	reserved		33	0x00
	15	reserved	checksum	34	checksum
A_WATT	16	A_WATT_1			
	17	A_WATT_m			
	18	A WATT h	1		

checksum= (0x58 + 0x55 + data1 + dat



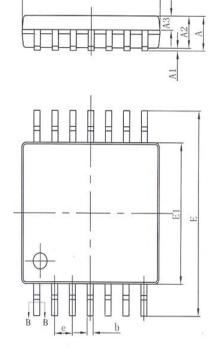
10.2.7 Protection mechanism of UART interface

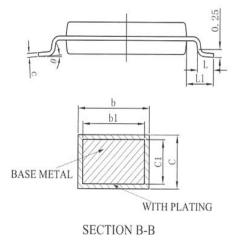
UART communication has a timeout protection mechanism. If the interval between bytes exceeds 18.5ms, the UART interface will automatically reset.

If the frame identification byte is incorrect or the checksum byte is incorrect, the frame data will be discarded.

UART module reset: The RX pin is pulled high after the low-level exceeds 6.65mS, and the UART module will be reset.

11. Package Information (TSSOP14)





SYMBOL	MILLIMETER				
31 MBOL	MIN	NOM	MAX		
A		s s	1.20		
A1	0.05	_	0.15		
A2	0.90	1.00	1.05		
A3	0.39	0.44	0.49		
b	0.20		0.28		
b1	0.19	0.22	0.25		
c	0.13	_	0.17		
cl	0.12	0.13	0.14		
D	4.90	5.00	5.10		
E1	4.30	4.40	4.50		
Е	6.20	6.40	6.60		
e	0.65BSC				
L	0.45	0.60	0.75		
L1	1.00BSC				
0	0		8°		



12. Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version: V1.03 Author: Lifeng Liu Time: 2021.9.09

Modify the record:

1. Re-typesetting the manual and checking some data

Statement

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