3A, Ultra Low Dropout Linear Regulator

1 FEATURES

- **3A Maximum Output Current**
- **Low Dropout Voltage**
  - **250mV(TYP) at 3A Output Current**
- **Output Voltage Accuracy: ±2%(TYP)**
- **Adjustable Output Voltage**
- **Fast Transient Response**
- **Power-On-Reset Monitoring on Both VCNTL and VIN Pins**
- **Internal Soft-Start**
- **Current-Limit and Short Current-Limit Protections**
- **Low Shutdown Quiescent Current**
- **Shutdown/Enable Control Function**
- **Temperature Protection and Over-Current Protection Function**
- **Open-Drain VOUT Voltage Indicator**
- **ESOP8 and DFN3x3-10L Packages**

2 APPLICATIONS

- **Note Book PC**
- **Motherboard Applications**
- **Front Side Bus VTT (1.2V/3A)**

3 DESCRIPTIONS

The RS3235 is a 3A ultra low dropout linear regulator. This device needs two supply voltages, one is a control voltage (V_{CNTL}) for the control circuitry, the other is a main supply voltage (V_{IN}) for power conversion, to reduce power dissipation and provide extremely low dropout voltage.

The RS3235 integrates many functions. A Power-On Reset (POR) circuit monitors both supply voltages on VCNTL and VIN pins to prevent erroneous operations.

The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads. A POK indicates the output voltage status with a delay time set internally. It can control other converter for power sequence. The RS3235 can be enabled by other power systems. Pulling the EN voltage below 0.5V shut off the output.

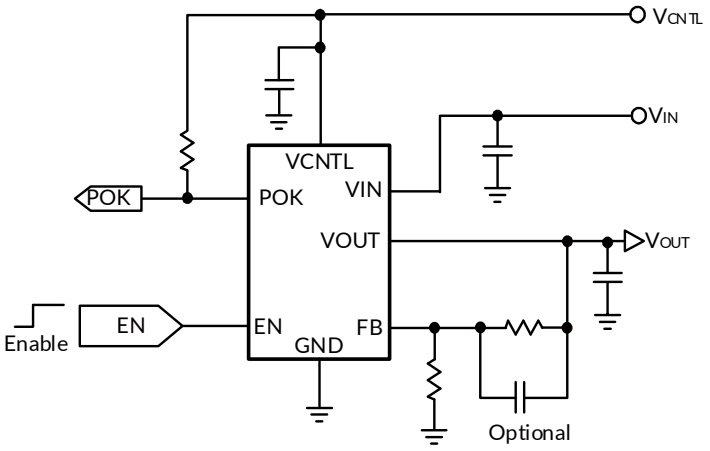
The RS3235 is available in Green ESOP8 and DFN3×3-10L packages. It operates over an ambient temperature range of -40°C to +85°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS3235	DFN3x3-10L	3.00mm×3.00mm
	ESOP8	4.90mm x 3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Application Circuit



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5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2023/03/02	Initial version completed
A.1	2023/08/28	1、Add dropout voltage at I_{OUT}=2A 2、Update the $V_{IN(MIN)}$ input voltage

6 PACKAGE/ORDERING INFORMATION (1)

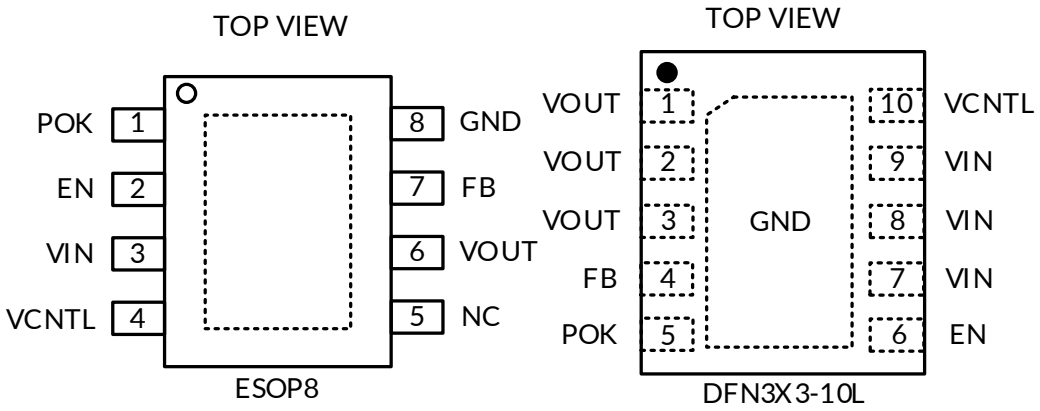
PRODUCT	ORDERING NUMBER	V_{OUT} Accuracy (TYP)	PACKAGE LEAD	PACKAGE MARKING (2)	PACKAGE OPTION
RS3235	RS3235YTDC10	±2%	DFN3x3-10L	RS3235	Tape and Reel,5000
	RS3235YEK	±2%	ESOP8	RS3235	Tape and Reel,4000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information(include data code and vendor code)，the logo or the environmental category on the device.

7 PIN Configuration and Functions (Top View)



PIN DESCRIPTION

NAME	PIN		FUNCTION
	DFN3x3-10L	ESOP8	
GND	Exposed PAD (1)	8	Ground pin of the circuitry.
VOUT	1,2,3	6	Output pin of the regulator. Connecting this pin to load and output capacitors (10μF at least) is required for stability and improving transient response. The output voltage is programmed by the resistor divider connected to FB pin. The VOUT can provide 3A (max.) load current to loads. During shutdown, the output voltage is quickly discharged by an internal pull-low MOSFET.
VIN	7,8,9	3	Main supply input pin for voltage conversions. A decoupling capacitor (≥10μF recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On-Reset purpose.
EN	6	2	Active-high enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new soft-start process. When leave this pin open, an internal pull-up/low current pulls the EN voltage and enables/shuts down the regulator.
FB	4	7	Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.
POK	5	1	Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing FB voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.
VCNTL	10	4	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (0.1μF typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On-Reset purpose.
NC	/	5	No Connection

(1) Connected to ground plane for better heat dissipation.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
V_{IN}	VIN Supply Voltage (VIN to GDN)		-0.3	7	V
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)		-0.3	7	
V_{OUT}	VOUT to GND Voltage		-0.3	7	
	POK to GND Voltage		-0.3	7	
	EN, FB to GND Voltage		-0.3	7	
θ_{JA}	Package thermal impedance (3)	DFN3×3-10L		50	°C/W
		ESOP8		50	
Temperature	Lead Temperature (Soldering,10secs)			260	°C
	Junction, T_J (4)		-40	150	
	Storage, T_{stg}		-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the GND pin.

(3) The package thermal impedance is calculated in accordance with JESD-51.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	
		Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

			MIN	MAX	UNIT
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)		3.0	6.0	V
V_{IN}	VIN Supply Voltage (VIN to GND)		1.0	6.0	V
V_{OUT}	VOUT Output Voltage (when V_{CNTL} - V_{OUT} >2V)		0.8	V_{IN} - V_{DROP}	V
	EN, FB, POK to GND Voltage		-0.3	6.0	V
I_{OUT}	VOUT Output Current	Continuous Current	0	3	A
		Peak Current	0	4	
C_{OUT}	VOUT output Capacitance (1)		10	2200	uF
$ESRC_{OUT}$	ESR of VOUT output capacitor		0	200	mΩ
T_J	Operating Junction temperature		-40	+125	°C
T_A	Ambient Temperature		-40	85	°C

(1) In this data sheet, the effective value of capacitance is defined as the actual capacitance under D.C. bias and temperature; not the rated or nameplate values.

8.4 Electrical Characteristics

(Unless otherwise noted, the specifications apply over V_{CNTL}=5V, V_{IN} = 1.8V, V_{OUT} =1.2V, T_A = -40°C to +85°C, typical values are at T_A = +25°C) (1)

PARAMETER		TEST CONDITIONS		TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY AND CURRENTS								
I_{CNTL}	VCNTL Supply Current	EN=HIGH, I_{OUT}=0A, POK=HIGH		+25°C		105	130	uA
				Full (4)			150	uA
I_{SD_VCNTL}	VCNTL Supply Current at Shutdown	EN = LOW		Full			1	uA
I_{SD_VIN}	VIN Supply Current at Shutdown	EN = LOW		+25°C			1	uA
		EN = LOW		Full			5	uA
POWER-ON-RESET(POR)								
	Rising VCNTL POR Threshold			+25°C	2.5	2.7	2.9	V
	VCNTL POR Hysteresis			+25°C		0.4		V
	Rising VIN POR Threshold			+25°C	0.8	0.9	1	V
	VIN POR Hysteresis			+25°C		0.5		V
OUTPUT VOLTAGE								
V_{REF}	Reference Voltage	FB=VOUT		+25°C		0.8		V
	Output Voltage Accuracy	V_{CNTL}=3.0~5.5V, I_{OUT}= 0~3A		+25°C		±2		%
	Load Regulation	I_{OUT} = 0~3A		+25°C		10		mV
	Line Regulation	I_{OUT}=10mA, V_{CNTL}=3.0~5.5V		+25°C	-0.15		0.15	%/V
	VOUT Pull-Low Resistance	V_{CNTL}=5V,V_{EN}=0V,V_{OUT}<0.8V		+25°C		55		Ω
	FB Input Current	V_{FB} = 0.8V		+25°C	-100		100	nA
DROPOUT VOLTAGE								
V_{DROP}	VIN-to-VOUT Dropout Voltage	V_{CNTL} = 5.0V I_{OUT} = 2A	V_{OUT}=2.5V	+25°C		0.16		V
				Full			0.24	
			V_{OUT}=1.8V	+25°C		0.15		V
				Full			0.21	
			V_{OUT}=1.2V	+25°C		0.14		V
				Full			0.20	
		V_{CNTL} = 5.0V I_{OUT} = 3A	V_{OUT}=2.5V	+25°C		0.25		V
				Full			0.36	
			V_{OUT}=1.8V	+25°C		0.22		V
				Full			0.33	
			V_{OUT}=1.2V	+25°C		0.21		V
				Full			0.31	
I_{LIM}	Current-Limit Level			+25°C		5.5		A
				Full	4			
PROTECTIONS								
I_{SHORT}	Short Current-Limit Level	V_{FB}<0.2V		+25°C		1.4		A
	Short Current-Limit Blanking Time	From beginning of soft-start		+25°C		2		ms
t_{SD}	Thermal Shutdown Temperature	T_J rising		+25°C		160		°C
	Thermal Shutdown Hysteresis			+25°C		50		°C

ENABLE AND SOFT-START							
V_{EN}	EN Logic High Threshold Voltage	EN rising	+25°C	1.2			V
	EN Logic Low Threshold Voltage	EN falling	+25°C			0.5	V
R_{EN_PL}	EN Internal Pull-Low Resistance		+25°C	800	1400	2000	kΩ
t_{SS}	Soft-Start Interval	V_{OUT} = 10% to 90%	+25°C		2		ms
			Full	1		4	ms
t_{ON}	Turn On Delay	From being enable to V_{OUT} rising 10%	+25°C		240		us
Power-OK and DELAY							
V_{TH_POK}	Rising POK Threshold Voltage	V_{FB} rising	+25°C	90	93	96	%
	POK Threshold Hysteresis		+25°C		8		%
	POK Pull-low Voltage	POK sink 5mA	+25°C		0.2	0.4	V
	POK Debounce Interval	V_{FB}<falling POK voltage threshold	+25°C		10		us
	POK Delay Time	From V_{FB}=V_{TH_POK} to rising edge of the V_{POK}	+25°C	1	3	4	ms

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) T_J = -40°C to +125°C.

8.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{CNTL} =5V, V_{IN} = 1.8V, V_{OUT} = 1.2V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.

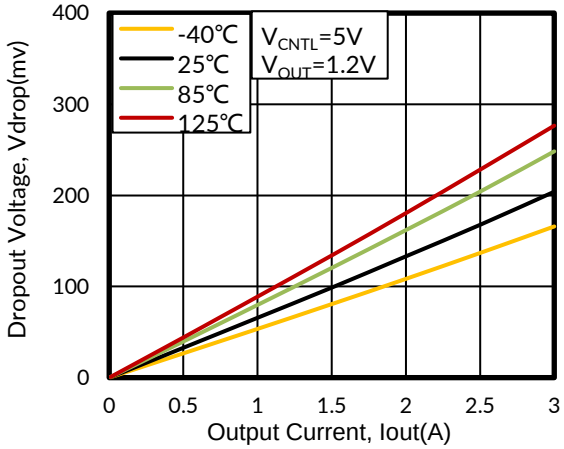


Figure 1. Dropout Voltage vs Output Current

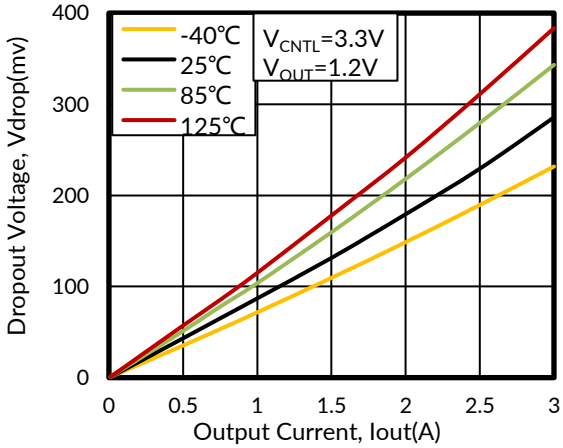


Figure 2. Dropout Voltage vs Output Current

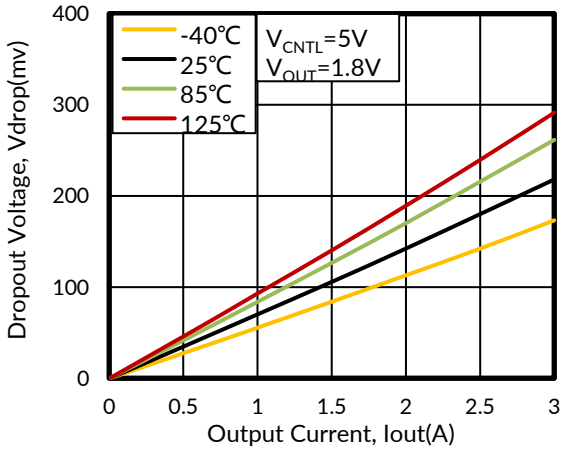


Figure 3. Dropout Voltage vs Output Current

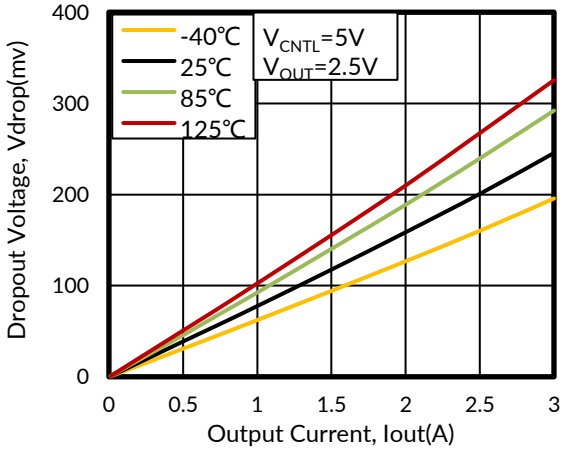


Figure 4. Dropout Voltage vs Output Current

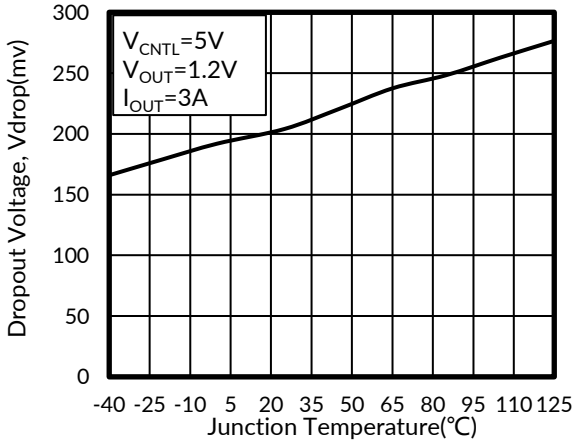


Figure 5. Dropout Voltage vs Junction Temperature

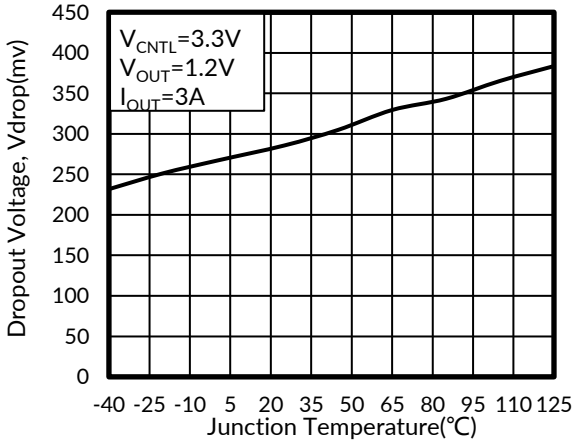


Figure 6. Dropout Voltage vs Junction Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{CNTL} =5V, V_{IN} = 1.8V, V_{OUT} = 1.2V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.

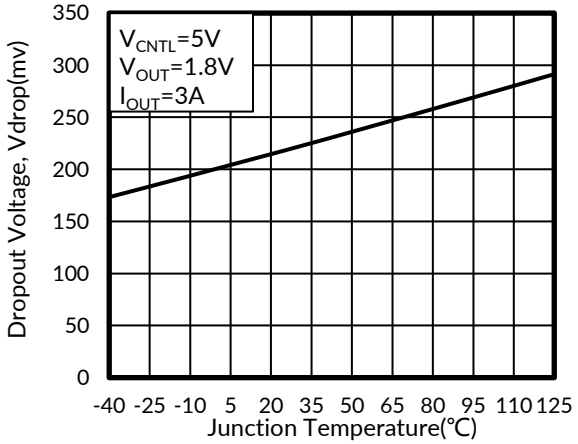


Figure 7. Dropout Voltage vs Junction Temperature

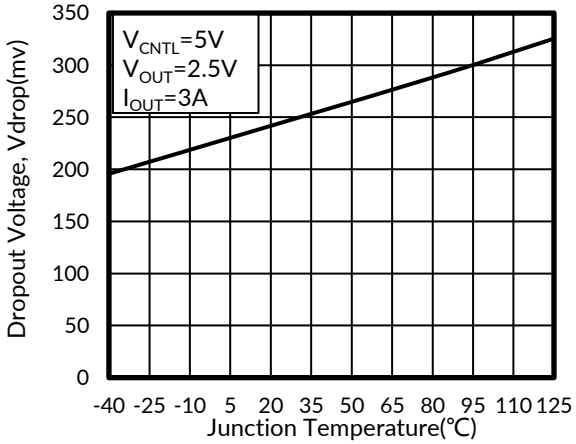


Figure 8. Dropout Voltage vs Junction Temperature

Figure 9. Reference Voltage vs Junction Temperature

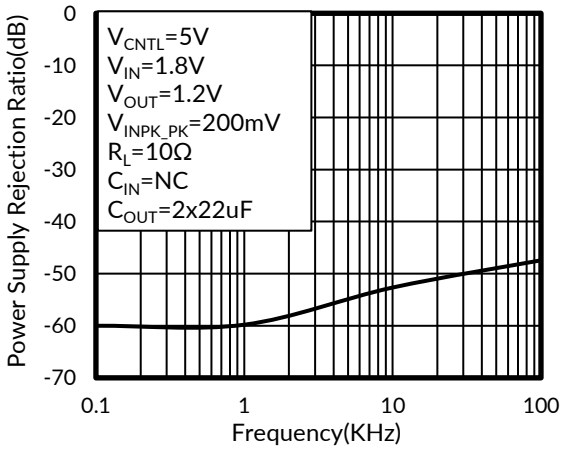


Figure 10. VIN Power Supply Rejection Ratio

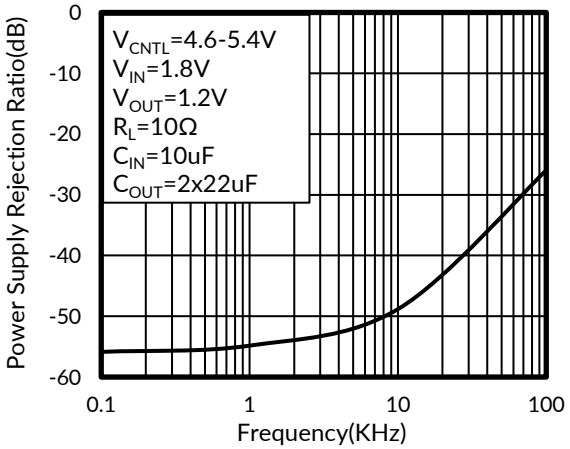


Figure 11. VCNTL Power Supply Rejection Ratio

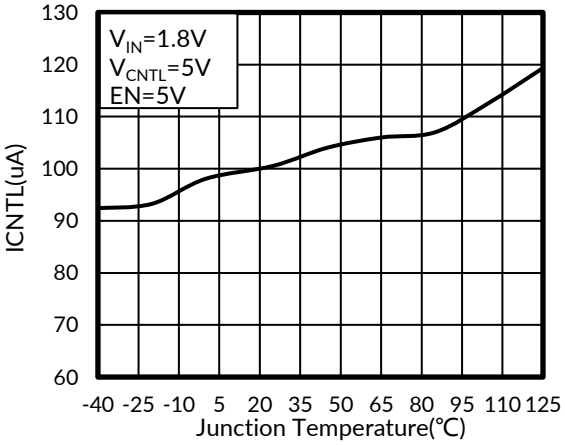


Figure 12. VCNTL Current vs Junction Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{CNTL} =5V, V_{IN} = 1.8V, V_{OUT} = 1.2V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.

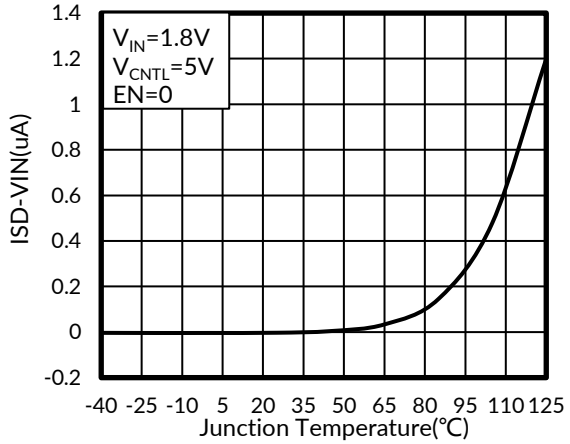


Figure 13. VIN Current vs Junction Temperature

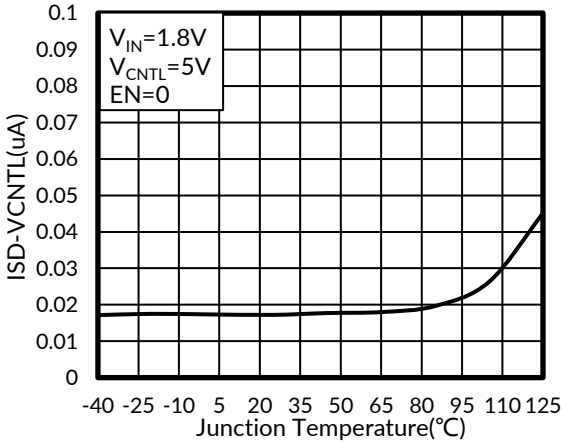


Figure 14. VCNTL Current vs Junction Temperature

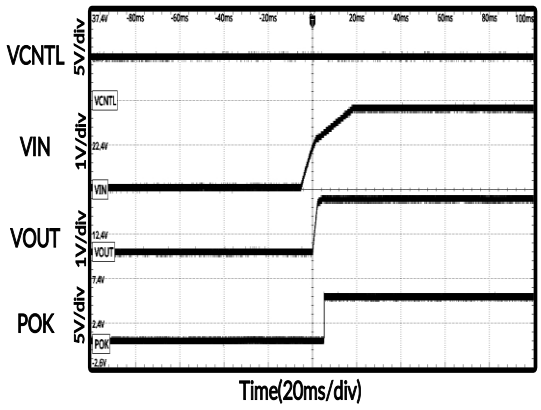


Figure 15. POWER ON

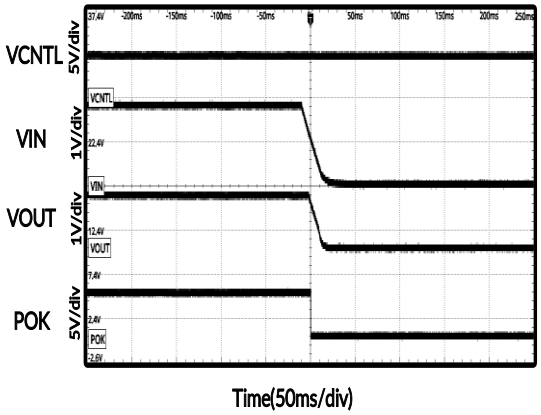


Figure 16. POWER OFF

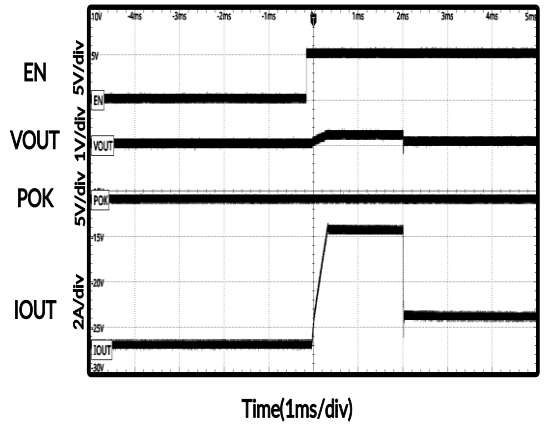


Figure 17. Short Circuit First, Then Turn On

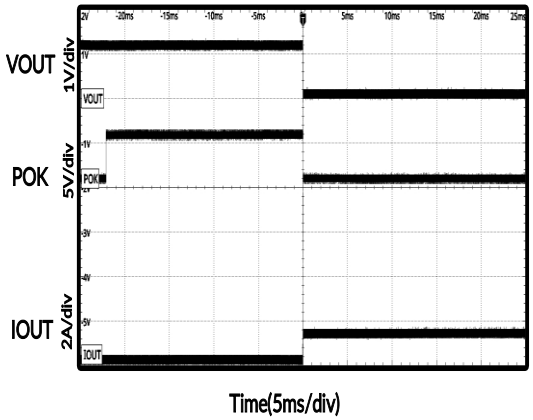


Figure 18. Turn On First, Then Short Circuit

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{CNTL} =5V, V_{IN} = 1.8V, V_{OUT} = 1.2V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.

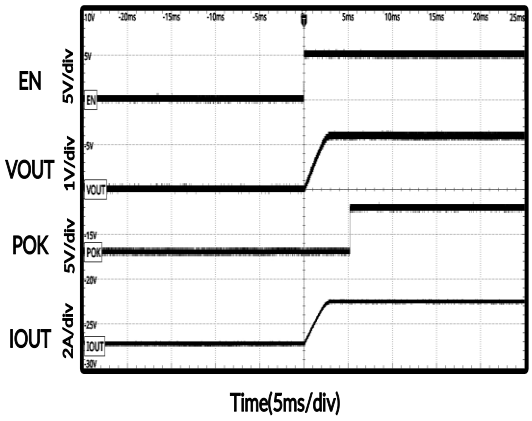


Figure 19. ENABLE

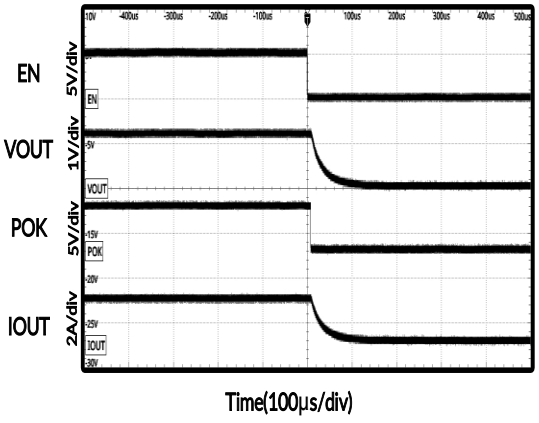


Figure 20. Shutdown

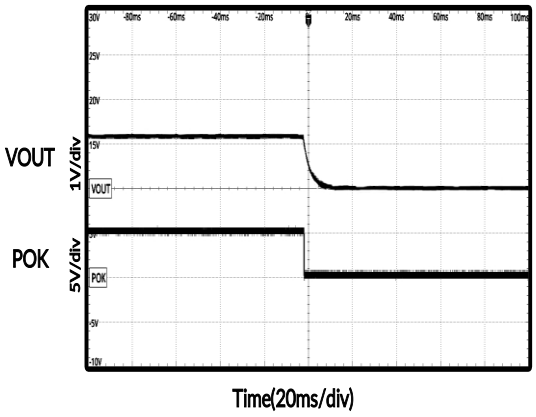


Figure 21. Enter Over Temperature Protection

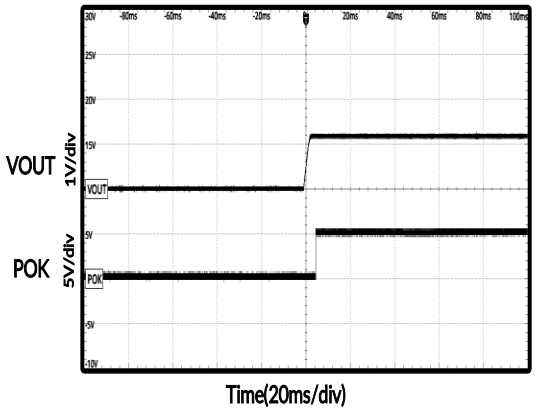
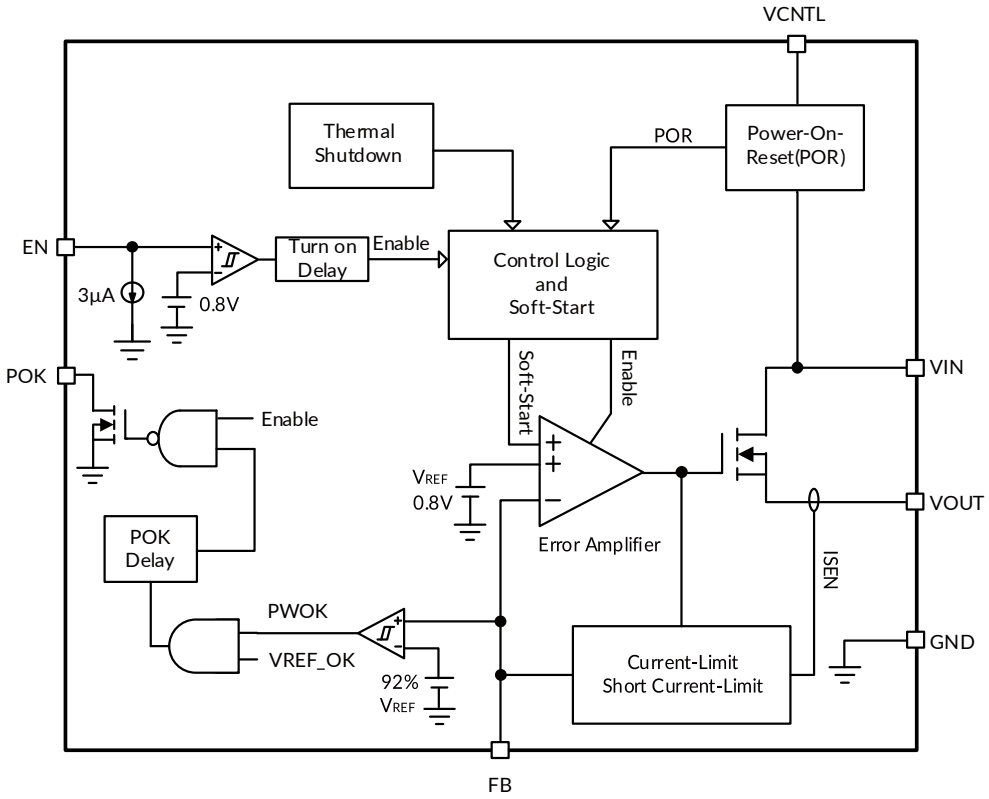


Figure 22. Exit Over Temperature Protection

9 Function Description

RS3235 series low dropout linear regulator (LDO) is a high performance, low dropout voltage regulator. This device needs two supply voltages, one is a control voltage for the control circuitry, the other is a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout voltage.

9.1 Functional Block Diagram



9.2 Power-on-Reset

A Power-On-Reset (POR) circuit monitors both of supply voltages on VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both of the supply voltages exceed their rising POR voltage thresholds during powering on. The POR function also pulls low the POK voltage regardless the output status when one of the supply voltages falls below its falling POR voltage threshold.

9.3 Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge during start-up. The typical soft-start interval is about 2ms.

9.4 Output Voltage Regulation

An error amplifier works with a temperature-compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier is designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

9.5 Current-Limit Protection

The RS3235 monitors the current flowing through the output NMOS and limits the maximum current to prevent load and RS3235 from damages during current overload conditions.

9.6 Output Capacitor

The RS3235 requires a proper output capacitor to maintain stability and improve transient response. The output capacitor selection is dependent upon ESR (equivalent series resistance) and capacitance of the output capacitor over the operating temperature. Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as output capacitors.

During load transients, the output capacitors, depending on the stepping amplitude and slew rate of load current, are used to reduce the slew rate of the current seen by the RS3235 and help the device to minimize the variations of output voltage for good transient response. For the applications with large stepping load current, the low ESR bulk capacitors are normally recommended. Decoupling ceramic capacitors must be placed at the load and ground pins as close as possible and the impedance of the layout must be minimized.

9.7 Short Current-Limit Protection

The short current-limit function reduces the current-limit level down to 1.4A (typical) when the voltage on FB pin falls below 0.2V (typical) during current overload or short circuit conditions.

The short current-limit function is disabled for successful start-up during soft-start interval.

9.8 Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of RS3235. When the junction temperature exceeds +160°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start process after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal over load conditions. The thermal shutdown is designed with a 50°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device.

For normal operation, the device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

9.9 Input Capacitor

The RS3235 requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance. Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as an input capacitor of VIN. For most applications, the recommended input capacitance of VIN is 10μF at least.

However, if the drop of the input voltage is not cared, the input capacitance can be less than 10μF. More capacitance reduces the variations of the supply voltage on VIN pin.

9.10 Enable Control

The RS3235 has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. When left open, this pin is pulled up/low by an internal current source to enable/shutdown normal operation. It's not necessary to use an external transistor to save cost.

9.11 Power-OK and Delay

The RS3235 indicates the status of the output voltage by monitoring the feedback voltage (V_{FB}) on FB pin. As the V_{FB} rises and reaches the rising Power-OK voltage threshold (V_{THPOK}), an internal delay function starts to work. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate that the output is ok. As the V_{FB} falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK (after a debounce time of 10μs typical).

9.12 Power Sequencing

The power sequencing of VIN and VCNTL is not necessary to be concerned. However, do not apply a voltage to VOUT for a long time when the main voltage applied at VIN is not present. The reason is the internal parasitic diode from VOUT to VIN conducts and dissipates power without protections due to the forward-voltage.

9.13 Setting Output Voltage

The output voltage is programmed by the resistor divider connected to FB pin. The preset output voltage is calculated by the following equation:

V_{OUT} = 0.8 x (R1+R2)/R2

Where R1 is the resistor connected from V_{OUT} to FB with Kelvin sensing connection and R2 is the resistor connected from FB to GND. A bypass capacitor(C1) may be connected with R1 in parallel to improve load transient response and stability.

10 Layout

10.1 Layout Consideration

1. Please solder the Exposed Pad on the ground pad on the top-layer of PCBs. The ground pad must have wide size to conduct heat into the ambient air through the ground plane and PCB as a heat sink.
2. Please place the input capacitors for VIN and VCNTL pins near the pins as close as possible for decoupling high-frequency ripples.
3. Ceramic decoupling capacitors for load must be placed near the load as close as possible for decoupling high-frequency ripples.
4. To place RS3235 and output capacitors near the load reduces parasitic resistance and inductance for excellent load transient response.
5. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
6. Large current paths, shown by bold lines on the figure 23, must have wide tracks.
7. Place the R1, R2, and C1 near the RS3235 as close as possible to avoid noise coupling.
8. Connect the ground of the R2 to the GND pin by using a dedicated track.
9. Connect the one pin of the R1 to the load for Kelvin sensing.

10.2 Layout Example

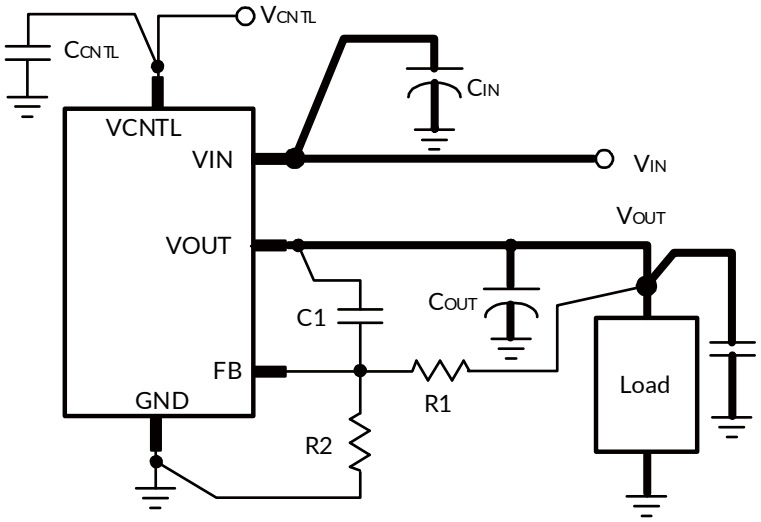
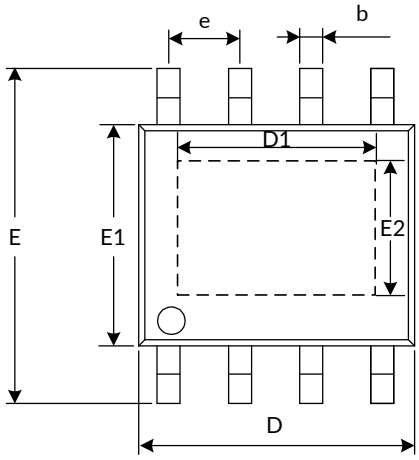
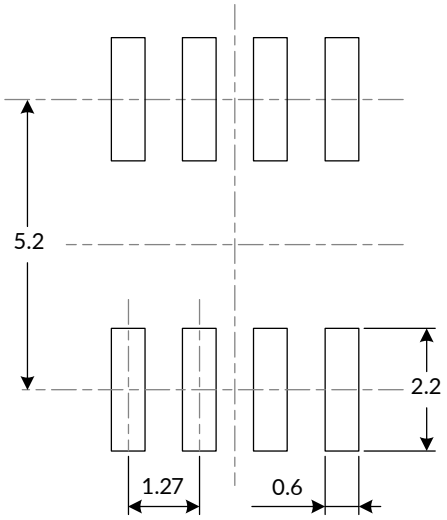


Figure 23. Layout Example

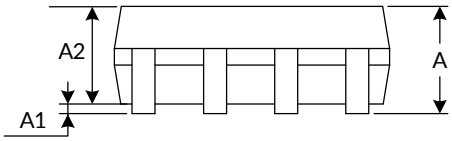
11 PACKAGE OUTLINE DIMENSIONS

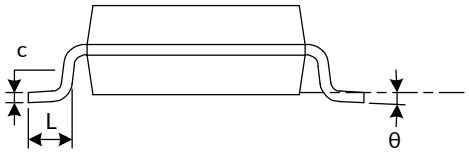
ESOP8 (4)





RECOMMENDED LAND PATTERN (Unit: mm)



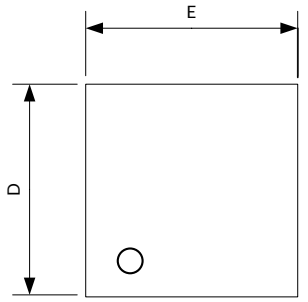


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.650		0.065
A1	0.050	0.150	0.002	0.006
A2	1.300	1.500	0.051	0.059
b	0.390	0.470	0.015	0.019
c	0.200	0.240	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270 (BSC) (2)		0.050 (BSC) (2)	
D1 (1)	2.090 (REF) (3)		0.082 (REF) (3)	
E2	2.090 (REF) (3)		0.082 (REF) (3)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.500	0.800	0.019	0.032
θ	0°	8°	0°	8°

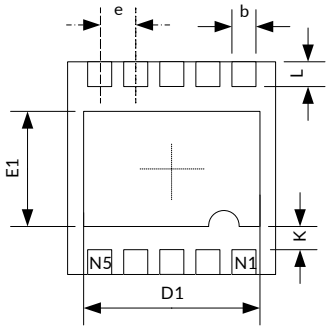
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

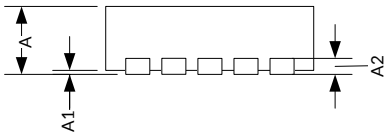
DFN3x3-10L (2)



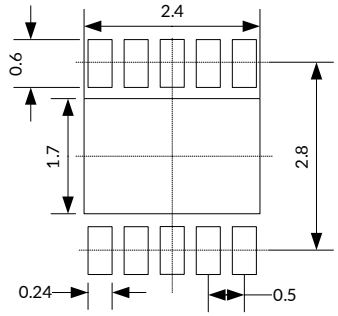
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203		0.008	
b	0.180	0.300	0.007	0.012
D (1)	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E (1)	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
e	0.500 TYP		0.020 TYP	
k	0.200 MIN		0.008 MIN	
L	0.300	0.500	0.012	0.020

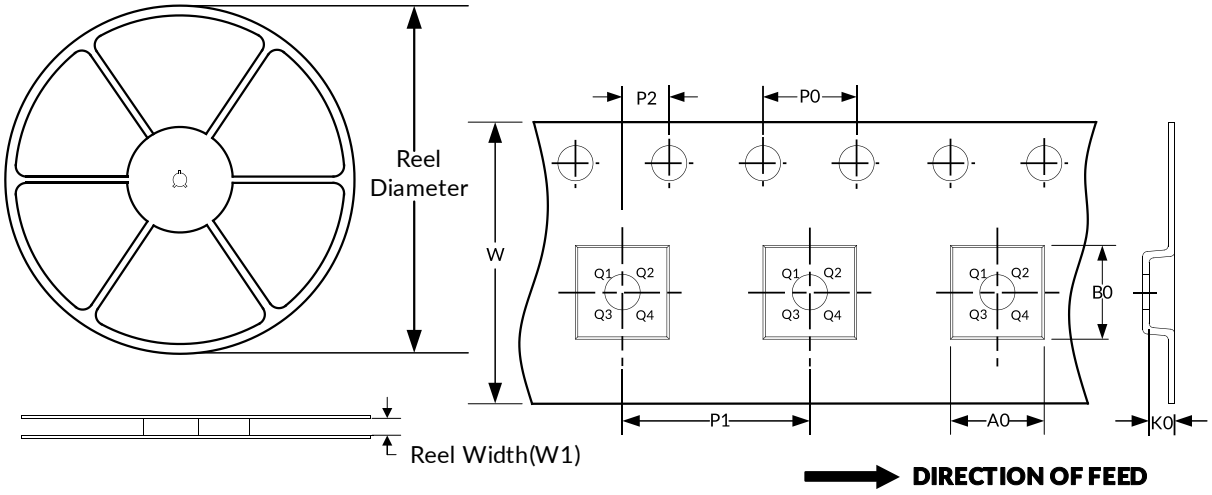
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
DFN3x3-10L	13”	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1
ESOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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