

TS74230L - 30W CW GaN Broadband RF Switch SPDT

1.0 Features

- Low insertion loss: 0.40dB @ 800MHz
- High isolation: 43dB @ 800MHz
- High linear power handling capability
- Versatile 2.6-5.5V Vdd power supply
- Vcp supply of -18V
- 43dBm Hot Switching Capable

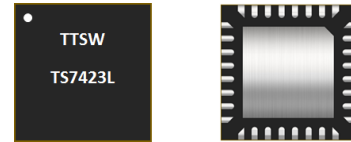


Figure 1 Device Image
(32 Pin 4x4x0.8mm QFN Package)

2.0 Applications

- Private Mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells



RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS74230L is a symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 1MHz to 3GHz makes the TS74230L an excellent switch for all the applications requiring low insertion loss, high isolation and high linearity within a small package size. This part has the internal charge pump disabled to eliminate the charge pump spurs. A -17 to -18V supply is needed on the VCP pin.

The TS74230L is packaged into a compact Quad Flat No lead (QFN) 4x4mm 32 leads plastic package.

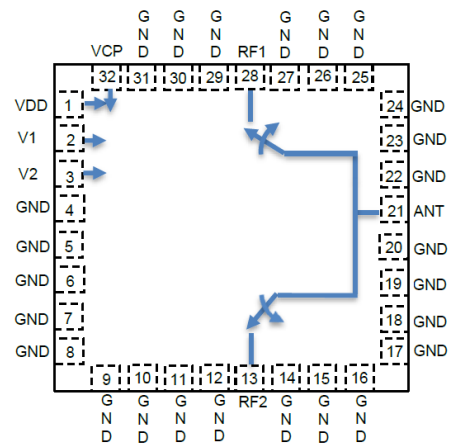


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

| Base Part Number | Package Type | Form | Qty | Reel Diameter | Reel Width | Orderable Part Number |
|------------------|----------------------|---------------|------|---------------|------------|-----------------------|
| TS74230L | 32 Pin 4x4x0.8mm QFN | Tape and Reel | 3000 | 13" (330mm) | 18mm | TS74230LMTRPBF |
| Evaluation Board | | | | | | TS74230L-EVB |

5.0 Pin Description

Table 2 Pin Definition

| Pin Number | Pin Name | Description |
|--|----------|---|
| 1 | VDD | DC power supply |
| 2 | V1 | Switch control input 1 |
| 3 | V2 | Switch control input 2 |
| 4,5,6,7,8,9,10,11,12,14,15,16,17,18,19,20,22,23,24,25,26,27,29,30,31 | NC | No internal connection, Can be grounded |
| 13 | RF2 | RF port 2 |
| 21 | ANT | Antenna port |
| 28 | RF1 | RF port 1 |
| 32 | VCP | Negative Voltage Supply, -17 to -18V |

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @ $T_A=+25^{\circ}\text{C}$ Unless Otherwise Specified

| Parameter | Symbol | Value | Unit |
|--|-----------------|--------------|-----------------------------|
| Electrical Ratings | | | |
| Power Supply Voltage Vdd | VDD | 2.6 to 5.5 | V |
| Charge Pump Voltage Vcp | Vcp | -15 to -19 | V |
| Storage Temperature Range | T_{st} | -55 to +125 | $^{\circ}\text{C}$ |
| Operating Temperature Range | T_{op} | -40 to +85 | $^{\circ}\text{C}$ |
| Maximum Junction Temperature | T_J | +140 | $^{\circ}\text{C}$ |
| RF Input Power CW, 20-3000MHz, $T_C=+85^{\circ}\text{C}$ | RFx | 45 | dBm |
| RF Input Power (VSWR 10:1), 1 minute | RFx | 44 | dBm |
| Thermal Ratings | | | |
| Thermal Resistance (junction-to-case) – Bottom side | $R_{\theta JC}$ | 10 | $^{\circ}\text{C}/\text{W}$ |
| Thermal Resistance (junction-to-top) | $R_{\theta JT}$ | ≤ 37 | $^{\circ}\text{C}/\text{W}$ |
| Soldering Temperature | T_{SOLD} | 260 | $^{\circ}\text{C}$ |
| ESD Ratings | | | |
| Human Body Model (HBM) | Level 1B | 500 to <1000 | V |
| Charged Device Model (CDM) | Level C3 | ≥ 1000 | V |
| Moisture Rating | | | |
| Moisture Sensitivity Level | MSL | 1 | - |

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @ $T_A=+25^\circ\text{C}$ Unless Otherwise Specified; $V_{DD}=+2.7\text{V}$; $V_{CP}= -18\text{V}$; 50Ω Source/Load.

| Parameter | Condition | Minimum | Typical | Maximum | Unit |
|--------------------------|---|---------|---------|---------|---------------|
| Operating Frequency | | 1 | | 3000 | MHz |
| Insertion Loss, RFx | 400MHz | | 0.35 | | dB |
| | 800MHz | | 0.40 | 0.5 | |
| | 1.95GHz | | 0.45 | 0.6 | |
| | 2.6GHz | | 0.50 | 0.7 | |
| Isolation, ANT-RFx | 400MHz | | 50 | | dB |
| | 800MHz | 40 | 43 | | |
| | 1.95GHz | 32 | 34 | | |
| | 2.6GHz | 28 | 30 | | |
| Return Loss, ANT-RFx | 400MHz | | 30 | | dB |
| | 800MHz | | 28 | | |
| | 1.95GHz | | 25 | | |
| | 2.6GHz | | 25 | | |
| H2 | 800MHz, Pin=40dBm | | -83 | | dBc |
| H3 | 800MHz, Pin=40dBm | | -81 | | dBc |
| IIP3 | 800MHz | | 74 | | dBm |
| P0.1dB ^[1] | 0.1dB compression point, 20MHz - 3GHz | | 46 | | dBm |
| P0.1dB ^[1] | 0.1dB compression point, 1 - 10MHz | | 43.5 | | dBm |
| Switching Time | 50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3) | | 2.0 | | μs |
| Control Voltage | Power supply VDD | 2.6 | 3.3 | 5.5 | V |
| | Charge Pump Supply Voltage VCP | -19 | -18 | -15 | V |
| | All control pins high, V_{ih} | 1.0 | 3.3 | 5.25 | V |
| | All control pins low, V_{il} | -0.3 | | 0.5 | V |
| Control Current | All control pins low, I_{il} | | 0 | | μA |
| | All control pins high, I_{ih} | | | 7.5 | μA |
| Current Consumption, IDD | Active mode | | 160 | 200 | μA |

Note: [1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

| V1 | V2 | Active RF Path |
|----|----|----------------|
| 0 | 1 | All OFF |
| 0 | 0 | ANT-RF1 |
| 1 | 0 | ANT-RF2 |

Bias Sequence:

- [1] VDD should be applied first before VCP. Minimum time between VDD and VCP should be 50usec.
- [2] Vc can be applied/toggled after VCP voltage has settled.

9.0 Evaluation Board Schematic

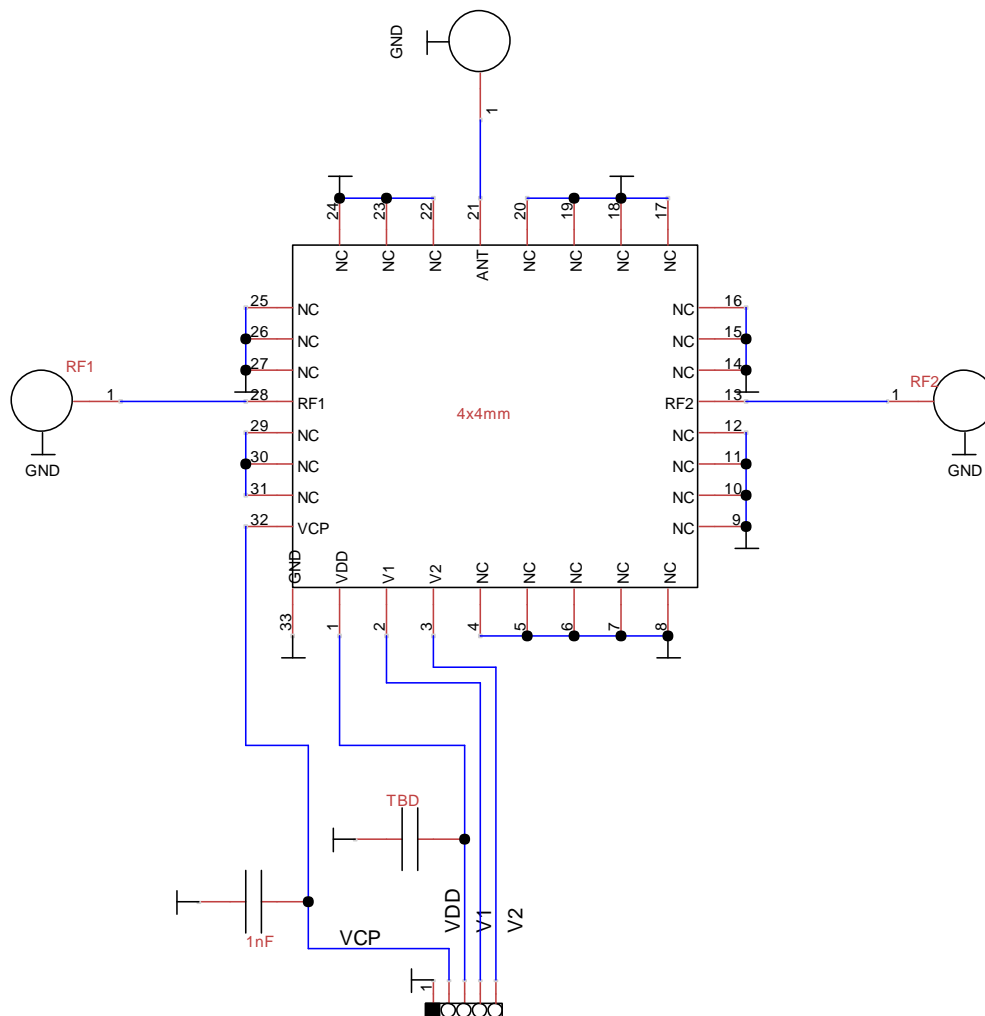


Figure 3 Evaluation Board Schematic

Attention:

- [1] 33 refers to the center pad of the device which is ground.
- [2] -17/-18V needed on VCP pin.

10.0 Typical Characteristics

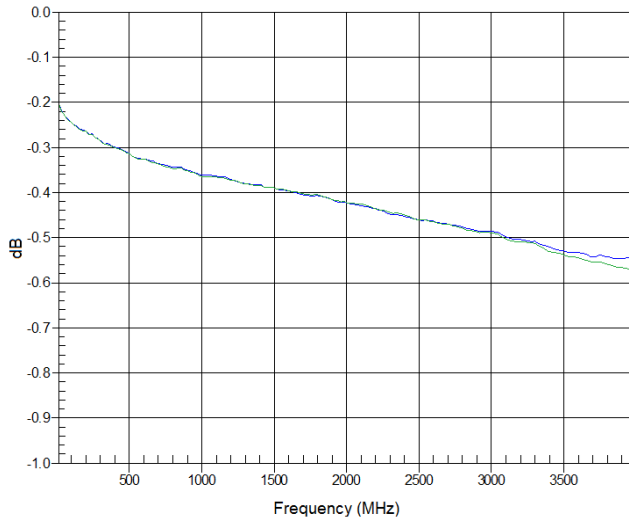


Figure 4 RF1, RF2 Insertion Loss

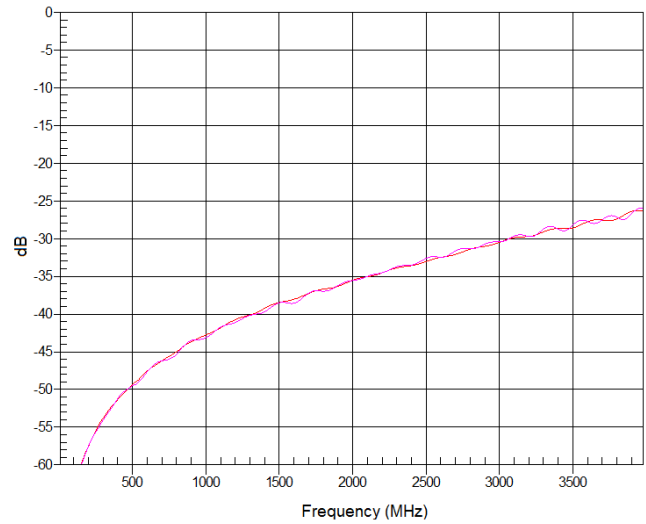


Figure 5 RF1, RF2 Isolation

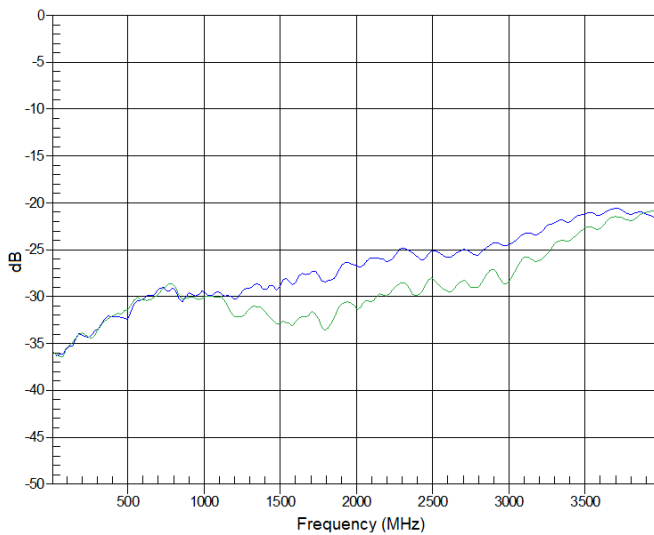


Figure 6 RF1, RF2 Return Loss

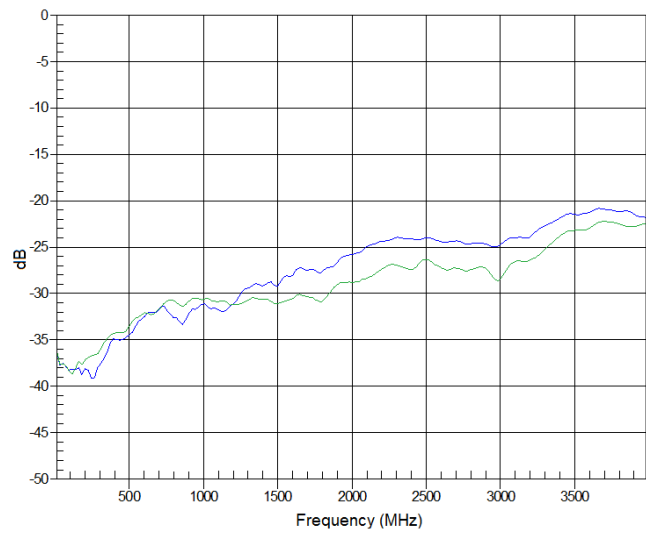


Figure 7 ANT Return Loss

11.0 Device Package Information

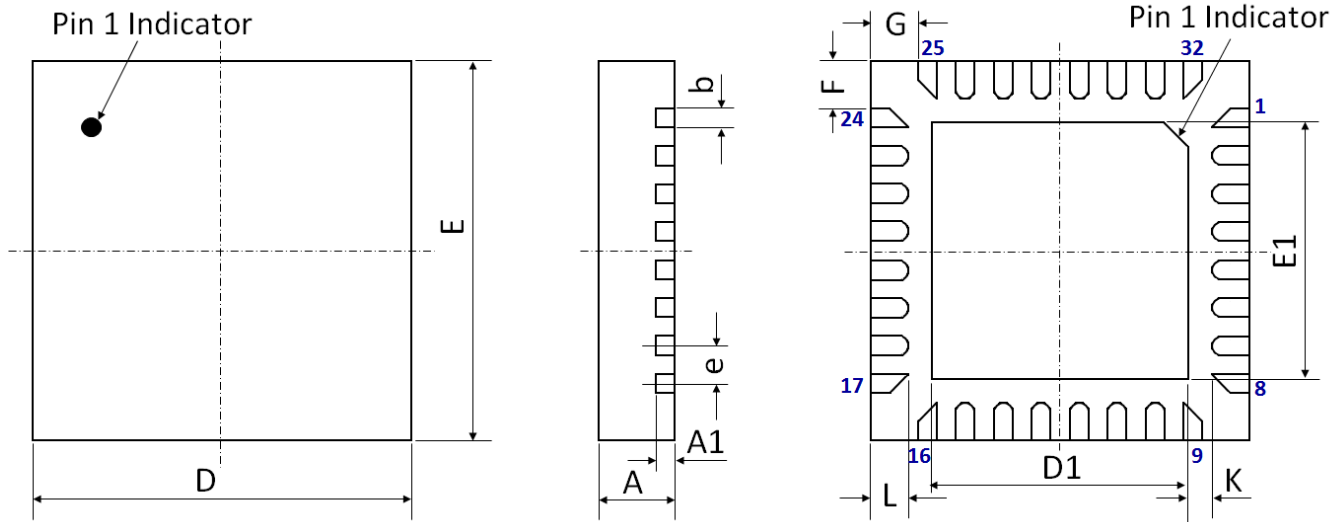


Figure 8 Device Package Drawing
(All dimensions are in mm)

Table 6 Device Package Dimensions

| Dimension (mm) | Value (mm) | Tolerance (mm) | Dimension (mm) | Value (mm) | Tolerance (mm) |
|----------------|------------|----------------|----------------|------------|----------------|
| A | 0.80 | ±0.05 | E | 4.00 BSC | ±0.05 |
| A1 | 0.203 | ±0.02 | E1 | 2.70 | ±0.05 |
| b | 0.20 | +0.05/-0.07 | F | 0.50 | ±0.05 |
| D | 4.00 BSC | ±0.05 | G | 0.50 | ±0.05 |
| D1 | 2.70 | ±0.05 | L | 0.40 | ±0.05 |
| e | 0.40 BSC | ±0.05 | K | 0.25 | ±0.05 |

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:

Please refer to application notes [TN-001](#) and [TN-002](#) at <http://www.tagoretech.com> for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:

- [1] 4 layer PCB is recommended.
- [2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- [3] Thermal vias shall only be placed on the center pad.
- [4] The maximum via number for the center pad is $6(X) \times 6(Y) = 36$.

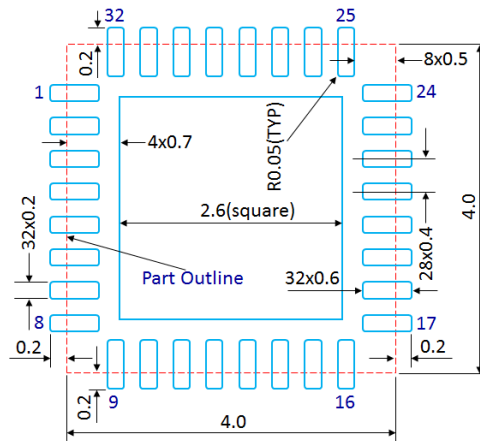


Figure 9 PCB Land Pattern
(Dimensions are in mm)

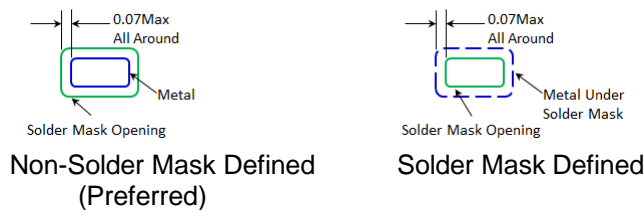


Figure 10 Solder Mask Pattern
(Dimensions are in mm)

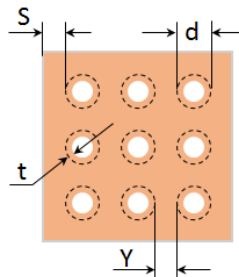


Figure 11 Thermal Via Pattern

(Recommended Values: $S \geq 0.15\text{mm}$; $Y \geq 0.20\text{mm}$; $d = 0.2\text{mm}$; Plating Thickness $t = 25\mu\text{m}$ or $50\mu\text{m}$)

13.0 PCB Stencil Design

Guidelines:

- [1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- [2] Stencil thickness is recommended to be 125µm.

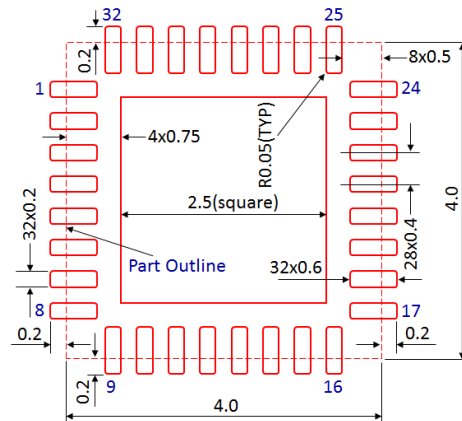


Figure 12 Stencil Openings
(Dimensions are in mm)

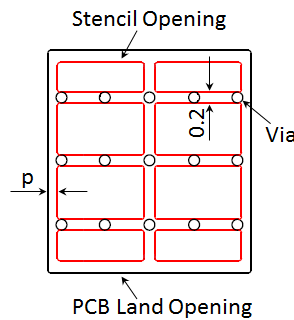


Figure 13 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

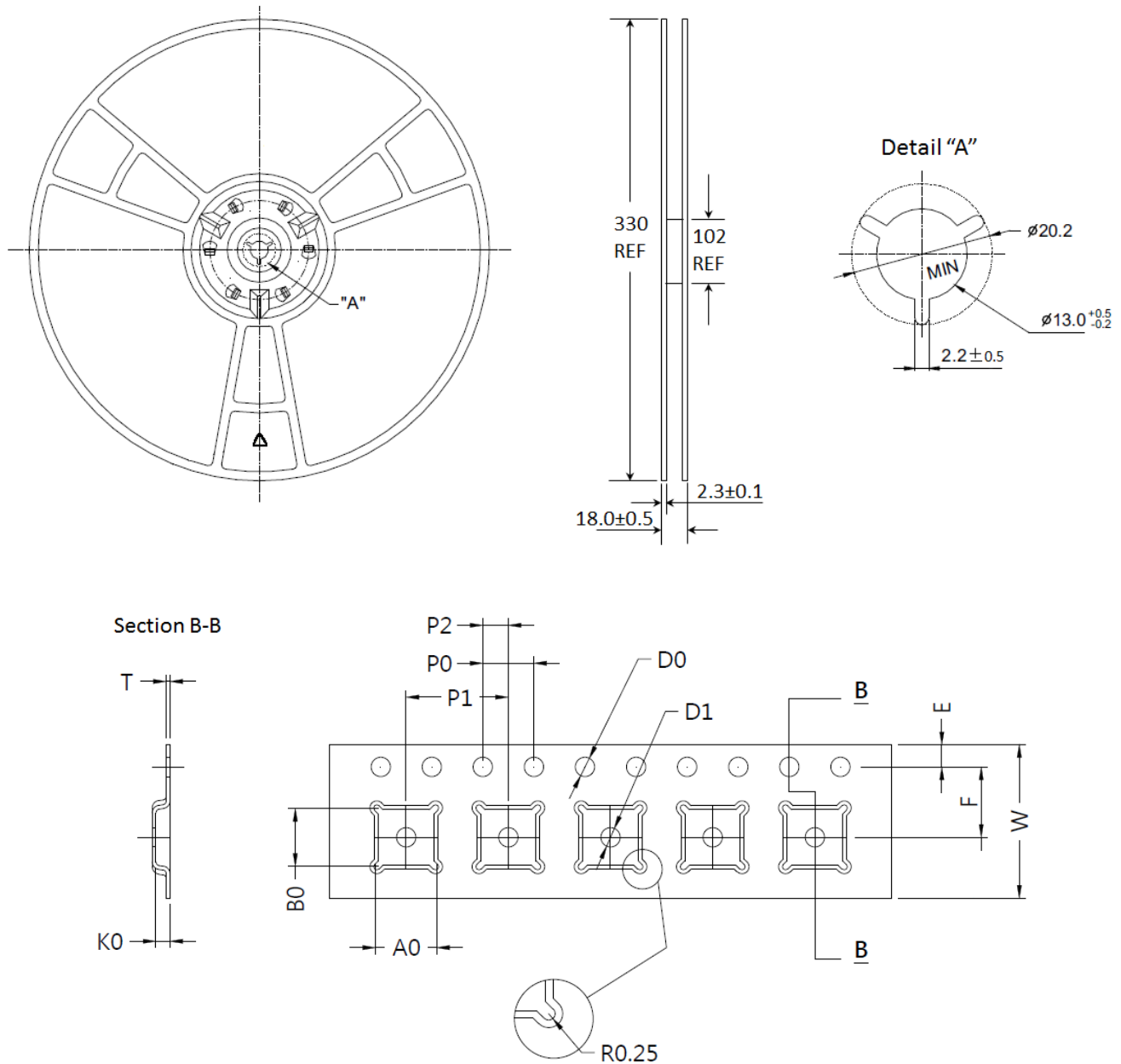


Figure 14 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

| Dimension (mm) | Value (mm) | Tolerance (mm) | Dimension (mm) | Value (mm) | Tolerance (mm) |
|----------------|------------|----------------|----------------|------------|----------------|
| A0 | 4.35 | ±0.10 | K0 | 1.10 | ±0.10 |
| B0 | 4.35 | ±0.10 | P0 | 4.00 | ±0.10 |
| D0 | 1.50 | +0.10/-0.00 | P1 | 8.00 | ±0.10 |
| D1 | 1.50 | +0.10/-0.00 | P2 | 2.00 | ±0.05 |
| E | 1.75 | ±0.10 | T | 0.30 | ±0.05 |
| F | 5.50 | ±0.05 | W | 12.00 | ±0.30 |

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