

Ultra low current consumption SPDT switch

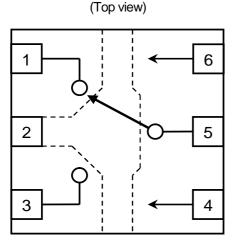
■FEATURES

- Low control voltage 1.6 V min.
- Low current consumption 0.1 µA typ.
- Low insertion loss
 0.45 dB typ. @ f = 920 MHz
 0.50 dB typ. @ f = 2.4 to 2.5 GHz
- High isolation
 30 dB typ. @ f = 920 MHz
 22 dB typ. @ f = 2.4 to 2.5 GHz
- High linearity
 - P_{-0.1dB} = +30 dBm typ. @ f = 920 MHz, 2.4 to 2.5 GHz
- Small package 1.0 mm x 1.0 mm, t = 0.375 mm
- RoHS compliant and Halogen Free, MSL1

■APPLICATION

- LPWA (SIGFOX, LoRaWAN, Wi-SUN) applications
- 2.4 GHz Wireless LAN (802.11b/g/n/ax), Bluetooth
- •Antenna switching, path switching, general purpose switching applications

BLOCK DIAGRAM (DFN6-75)



■GENERAL DESCRIPTION

The NJG1816K75 is a 2-bit control SPDT switch with 0.1 μ A ultra-low current consumption.

The NJG1816K75 features high linearity and low insertion loss at 1.8 V operating voltage up to 3 GHz. This switch is suitable for wireless communication devices with low power consumption such as wearable and mobile terminals.

The small and thin package of DFN6-75 offers small mounting area.

■FUNCTIONAL DESCRIPTION

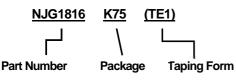
"H" = V_{CTL}(H), "L" = V_{CTL}(L)

| ON Path | VCTL1 | VCTL2 |
|---------|-------|-------|
| PC-P1 | L | Н |
| PC-P2 | Н | L |

■PIN CONFIGURATION

| PIN NO. | SYMBOL | DESCRIPTION |
|---------|---------|----------------------------------|
| 1 | P1 | RF terminal |
| 2 | NC(GND) | Ground terminal |
| 3 | P2 | RF terminal |
| 4 | VCTL2 | Control signal input terminal |
| 5 | PC | RF terminal |
| 6 | VCTL1 | Control signal input terminal |

■ PRODUCT NAME INFORMATION



ORDERING INFORMATION

| PART NUMBER | PACKAGE OUTLINE | RoHS | HALOGEN- FREE | TERMINAL FINISH | MARKING | WEIGHT (mg) | MOQ (pcs.) |
|-------------|--------------------|------|------------------|--------------------|---------|----------------|------------|
| NJG1816K75 | DFN6-75 | Yes | Yes | Ni/Pd/Au | 5 | 1.2 | 5,000 |

ABSOLUTE MAXIMUM RATINGS

| $T_a = 25^{\circ}C, \ Z_s = Z_i$ | | | | |
|----------------------------------|------------------|-------------|------|--|
| PARAMETER | SYMBOL | RATINGS | UNIT | |
| RF input power ⁽¹⁾ | P _{IN} | +30 | dBm | |
| Control voltage | V _{CTL} | 4.5 | V | |
| Power dissipation ⁽²⁾ | PD | 380 | mW | |
| Operating temperature | T _{opr} | -40 to +105 | °C | |
| Storage temperature | T _{stg} | -55 to +150 | °C | |

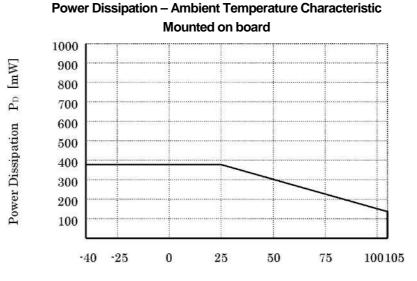
(1): $V_{CTL}(L) = 0 V$, $V_{CTL}(H) = 1.8 V$, on state port

(2): Mounted on four-layer FR4 PCB with through-hole (76.2 \times 114.3 mm), T_j = 150 °C

■ POWER DISSIPATION VS.AMBIENT TEMPERATURE

Please, refer to the following Power Dissipation and Ambient Temperature.

(Please note the surface mount package has a small maximum rating of Power Dissipation $[P_D]$, a special attention should be paid in designing of thermal radiation.)



Ambient Temperature Ta [°C]

■ ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

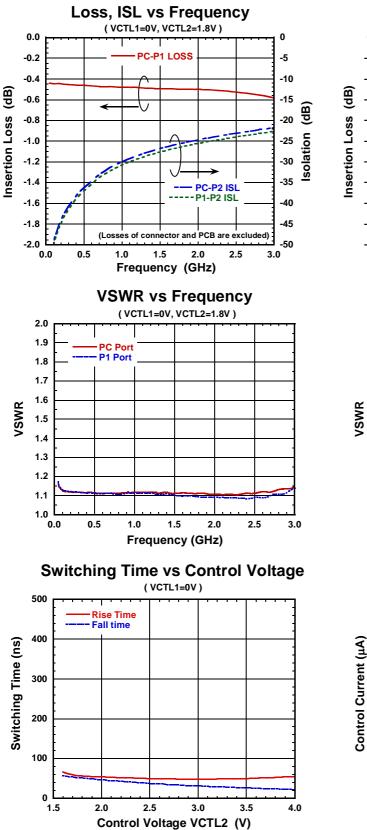
| $V_{CTL}(H) = 1.8 \text{ V}, V_{CTL}(L) = 0 \text{ V}, T_a = 25^{\circ}\text{C}, Z_s = Z_l = 50 \Omega$, with application circuit | | | | | | |
|--|----------------------|-----------------------|------|------|------|------|
| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
| Control voltage (HIGH) | Vctl(H) | VCTL1, VCTL2 terminal | 1.6 | 1.8 | 4.0 | V |
| Control voltage (LOW) | V _{CTL} (L) | VCTL1, VCTL2 terminal | -0.2 | - | 0.2 | V |
| Control current | ICTL | | - | 0.1 | 2.0 | μΑ |

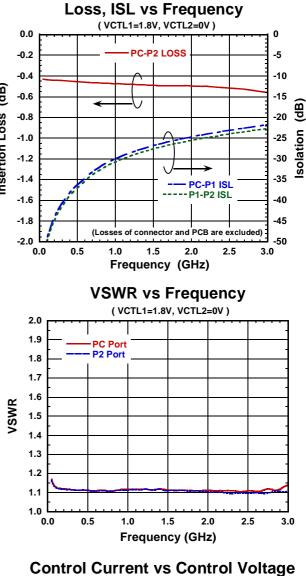
■ ELECTRICAL CHARACTERISTICS (RF CHARACTERISTICS)

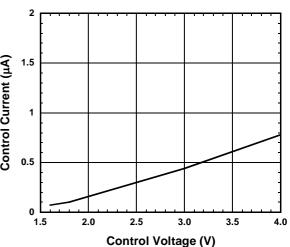
VCTL(H) = 1.8 V, VCTL(L) = 0 V, Ta = 25°C, Zs = ZI = 50 Ω , with application circuit

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------------------|---------|------------------------|------|------|------|-------|
| Insertion loss | LOSS | f = 920 MHz | - | 0.45 | 0.65 | ٩D |
| Insertion loss | 1033 | f = 2.4 to 2.5 GHz | - | 0.50 | 0.70 | dB |
| lociation | | f = 920 MHz | 26 | 30 | - | ٩D |
| Isolation | ISL | f = 2.4 to 2.5 GHz | 18 | 22 | - | dB |
| Input power at 0.1 dB | P-0.1dB | f = 920 MHz | +25 | +30 | - | dDaa |
| compression point | | f = 2.4 to 2.5 GHz | +25 | +30 | - | dBm |
| Input power at 1 dB | P-1dB | f = 920 MHz | +28 | +30 | - | dBm |
| compression point | | f = 2.4 to 2.5 GHz | +28 | +30 | - | UDITI |
| | | f = 920 MHz | - | 1.1 | 1.4 | |
| VSWR | VSWR | f = 2.4 to 2.5 GHz | - | 1.2 | 1.4 | - |
| Switching time | Tsw | 50% Vcr∟ to 10%/90% RF | - | 100 | 300 | ns |

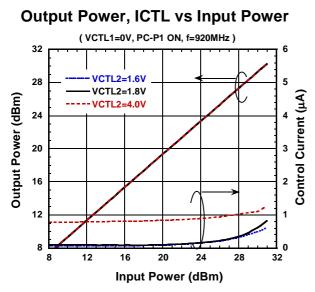
ELECTRICAL CHARACTERISTICS



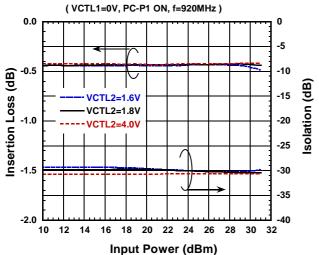




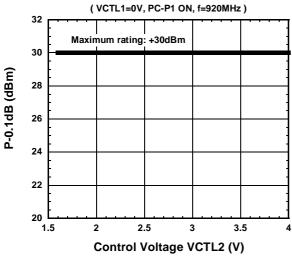
■ ELECTRICAL CHARACTERISTICS



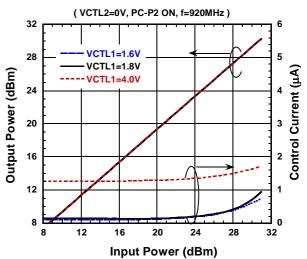
Insertion Loss, Isolation vs Input Power



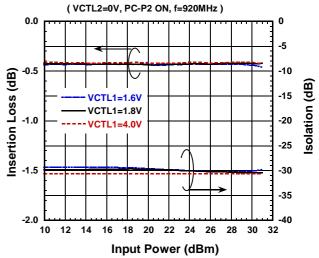




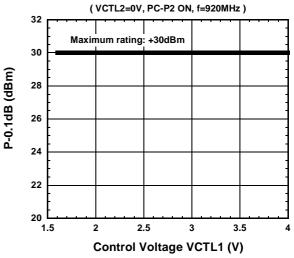
Output Power, ICTL vs Input Power



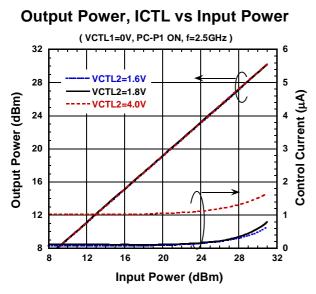
Insertion Loss, Isolation vs Input Power



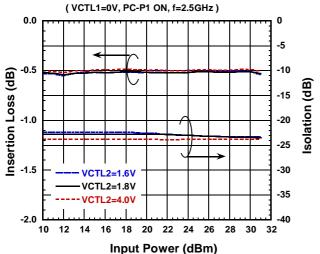
P-0.1dB vs Control Voltage



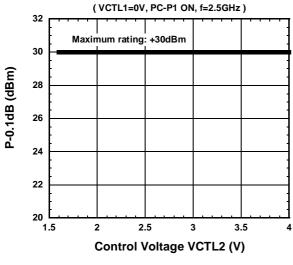
■ ELECTRICAL CHARACTERISTICS



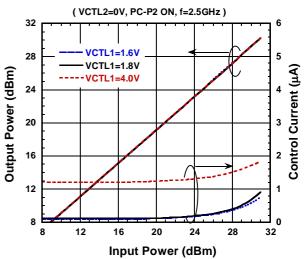
Insertion Loss, Isolation vs Input Power



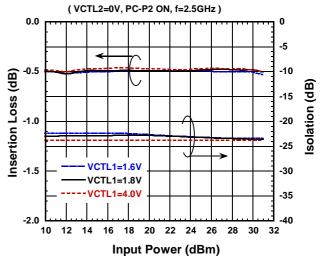




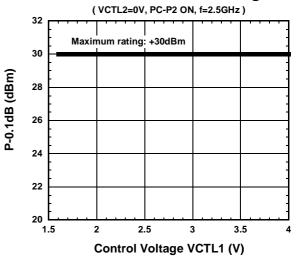




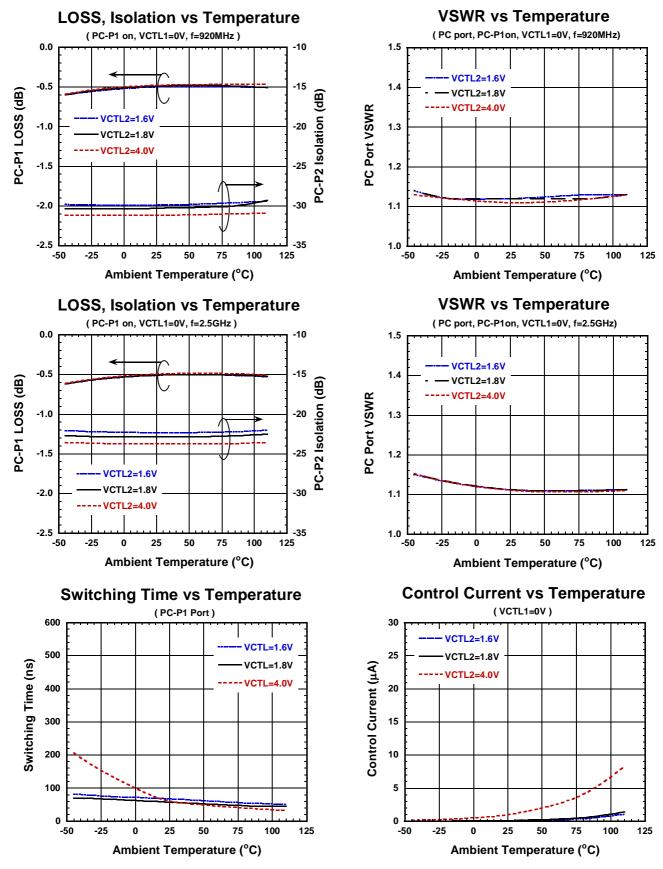
Insertion Loss, Isolation vs Input Power



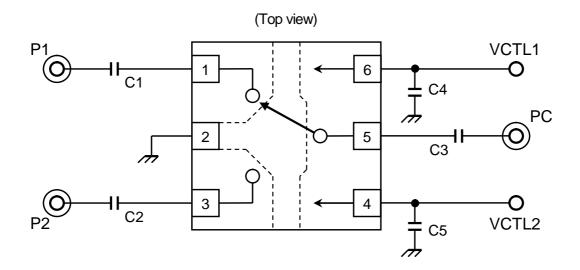
P-0.1dB vs Control Voltage



■ ELECTRICAL CHARACTERISTICS



■ APPLICATION CIRCUIT



■ PARTS LIST

| Part ID | Value | Notes |
|----------|---------|----------------|
| C1 to C3 | 1000 pF | MURATA (GRM03) |
| C4 to C5 | 10 pF | MURATA (GRM03) |

NJG1816K75

P2

PC

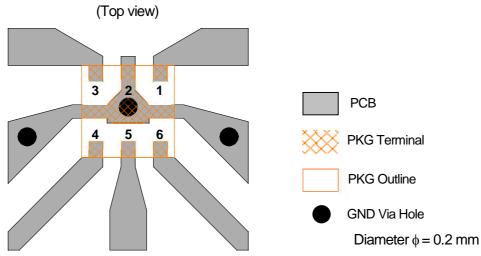
| Losses of PCB and connectors | Ta – +25℃ |
|-------------------------------|--------------------------|
| LUSSES OF FUD and CONTRECIONS | , 1a = 1 25 C |

| Frequency (MHz) | Loss (dB) |
|-----------------|-----------|
| 920 | 0.22 |
| 2400 | 0.42 |
| 2500 | 0.42 |

PCB: FR-4 t = 0.2 mm MICROSTRIP LINE WIDTH: 0.4 mm (Zo = 50 Ω) PCB SIZE: 19.4 x 14.0 mm

■ PCB LAYOUT GUIDELINE

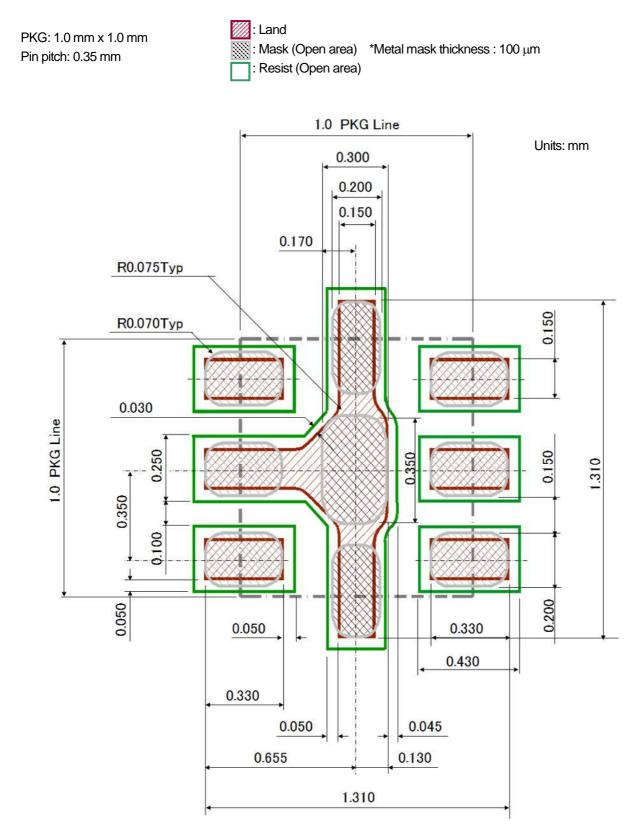
EVALUATION BOARD



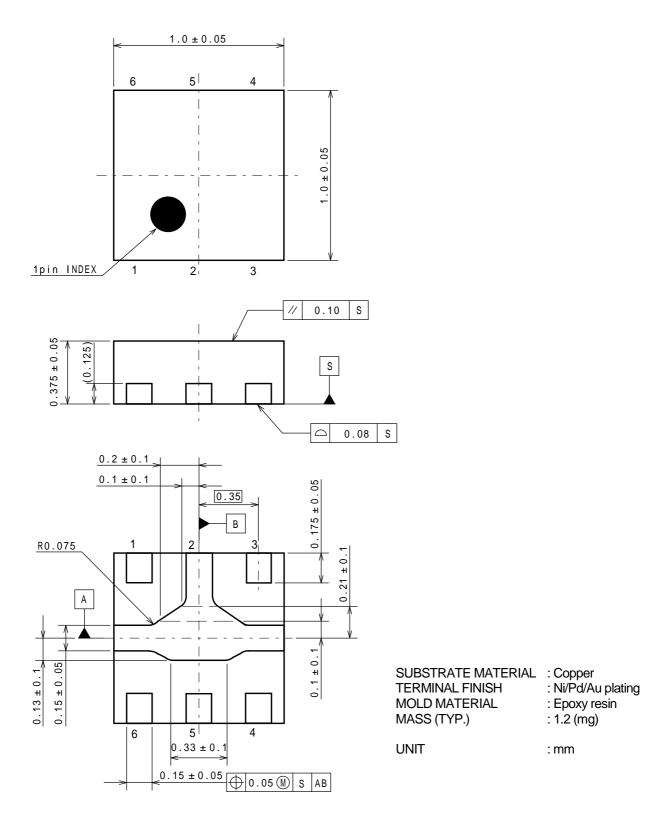
■ PRECAUTIONS

- [1] The DC blocking capacitors (C1, C2, C3) should be placed at RF terminals. Please choose appropriate capacitance value at the application frequency.
- [2] For avoiding the degradation of RF performance, the bypass capacitors (C4, C5) should be placed as close as possible to VCTL terminals.
- [3] For good RF performance, exposed pad should be connected to PCB ground plane of substrate, and through –holes should be placed near the IC.

■ RECOMMENDED FOOTPRINT PATTERN (DFN6-75)

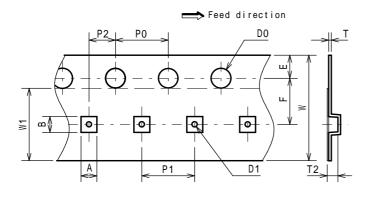


■ PACKAGE OUTLINE (DFN6-75)



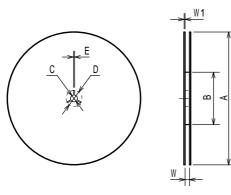
■ PACKING SPECIFICATION (DFN6-75)

TAPING DIMENSIONS



| SYMBOL | DIMENSION | REMARKS |
|--------|--------------------------------|--------------------|
| А | 1.19 ^{+0:04} | BOTTOM DIMENSION |
| В | 1.19 ^{+0.04} -0.01 | BOTTOM DIMENSION |
| DO | 1.5 ^{+0.1} | |
| D1 | 0.5±0.05 | |
| E | 1.75±0.1 | |
| F | 3.5 ± 0.05 | |
| P0 | 4.0±0.1 | |
| P1 | 4.0 ± 0.1 | |
| P2 | 2.0±0.05 | |
| Т | 0.18 ± 0.05 | |
| T2 | 0.69 ± 0.1 | |
| W | 8.0±0.1 | |
| W1 | 5.5 ± 0.1 | THICKNESS 60 µ max |

REEL DIMENSIONS

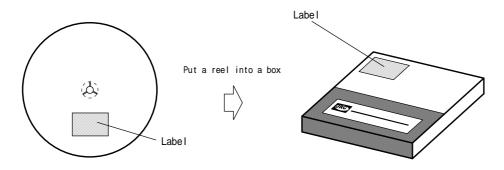


| SYMBOL | DIMENSION |
|--------|--------------------|
| Α | 180 _ ₃ |
| В | 60 ⁺¹ |
| С | 13 ± 0.2 |
| D | 21 ± 0.8 |
| E | 2±0.5 |
| W | 9±0.3 |
| W1 | 1.2 |

TAPING STATE

| Insert | direction | Sealing with covering tape | > | |
|--------|------------------------|----------------------------|--------------|---------------|
| | | | | |
| | Empty tape | Devices | Empty tape | Covering tape |
| Feed | direction 150 to 200mm | 5000pcs/reel | 150 to 200mm | 600 to 800mm |

PACKING STATE



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 - 8-1. Quality Warranty Period

In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.

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When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.

- Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
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With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.

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