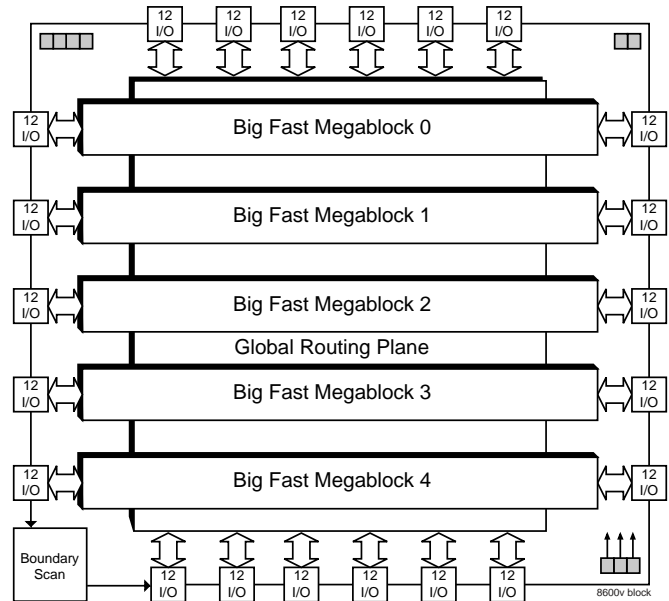


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## Features

- **SuperBIG HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - 3.3V Power Supply
  - 32,000 PLD Gates/600 Macrocells
  - 192-264 I/O Pins Supporting 3.3V/2.5V I/O
  - 864 Registers
  - High-Speed Global and Big Fast Megablock (BFM) Interconnect
  - Wide 20-Macrocell Generic Logic Block (GLB) for High Performance
  - Wide Input Gating (44 Inputs per GLB) for Fast Counters, State Machines, Address Decoders, Etc.
  - PCB-Efficient Ball Grid Array (BGA) Package Options
- **HIGH-PERFORMANCE E<sup>2</sup>CMOS<sup>®</sup> TECHNOLOGY**
  - $f_{max} = 125$  MHz Maximum Operating Frequency
  - $t_{pd} = 8.5$  ns Propagation Delay
  - Electrically Erasable and Reprogrammable
  - Non-Volatile
  - Programmable Speed/Power Logic Path Optimization
- **IN-SYSTEM PROGRAMMABLE**
  - Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - Reprogram Soldered Devices for Faster Debugging
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE AND 3.3V IN-SYSTEM PROGRAMMABLE**
- **ARCHITECTURE FEATURES**
  - Enhanced Pin-Locking Architecture, Symmetrical Generic Logic Blocks Connected by Hierarchical Big Fast Megablock and Global Routing Planes
  - Product Term Sharing Array Supports up to 28 Product Terms per Macrocell Output
  - Macrocells Support Concurrent Combinatorial and Registered Functions
  - Embedded Tristate Bus Can Be Used as an Internal Tristate Bus or as an Extension of an External Tristate Bus
  - Macrocell and I/O Registers Feature Multiple Control Options, Including Set, Reset and Clock Enable
  - I/O Pins Support Programmable Bus Hold, Pull-Up, Open-Drain and Slew Rate Options
  - Separate VCCIO Power Supply to Support 3.3V or 2.5V Input/Output Logic Levels
  - I/O Cell Register Programmable as Input Register for Fast Setup Time or Output Register for Fast Clock to Output Time

## Functional Block Diagram



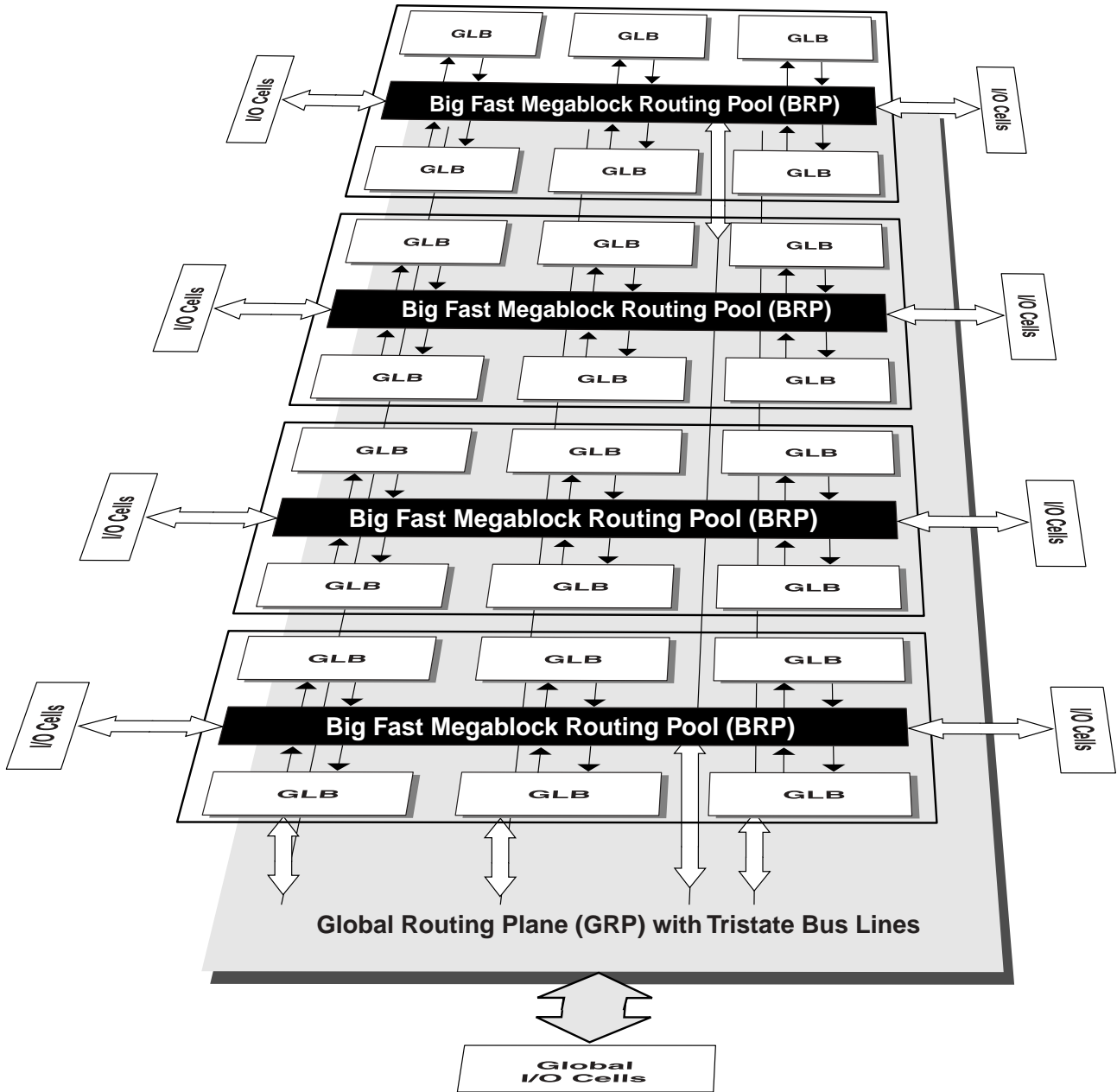
## ispLSI 8000V Family Description

The ispLSI 8000V Family of Register-Intensive, 3.3V SuperBIG In-System Programmable Logic Devices is based on Big Fast Megablocks of 120 registered macrocells and a Global Routing Plane (GRP) structure interconnecting the Big Fast Megablocks. Each Big Fast Megablock contains 120 registered macrocells arranged in six groups of 20, a group of 20 being referred to as a Generic Logic Block, or GLB. Within the Big Fast Megablock, a Big Fast Megablock Routing Pool (BRP) interconnects the six GLBs to each other and to 24 Big Fast Megablock I/O cells with optional I/O registers. The Global Routing Plane which interconnects the Big Fast Megablocks has additional global I/Os with optional I/O registers. The 192-I/O version contains 72 Big Fast Megablock I/O and 120 global I/O, while the 264-I/O version contains 120 Big Fast Megablock I/O and 144 global I/O.

Outputs from the GLBs in a Big Fast Megablock can drive both the Big Fast Megablock Routing Pool within the Big Fast Megablock and the Global Routing Plane between the Big Fast Megablocks. Switching resources are provided to allow signals in the Global Routing Plane to drive any or all the Big Fast Megablocks in the device. This

**Functional Block Diagram**

Figure 1. ispLSI 8600V Functional Block Diagram (Perspective)



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## ispLSI 8000V Family Description (Continued)

mechanism allows fast, efficient connections, both within the Big Fast Megablocks and between them.

Each GLB contains 20 macrocells and a fully populated, programmable AND-array with 82 logic product terms. The GLB has 44 inputs from the Big Fast Megablock Routing Pool which are available in both true and complement form for every product term. Up to 20 of these inputs can be switched to provide local feedback into the GLB for logic functions that require it. The 80 general-purpose product terms can be grouped into 20 sets of four and sent into a Product Term Sharing Array (PTSA) which allows sharing up to a maximum of 28 product terms for a single function. Alternatively, the PTSA can be bypassed for functions of four product terms or less.

The 20 registered macrocells in the GLB are driven by the 20 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. Each macrocell has two outputs, one output can be fed back inside the GLB to the AND-array, while the other output drives both the Big Fast Megablock Routing Pool and the Global Routing Plane. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function.

Macrocell registers can be clocked from one of several global, local or product term clocks available on the device. A global, local and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The polarity of all of these control signals is selectable on an individual macrocell basis. The macrocell register can be programmed to operate as a D-type register, a D-type flow-through latch or a T-type flip flop.

The 20 outputs from the GLB can drive both the Big Fast Megablock Routing Pool within the Big Fast Megablock and the Global Routing Plane between the Big Fast Megablocks. The Big Fast Megablock Routing Pool contains general purpose tracks which interconnect the six GLBs within the Big Fast Megablock and dedicated tracks for the signals from the Big Fast Megablock I/O cells. The Global Routing Plane contains general purpose tracks that interconnect the Big Fast Megablocks and also carry the signals from the I/Os connected to the Global Routing Plane.

Control signals for the I/O cell registers are generated using an extra product term within each GLB, or using dedicated input pins. Each GLB has two extra product terms beyond the 80 available for the macrocell logic. The first additional product term is used as an optional shared product term clock for all the macrocells within the GLB. The second additional product term is then routed to an I/O Control Bus using a separate routing structure from the Big Fast Megablock Routing Pool and Global Routing Plane. Use of a separate control bus routing structure allows the I/O registers to have many control signals with no impact on the interconnection of the GLBs and Big Fast Megablocks. The I/O Control Bus is split into four quadrants, each servicing the I/O cell control requirements for one edge of the device. Signals in the control bus can be independently selected by any or all I/O cells to act as clock, clock enable, output enable, reset or preset.

Each Big Fast Megablock has 24 I/O cells. The Global Routing Pool has 144 I/O cells. Each I/O cell can be configured as a combinatorial input, combinatorial output, registered input, registered output or bidirectional I/O. I/O cell registers can be clocked from one of several global, local or product term clocks which are selected from the I/O control bus. A global and product term clock enable is also provided, eliminating the need for the user to gate the clock to the I/O cell registers. Reset and preset for the I/O cell register is provided from both global and product term signals. The polarity of all of these control signals is selectable on an individual I/O cell basis. The I/O cell register can be programmed to operate as a D-type register or a D-type latch.

The input thresholds are fixed at levels which comply with both 3.3V and 2.5V interfaces. The output driver can source 4mA and sink 8mA (3.3V output supply). The output drivers have a separate VCCIO power supply which is independent of the main VCC supply for the device. This feature allows the output drivers to run from either 3.3V or 2.5V while the device logic is always powered from 3.3V. The output drivers also provide individually programmable edge rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by another device.

The ispLSI 8000V Family features 3.3V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop

## ispLSI 8000V Family Description (Continued)

truly reconfigurable systems. Programming is achieved through the industry standard IEEE 1149.1-compliant Boundary Scan interface using the JTAG protocol. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

## ispLSI 8600V Description

The ispLSI 8600V device has five Big Fast Megablocks for a total of  $5 \times 120 = 600$  macrocells.

Each Big Fast Megablock has a total of 24 I/O cells and the Global Routing Plane has a total of 144 I/O cells. This gives  $(5 \times 24) + 144 = 264$  I/Os for the full I/O version, while the partial I/O version contains 72 BFM I/O + 120 Global I/O = 192 I/Os.

The total registers in the device is the sum of macrocells plus I/O cells,  $600 + 264 = 864$  registers.

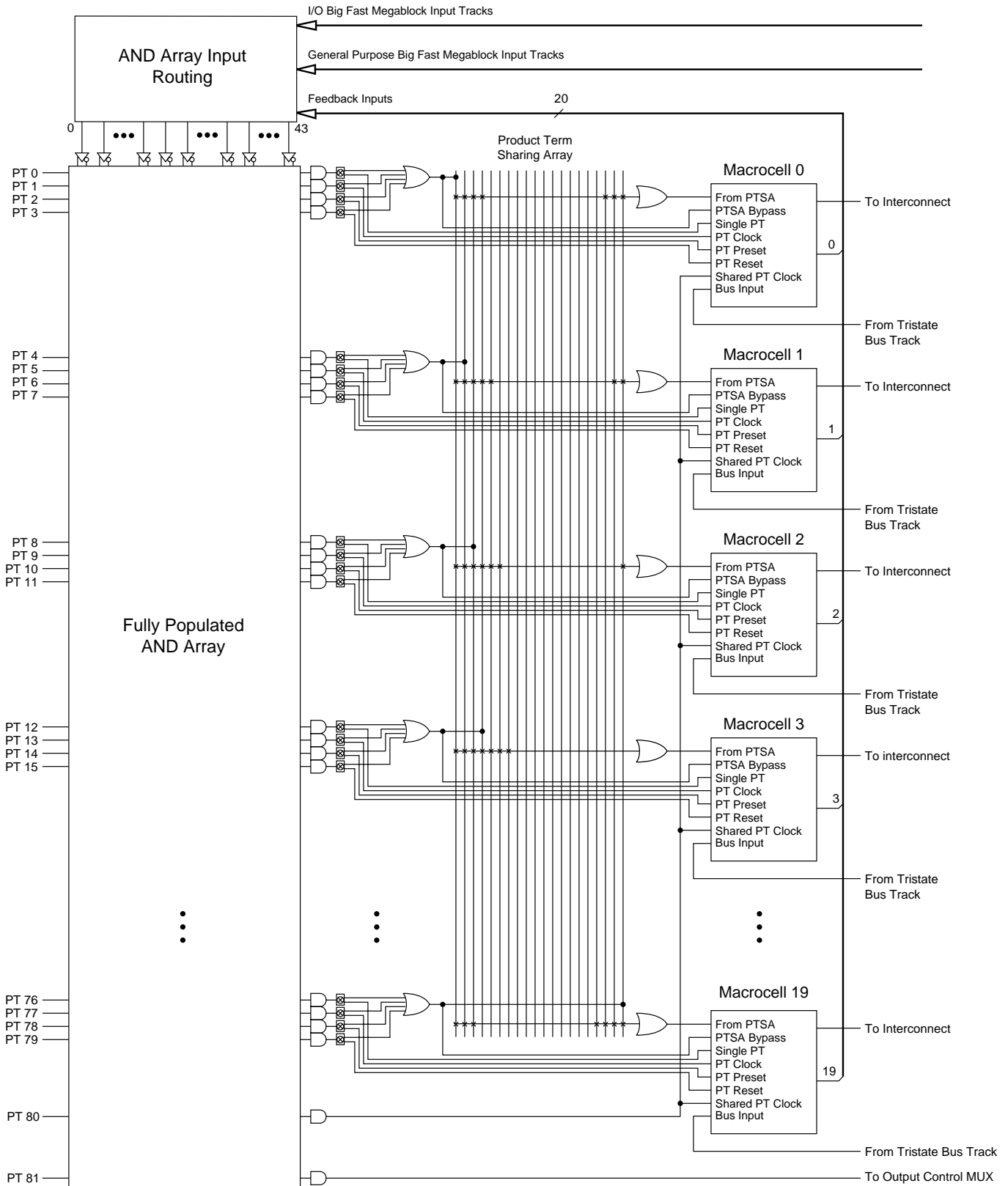
## Embedded Tristate Bus

There is a 108-line embedded internal tristate bus as part of the Global Routing Plane (GRP), enabling multiple GLBs to drive the same tracks. This bus can be partitioned into various bus widths such as twelve 9-line buses, six 18-line buses or three 36-line buses. The GLBs can dynamically share a subset of the Global Routing Plane tracks. This feature eliminates the need to convert tristate buses to wide multiplexers on the pro-

grammable device. Up to 18 macrocells per GLB can participate in driving the embedded tristate bus. The remaining two macrocells per GLB are used to generate the internal tristate driver control signals on each data byte (with parity). The embedded tristate bus can also be configured as an extension of an external tristate bus using the bidirectional capability of the I/O cells connected to the Global Routing Plane. The Global Routing Plane I/Os 0-8 and 15-23 from each group (I/OGx as defined in the I/O Pin Location Table) can connect to the internal tristate bus as well as the unidirectional/non-tristate global routing channels. I/Os 9-14 connect only to the global routing channel.

The embedded tristate bus has internal bus hold and arbitration features in order to make the function more "user friendly". The bus hold feature keeps the internal bus at the previously driven logic state when the bus is not driven to eliminate bus float. The bus arbitration is performed on a "first come, first served" priority. In other words, once a logic block drives the bus, other logic blocks cannot drive the bus until the first releases the bus. This arbitration feature prevents internal bus contention when there is an overlap between two bus enable signals. Typically, it takes about 3ns to resolve one bus signal coming off the bus to another bus signal driving the bus. The arbitration feature, combined with the predictability of the CPLD, makes the embedded tristate bus the most practical for real world bus implementation.

Figure 2. ispLSI 8000V GLB Overview

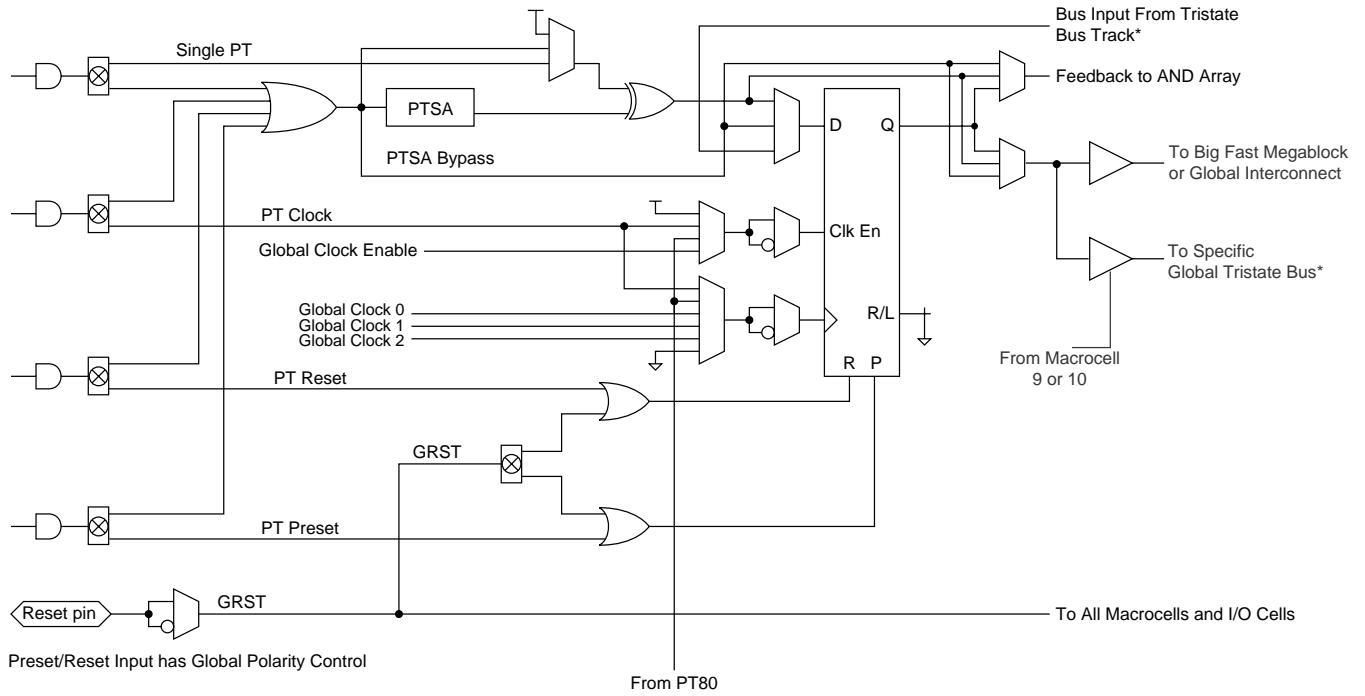


Note: Macrocells 9 and 10 do not support Tristate Bus Feedback.


☐ Function Selector (E<sup>2</sup> Cell Controlled)

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Figure 3. ispLSI 8000V Macrocell Overview

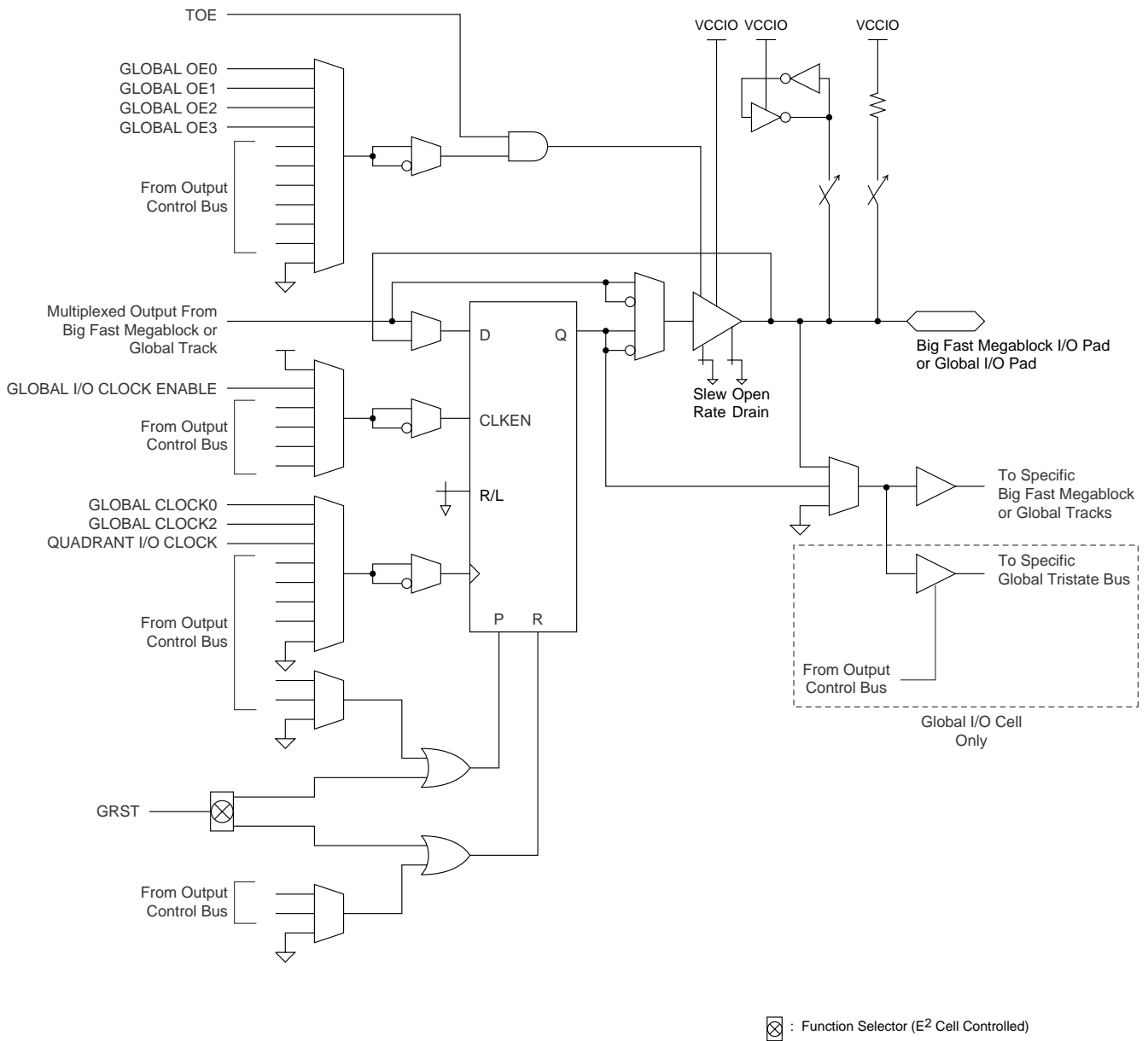


\*Not available for Macrocells 9 and 10.

 : Function Selector (E<sup>2</sup> Cell Controlled)

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Figure 4. ispLSI 8000V I/O Cell



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**Output Control Organization**

In addition to the data input and output to the I/O cells, each I/O cell can have up to six different I/O cell control signals. In addition to the internal OE control, the five control signals for each I/O cell consist of pin OE control, clock enable, clock input, asynchronous preset and asynchronous reset. All of the I/O control signals can be driven either from the dedicated external input pins or from the internal control bus.

The output enable of each I/O cell can be driven by 21 different sources – 16 from the output control bus, four from the Global OE pins and one from the Test OE pin.

The Global OE signals and Test OE signal are driven from the dedicated external control input pins.

The 16-bit wide output control buses are organized in four different quadrants as shown in Figure 5. Since each GLB is capable of generating the output control signals, each of the output control bus signals can be driven from a unique GLB. The 30 GLBs can generate a total of 30 unique I/O control signals. Referring to Figure 2, the GLB generates its output control signal from control product term (PT81).

Figure 5 also illustrates how the quadrant clocks are routed to the appropriate quadrant I/O cells.

**Figure 5. Output Control Bus and Quadrant Organization**



OE Bus/8600V.eps

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Figure 6. Boundary Scan Register Circuit for I/O Pins

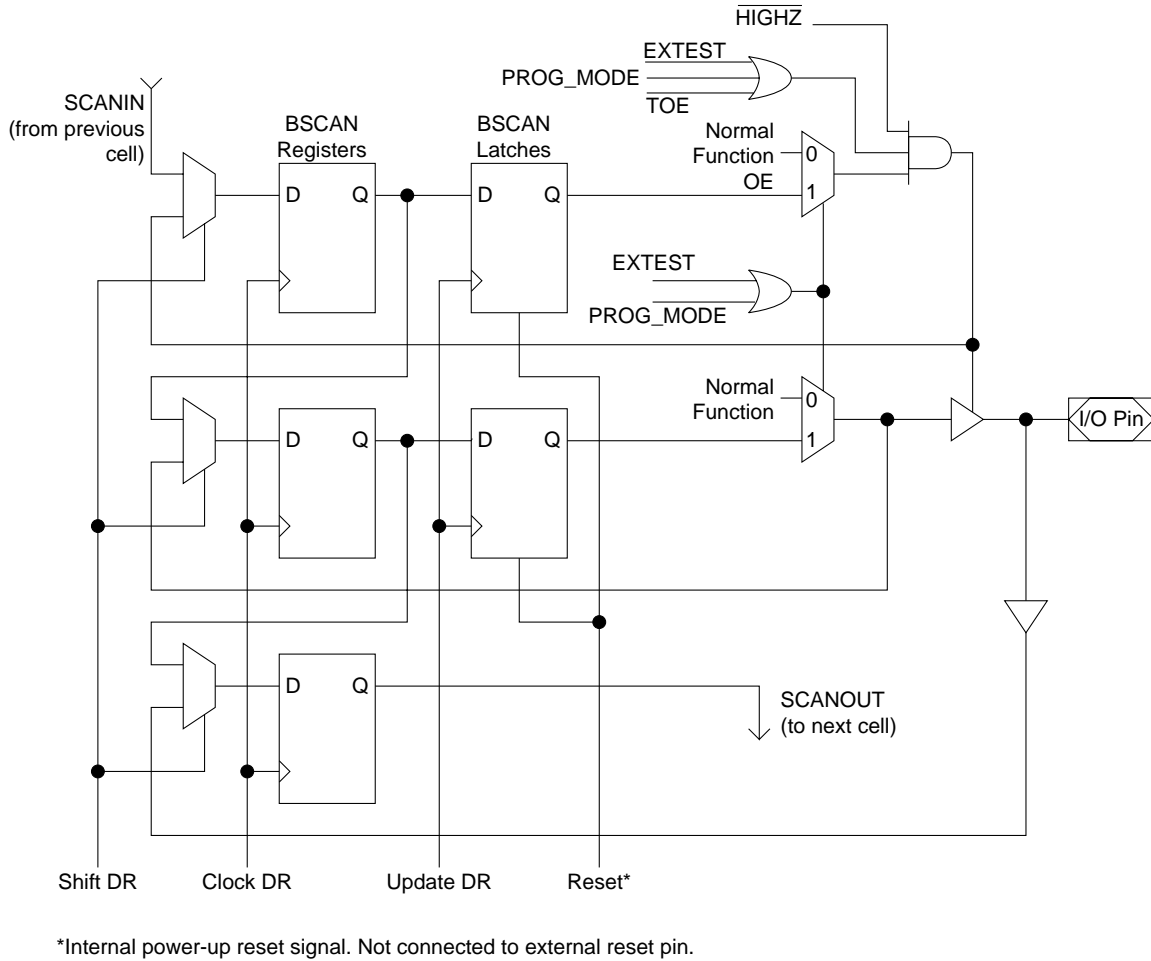
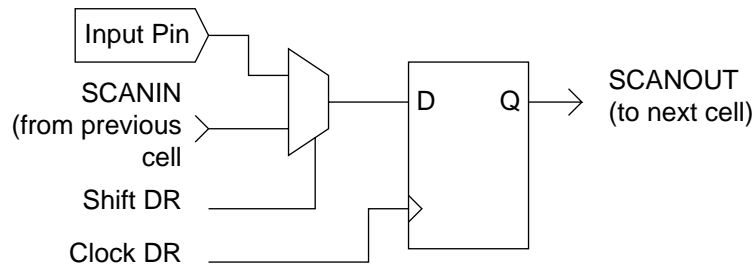
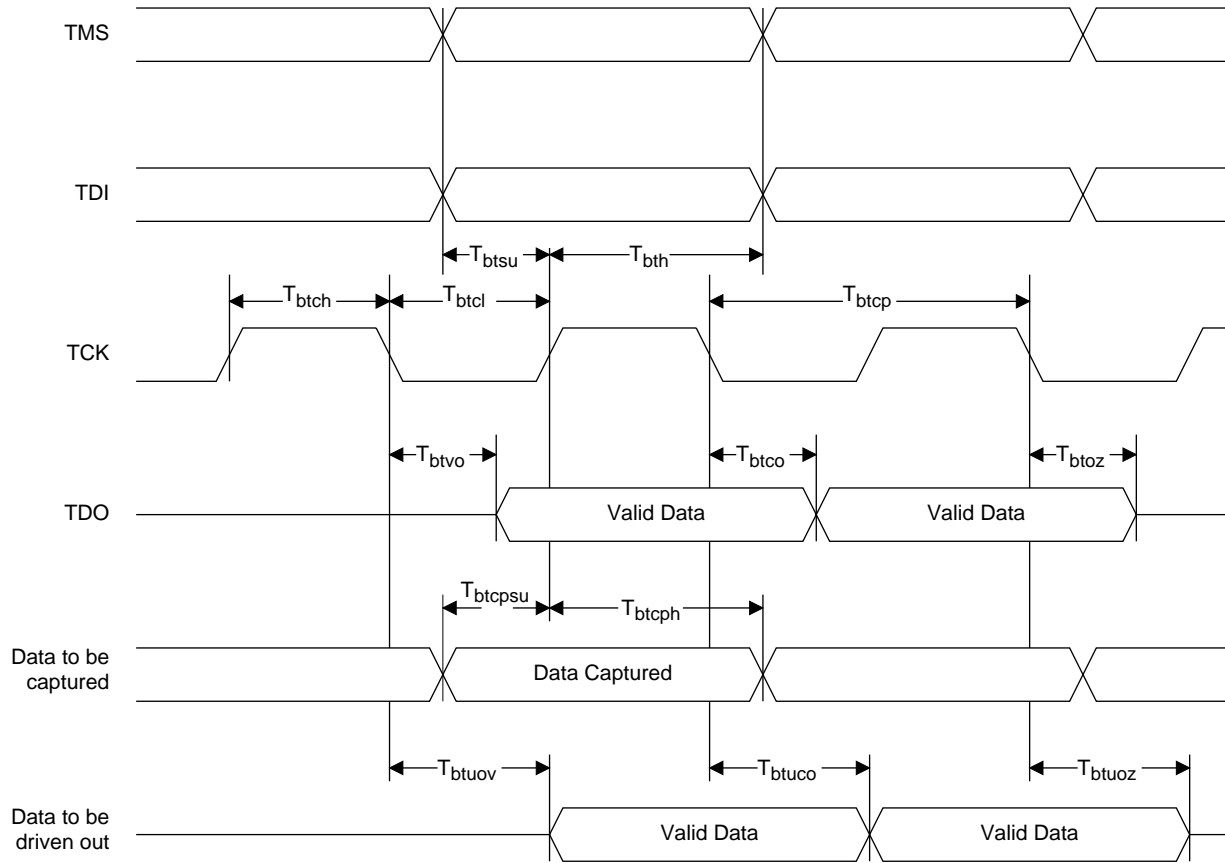


Figure 7. Boundary Scan Register Circuit for Input-Only Pins



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Figure 8. Boundary Scan Waveforms and Timing Specifications



SYMBOL	PARAMETER	MIN	MAX	UNITS
$t_{btcp}$	TCK Clock Pulse Width	100	—	ns
$t_{btch}$	TCK Pulse Width High	50	—	ns
$t_{btcl}$	TCK Pulse Width Low	50	—	ns
$t_{btso}$	TDI, TMS Setup Time to TCK	25	—	ns
$t_{btth}$	TDI, TMS Hold Time from TCK	25	—	ns
$t_{rf}$	TCK, TDI, TMS Rise and Fall Time	50	—	mV/ns
$t_{btco}$	TAP Controller, TCK to TDO Valid	—	25	ns
$t_{btsoz}$	TAP Controller, TCK to TDO High-Impedance	—	25	ns
$t_{btvo}$	TAP Controller, TCK to TDO High-Impedance to Valid Output	—	25	ns
$t_{btcpso}$	BSCAN Test Capture Register Setup Time	25	—	ns
$t_{btcp}$	BSCAN Test Capture Register Hold Time	25	—	ns
$t_{btuco}$	BSCAN Test Update Register Clock to Valid Output	—	65	ns
$t_{btuoiz}$	BSCAN Test Update Register Clock to High-Impedance	—	65	ns
$t_{btuoov}$	BSCAN Test Update Register High-Impedance to Valid Output	—	65	ns

Table 2-0010/8600V

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**Absolute Maximum Ratings 1,2**

- Supply Voltage  $V_{CC}$  ..... -0.5 to +5.4V
- Input Voltage Applied ..... -0.5 to +5.6V
- Tri-Stated Output Voltage Applied ..... -0.5 to +5.6V
- Storage Temperature ..... -65 to 150°C
- Case Temp. with Power Applied ..... -55 to 125°C
- Max. Junction Temp. ( $T_J$ ) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

**DC Recommended Operating Condition**

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
$V_{CC}$	Supply Voltage	Commercial $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$	3.0	3.6	V
$V_{CCIO}$	I/O Supply Voltage		2.3	3.6	V

Table 2-0005/8600V

**Capacitance ( $T_A=25^\circ\text{C}, f=1.0\text{ MHz}$ )**

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
$C_1$	I/O Capacitance	10	pf	$V_{CC} = 3.3\text{V}, V_{I/O} = 2.0\text{V}$
$C_2$	Clock Capacitance	10	pf	$V_{CC} = 3.3\text{V}, V_{CK} = 2.0\text{V}$
$C_3$	Global Input Capacitance	10	pf	$V_{CC} = 3.3\text{V}, V_G = 2.0\text{V}$

Table 2-0006/8600V

**Erase/Reprogram Specification**

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/8600V

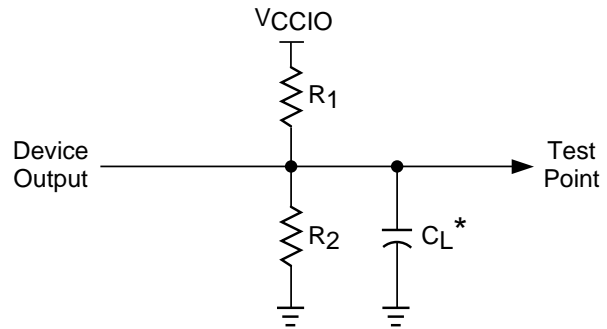
**Switching Test Conditions**

Input Pulse Levels	GND to VCCIO <sub>min</sub>
Input Rise and Fall Time	≤ 1.5 ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 9

3-state levels are measured 0.5V from steady-state active level.

Table 2-0003/8600V

**Figure 9. Test Load**



\*CL includes Test Fixture and Probe Capacitance.

0213A/8600V

**Output Load Conditions (See Figure 9)**

		3.3V		2.5V		
TEST CONDITION		R1	R2	R1	R2	CL
A		316Ω	348Ω	511Ω	475Ω	35pF
B	Active High	∞	348Ω	∞	475Ω	35pF
	Active Low	316Ω	∞	511Ω	∞	35pF
C	Active High to Z at V <sub>OH</sub> -0.5V	∞	348Ω	∞	475Ω	5pF
	Active Low to Z at V <sub>OL</sub> +0.5V	316Ω	∞	511Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2-0004A/8600V

**DC Electrical Characteristics for 3.3V Range**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNITS
VCCIO	I/O Supply Voltage	T <sub>A</sub> = 0°C to + 70°C	3.0	3.6	V
VIL	Input Low Voltage		-0.3	0.8	V
VIH	Input High Voltage		2.0	5.25	V
VOL	Output Low Voltage	I <sub>OL</sub> = 8 mA	-	0.4	V
VOH	Output High Voltage	I <sub>OH</sub> = -4 mA	2.4	-	V

Table 2-0007/8600V

**DC Electrical Characteristics for 2.5V Range**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNITS
VCCIO	I/O Supply Voltage	T <sub>A</sub> = 0°C to + 70°C	2.3	2.7	V
VIL	Input Low Voltage		-0.3	0.7	V
VIH	Input High Voltage		1.7	5.25	V
VOL	Output Low Voltage	VCCIO=min, VIN=VIH or VIL, IOL= 100μA	-	0.2	V
		VCCIO=min, VIN=VIH or VIL, IOL= 2mA	-	0.7	V
VOH	Output High Voltage	VCCIO=min, VIN=VIH or VIL, IOH= -100μA	2.1	-	V
		VCCIO=min, VIN=VIH or VIL, IOH= -2mA	1.7	-	V

Table 2-0007B/8600V

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**DC Electrical Characteristics**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>2</sup>	MAX.	UNITS	
I <sub>IL</sub>	Input or I/O Low Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>IL</sub> (Max.)	–	–	-10	μA	
I <sub>IH</sub>	Input or I/O High Leakage Current	(V <sub>CCIO</sub> -0.2)V ≤ V <sub>IN</sub> ≤ V <sub>CCIO</sub>	–	–	10	μA	
		V <sub>CCIO</sub> ≤ V <sub>IN</sub> ≤ 5.25V	–	–	50	μA	
I <sub>PU</sub> <sup>4</sup>	I/O Active Pullup Current	0V ≤ V <sub>IN</sub> ≤ V <sub>IL</sub>	–	–	-250	μA	
I <sub>BHL</sub>	Bus Hold Low Sustaining Current	V <sub>IN</sub> = V <sub>IL(max)</sub>	40	–	–	μA	
I <sub>BHH</sub>	Bus Hold High Sustaining Current	V <sub>IN</sub> = V <sub>IH(min)</sub>	-40	–	–	μA	
I <sub>BHLO</sub>	Bus Hold Low Overdrive Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CCIO</sub>	–	–	550	μA	
I <sub>BHLH</sub>	Bus Hold High Overdrive Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CCIO</sub>	–	–	-550	μA	
I <sub>BHT</sub>	Bus Hold Trip Points		V <sub>IL</sub>	–	V <sub>IH</sub>	V	
I <sub>CC</sub> <sup>1,3,5</sup>	Operating Power Supply Current	V <sub>IL</sub> = 0.5V, V <sub>IH</sub> = 3.0V f <sub>TOGGLE</sub> = 1 MHz	High Speed Mode	–	330	–	mA
			Low Power Mode	–	160	–	

Table 2-0007C/8600V

1. Measured at a frequency of 1MHz using 30 20-bit counters.
2. Typical values are at V<sub>CC</sub> = 3.3V and T<sub>A</sub> = 25°C.
3. Maximum I<sub>CC</sub> varies widely with specific device configuration and operating frequency.
4. Pullup is capable of pulling minimum voltage of V<sub>OH</sub> under no-load conditions.
5. Unused inputs held at GND.

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**External Switching Characteristics<sup>1</sup>**

**Over Recommended Operating Conditions**

PARAMETER	TEST COND. <sup>4</sup>	# <sup>2</sup>	DESCRIPTION	-125		-90		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>pd1</sub>	A	1	Prop Delay, BFM Input to Same BFM Output, 4 PT Bypass	—	8.5	—	10.0	—	15.0	ns
t <sub>pd2</sub>	A	2	Prop Delay, Global Input to Global Output	—	13.5	—	16.0	—	24.0	ns
f <sub>max</sub>	—	3	Clk Frequency, Local Feedback, Same GLB <sup>3</sup>	125.0	—	90.0	—	60.0	—	MHz
t <sub>suq</sub>	—	4	I/O Cell Reg, Data Setup Time, Quadrant I/O Clock	5.0	—	8.0	—	12.0	—	ns
t <sub>hq</sub>	—	5	I/O Cell Reg, Data Hold Time, Quadrant I/O Clock	0.0	—	0.0	—	0.0	—	ns
t <sub>coq</sub>	A	6	I/O Cell Reg, Quadrant Clock to Output Delay	—	4.0	—	6.0	—	9.0	ns
t <sub>sug</sub>	—	7	I/O Cell Reg, Data Setup Time, Global Clock	3.5	—	6.0	—	9.0	—	ns
t <sub>hg</sub>	—	8	I/O Cell Reg, Data Hold Time, Global Clock	0.0	—	0.0	—	0.0	—	ns
t <sub>cog</sub>	A	9	I/O Cell Reg, Global Clock to Output Delay	—	6.0	—	7.5	—	11.0	ns
t <sub>su1</sub>	—	10	GLB Reg Setup, BFM Input to Same BFM GLB, 4 PT Bypass	4.5	—	7.0	—	10.0	—	ns
t <sub>h1</sub>	—	11	GLB Reg Hold Time, BFM Input to Same BFM GLB	0.0	—	0.0	—	0.0	—	ns
t <sub>co1</sub>	A	12	GLB Reg, Global Clock to Same BFM Output Delay	—	8.0	—	10.0	—	15.0	ns
t <sub>suceq</sub>	—	13	I/O Cell Reg, CLKEN Setup Time, Quadrant I/O Clock	5.5	—	6.5	—	9.5	—	ns
t <sub>hceq</sub>	—	14	I/O Cell Reg, CLKEN Hold Time, Quadrant I/O Clock	0.0	—	0.0	—	0.0	—	ns
t <sub>suceg</sub>	—	15	GLB Reg, CLKEN Setup Time, Global Clock	3.5	—	4.5	—	6.5	—	ns
t <sub>hceg</sub>	—	16	GLB Reg, CLKEN Hold Time, Global Clock	0.0	—	0.0	—	0.0	—	ns
t <sub>goe</sub>	B/C	17	Global Output Enable/Disable Delay	—	7.0	—	10.0	—	15.0	ns
t <sub>rglb</sub>	—	18	Global Reset/Preset Time, GLB Reg	—	14.0	—	15.0	—	22.0	ns
t <sub>rio</sub>	—	19	Global Reset/Preset Time, I/O Cell Reg	—	8.5	—	10.0	—	15.0	ns
t <sub>rw</sub>	—	20	Global Reset/Preset Pulse Duration	5.0	—	6.5	—	9.5	—	ns
t <sub>wh</sub>	—	21	Global or Quadrant Clock Pulse, High Duration	4.0	—	6.0	—	9.0	—	ns
t <sub>wl</sub>	—	22	Global or Quadrant Clock Pulse, Low Duration	4.0	—	6.0	—	9.0	—	ns

Table 2-0030/8600V

1. Unless noted otherwise, all parameters use PTSA and CLK0.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 20-bit counter with local feedback.
4. Refer to Switching Test Conditions section.

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**Internal Timing Parameters**

**Over Recommended Operating Conditions**

PARAMETER	#2	DESCRIPTION	-125		-90		-60		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>I/O Cell Delay</b>									
t <sub>idcom</sub>	23	Input Pad and Input Buffer, Combinatorial Input	–	0.3	–	0.4	–	0.6	ns
t <sub>idreg</sub>	24	Input Pad and Input Buffer, Registered Input	–	6.4	–	7.6	–	11.2	ns
t <sub>obp</sub>	25	Output Register/Latch Bypass to Output Buffer	–	0.0	–	0.0	–	0.0	ns
t <sub>ibp</sub>	26	Input Register/Latch Bypass to BFM Routing or GRP	–	0.4	–	0.5	–	0.8	ns
t <sub>iolat</sub>	27	I/O Cell Latch, Transparent Mode	–	2.0	–	2.4	–	3.6	ns
t <sub>ioco</sub>	28	I/O Cell Register/Latch, Clk/Gate to Output	–	0.5	–	1.2	–	1.6	ns
t <sub>iosu</sub>	29	I/O Cell Register/Latch, Setup Time	0.5	–	2.4	–	3.9	–	ns
t <sub>ioh</sub>	30	I/O Cell Register/Latch, Hold Time	2.5	–	3.2	–	4.7	–	ns
t <sub>iorst</sub>	31	I/O Cell Register/Latch, Reset or Set Time	–	1.5	–	1.7	–	2.5	ns
t <sub>iosuce</sub>	32	I/O Cell Register/Latch, Setup Time for Clk Enable	0.9	–	1.0	–	1.2	–	ns
t <sub>iohce</sub>	33	I/O cell Register/Latch, Hold Time for Clk Enable	4.6	–	4.6	–	6.9	–	ns
t <sub>odreg</sub>	34	I/O Cell Output Buffer Delay, Registered Output	–	1.6	–	1.9	–	2.9	ns
t <sub>odcom</sub>	35	I/O Cell Output Buffer Delay, Combinatorial Output	–	1.6	–	1.9	–	2.9	ns
t <sub>odz</sub>	36	Output Driver Disable Time	–	1.4	–	1.7	–	2.6	ns
t <sub>slf</sub>	37	Slew Rate Adder, Fast Slew Rate	–	0.0	–	0.0	–	0.0	ns
t <sub>sls</sub>	38	Slew Rate Adder, Slow Slew Rate	–	6.2	–	7.3	–	10.9	ns
<b>GLB / Macrocell Delay</b>									
t <sub>andhs</sub>	39	AND Array, High Speed Mode	–	2.6	–	2.9	–	4.2	ns
t <sub>andlp</sub>	40	AND Array, Low Power Mode	–	6.5	–	7.7	–	11.5	ns
t <sub>1pt</sub>	41	Single Product Term Bypass	–	1.9	–	2.2	–	3.4	ns
t <sub>4ptcom</sub>	42	Four Product Term Bypass, Combinatorial Macrocell	–	0.5	–	0.6	–	0.9	ns
t <sub>4ptreg</sub>	43	Four Product Term Bypass, Registered Macrocell	–	1.4	–	1.7	–	2.2	ns
t <sub>ptsa</sub>	44	Product Term Sharing Array	–	2.4	–	2.7	–	4.1	ns
t <sub>mbp</sub>	45	Macrocell Register/Latch Bypass	–	0.0	–	0.0	–	0.0	ns
t <sub>mlat</sub>	46	Macrocell Latch, Transparent Mode	–	4.6	–	5.5	–	8.2	ns
t <sub>mco</sub>	47	Macrocell Register/Latch, Clk/Gate to Output	–	0.2	–	0.8	–	0.9	ns
t <sub>msu</sub>	48	Macrocell Register/Latch, Setup Time	2.7	–	4.5	–	6.9	–	ns
t <sub>mh</sub>	49	Macrocell Register/Latch, Hold Time	1.0	–	1.2	–	1.1	–	ns
t <sub>mrst</sub>	50	Macrocell Register/Latch, Reset or Set Time	–	2.0	–	1.5	–	1.6	ns
t <sub>msuce</sub>	51	Macrocell Register/Latch, Setup Time for Clk Enable	1.0	–	1.3	–	1.7	–	ns
t <sub>mhce</sub>	52	Macrocell Register/Latch, Hold Time for Clk Enable	2.3	–	2.6	–	3.9	–	ns
t <sub>floc</sub>	54	Local Feedback to AND Array	–	0.1	–	0.1	–	0.6	ns
t <sub>pk</sub>	55	Single Product Term, Clk	1.3	1.3	1.6	1.6	2.5	2.5	ns
t <sub>pkcn</sub>	56	Single Product Term, Clk Enable	–	1.7	–	2.0	–	3.1	ns
t <sub>sck</sub>	57	Shared Product Term, Clk	1.7	1.9	2.0	2.3	3.1	3.5	ns
t <sub>sckcn</sub>	58	Shared Product Term, Clk Enable	1.7	1.9	2.0	2.3	3.1	3.5	ns
t <sub>prst</sub>	59	Single Product Term, Reset or Set Delay	–	1.5	–	1.7	–	2.6	ns
t <sub>rdir</sub>	60	Macrocell Register, Direct Input from GRP	–	7.2	–	8.4	–	12.7	ns

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**Internal Timing Parameters**

**Over Recommended Operating Conditions**

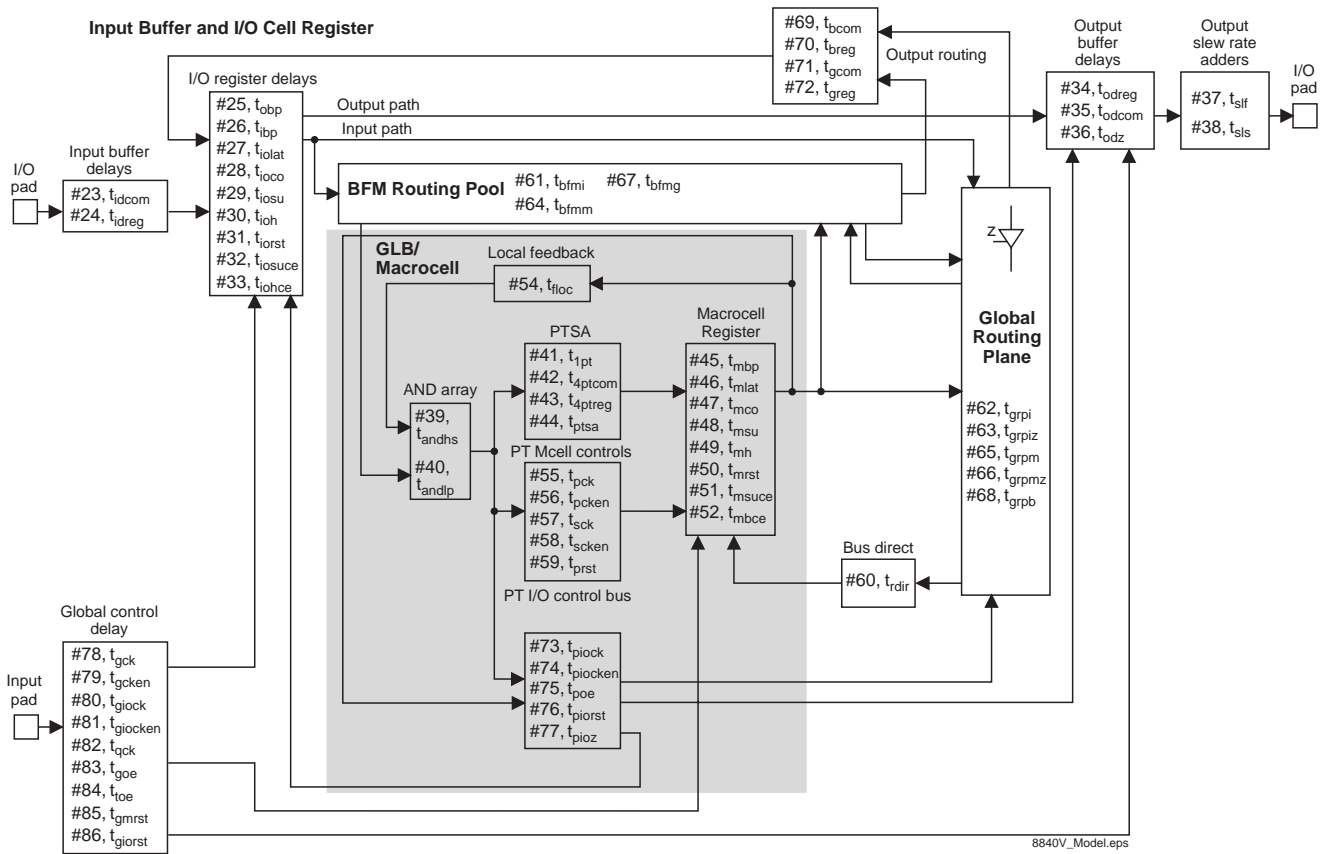
PARAMETER	#2	DESCRIPTION	-125		-90		-60		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>BFM / Global Routing Pool Delay</b>									
tbfmi	61	BFM Routing Delay, Signal from I/O Cell	0.4	1.0	0.6	1.3	0.8	1.9	ns
tgrpi	62	GRP Delay, Signal from I/O Cell	–	1.6	–	1.9	–	2.8	ns
tgrpiz	63	Internal Tristate Bus Enable/Disable, I/O Cell Buffer	–	4.1	–	4.9	–	7.3	ns
tbfmm	64	BFM Routing Delay, Signal from Macrocell	–	0.6	–	0.7	–	1.1	ns
tgrpm	65	GRP Delay, Signal from Macrocell	–	2.0	–	3.0	–	4.5	ns
tgrpmz	66	Internal Tristate Bus Enable/Disable, Macrocell Buffer	–	3.0	–	4.3	–	6.5	ns
tbfmg	67	BFM Routing Delay, Signal from GRP	–	2.5	–	3.3	–	4.9	ns
tgrpb	68	GRP Delay, Signal from BFM Routing	–	1.3	–	1.5	–	2.3	ns
tocom	69	BFM Routing to I/O Cell, Combinatorial Path	–	1.5	–	1.7	–	2.6	ns
treg	70	BFM Routing to I/O Cell, Registered Path	–	2.3	–	2.6	–	4.0	ns
tgcom	71	GRP to I/O Cell, Combinatorial Path	–	0.8	–	0.8	–	1.2	ns
tgreg	72	GRP to I/O Cell, Registered Path	–	1.6	–	1.7	–	2.6	ns
<b>I/O Control Bus Delay</b>									
tpiock	73	Product Term as I/O Cell Register Clock	–	4.1	–	4.7	–	7.2	ns
tpiocken	74	Product Term as I/O Cell Register Clock Enable	–	4.6	–	5.3	–	8.1	ns
tpoe	75	Product Term as Output Buffer Enable/Disable	–	5.6	–	6.5	–	9.9	ns
tpiorst	76	Product Term as I/O Cell Register Reset or Set Delay	–	4.3	–	5.0	–	7.6	ns
tpioz	77	Internal Tristate Bus Control Signal for I/O Cell Buffer	–	3.3	–	3.8	–	5.8	ns
<b>Global Control Delay</b>									
tgck	78	Global Macrocell Register Clk	3.9	4.1	4.3	4.9	6.6	7.5	ns
tgcken	79	Global Macrocell Register Clk Enable	6.4	6.4	7.5	7.5	11.4	11.4	ns
tgiock	80	Global I/O Register Clk	3.4	3.9	4.0	4.4	6.1	6.5	ns
tgiocken	81	Global I/O Register Clk Enable	6.5	6.5	7.5	7.5	11.4	11.4	ns
tqck	82	Quadrant I/O Register Clk	1.9	1.9	2.0	2.9	3.1	4.5	ns
tgoe	83	Global Output Enable	–	5.6	–	8.3	–	12.4	ns
ttoe	84	Test Output Enable	–	8.5	–	10.1	–	15.2	ns
tgmrst	85	Global GLB Register Reset	–	7.6	–	7.8	–	11.8	ns
tgorst	86	Global I/O Cell Register Reset	–	5.4	–	6.4	–	9.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

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**ispLSI 8600V Timing Model**



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## Example Timing Calculations

$$\begin{aligned}
 \text{tpd1} &= (\text{BFM Input Path Delay}) + (\text{GLB Delay}) + (\text{Output Path Delay}) \\
 &= (\text{t}_{\text{idcom}} + \text{t}_{\text{ibp}} + \text{t}_{\text{bfmi max}}) + (\text{t}_{\text{andhs}} + \text{t}_{\text{4ptcom}} + \text{t}_{\text{mbp}}) + (\text{t}_{\text{bfmm}} + \text{t}_{\text{bcom}} + \text{t}_{\text{obp}} + \text{t}_{\text{odcom}} + \text{t}_{\text{slf}}) \\
 &= (\#23 + \#26 + \#61) + (\#39 + \#42 + \#45) + (\#64 + \#69 + \#25 + \#35 + \#37) \\
 &= (0.3 + 0.4 + 1.0) + (2.6 + 0.5 + 0.0) + (0.6 + 1.5 + 0.0 + 1.6 + 0.0) \\
 &= 8.5 \text{ ns}
 \end{aligned}$$

$$\begin{aligned}
 \text{tpd (within BFM)} &= (\text{BFM Delay}) + (\text{GLB Delay}) \\
 &= (\text{t}_{\text{bfmm}}) + (\text{t}_{\text{andhs}} + \text{t}_{\text{4ptcom}} + \text{t}_{\text{mbp}}) \\
 &= (\#64) + (\#39 + \#42 + \#45) \\
 &= (0.6) + (2.6 + 0.5 + 0.0) \\
 &= 3.7 \text{ ns}
 \end{aligned}$$

$$\begin{aligned}
 \text{tpd (between BFMs)} &= (\text{GRP Delay}) + (\text{BFM Delay}) + (\text{GLB Delay}) \\
 &= (\text{t}_{\text{grpm}}) + (\text{t}_{\text{bfmg}}) + (\text{t}_{\text{andhs}} + \text{t}_{\text{4ptcom}} + \text{t}_{\text{mbp}}) \\
 &= (\#65) + (\#67) + (\#39 + \#42 + \#45) \\
 &= (2.0) + (2.5) + (2.6 + 0.5 + 0.0) \\
 &= 7.6 \text{ ns}
 \end{aligned}$$

$$\begin{aligned}
 \text{BFM I/O to internal tri-state Enable/Disable} &= (\text{BFM Input Path Delay}) + (\text{GLB Delay, 1PT}) + (\text{Tri-state Control Delay}) \\
 &= (\text{t}_{\text{idcom}} + \text{t}_{\text{ibp}} + \text{t}_{\text{bfmi max}}) + (\text{t}_{\text{andhs}} + \text{t}_{\text{1pt}} + \text{t}_{\text{mbp}}) + (\text{t}_{\text{grpmz}}) \\
 &= (\#23 + \#26 + \#61) + (\#39 + \#41 + \#45) + (\#66) \\
 &= (0.3 + 0.4 + 1.0) + (2.6 + 1.9 + 0.0) + (3.0) \\
 &= 9.2 \text{ ns}
 \end{aligned}$$

$$\begin{aligned}
 \text{tsu1} &= (\text{BFM Input Path Delay}) + (\text{GLB Setup Time}) - (\text{Min. Global Clock Delay}) \\
 &= (\text{t}_{\text{idcom}} + \text{t}_{\text{ibp}} + \text{t}_{\text{bfmi max}}) + (\text{t}_{\text{andhs}} + \text{t}_{\text{4ptreg}} + \text{t}_{\text{msu}}) - (\text{t}_{\text{gck min}}) \\
 &= (\#23 + \#26 + \#61) + (\#39 + \#43 + \#48) - (\#78) \\
 &= (0.3 + 0.4 + 1.0) + (2.6 + 1.4 + 2.7) - (3.9) \\
 &= 4.5 \text{ ns}
 \end{aligned}$$

$$\begin{aligned}
 1/\text{Fmax} &= (\text{Global Clk to MC Output}) + (\text{Local Feedback}) + (\text{GLB Setup Time}) \\
 &= (\text{t}_{\text{mco}}) + (\text{t}_{\text{floc}}) + (\text{t}_{\text{andhs}} + \text{t}_{\text{ptsa}} + \text{t}_{\text{msu}}) \\
 &= (\#47) + (\#54) + (\#39 + \#44 + \#48) \\
 &= (0.2) + (0.1) + (2.6 + 2.4 + 2.7) \\
 &= 8.0 \text{ ns}
 \end{aligned}$$

$$\text{Fmax} = 125 \text{ MHz}$$

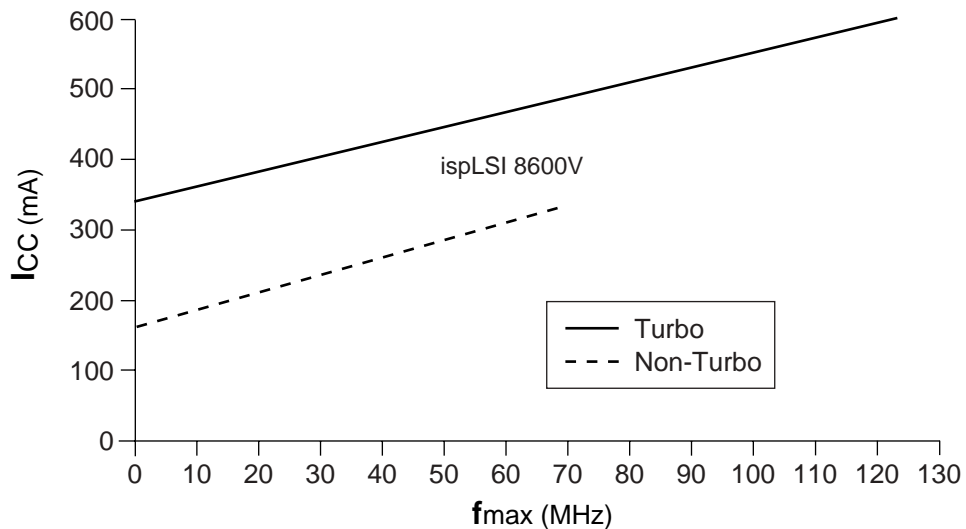
Note: Calculations are based upon timing specifications for the ispLSI 8600V-125L

**Power Consumption**

Power consumption in the ispLSI 8600V device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of four product terms has a single speed/power tradeoff control fuse that acts on the complete group of four. The fast “high-speed” setting

operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower “low-power” setting will significantly reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating speed.

**Figure 10. Typical Device Power Consumption vs fmax**



Notes: Configuration of 30 20-bit counters  
Typical current at 3.3V, 25°C

ICC can be estimated for the ispLSI 8600V using the following equation:

$$I_{CC} = 25.0 + (\# \text{ of Turbo PTs} * 0.25) + (\# \text{ of Non-Turbo PTs} * 0.11) + (\# \text{ of Macrocells Used} * f_{max} * AF * 0.04)$$

# of Turbo PTs = Number of Turbo Product Terms Used in Design  
 # of Non-Turbo PTs = Number of Non-Turbo Product Terms Used in Design  
 fmax = Maximum Operating Frequency

$$AF \text{ (Activity Factor)} = \frac{\text{Average Macrocell Toggle Frequency}}{F_{max}}$$

Note: An Activity Factor of 1.0 means all macrocell registers toggle at fmax. An Activity Factor of 0.5 means the average macrocell register toggles at half of fmax.

The ICC estimate is based on typical conditions (VCC = 3.3V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

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**Signal Descriptions**

Signal Name	Description
CLK0, CLK1, CLK2	Dedicated clock input for the GLB registers only. These clock inputs are connected to one of the clock inputs of all GLB registers in the device.
CLKEN	Dedicated clock enable input for the GLB registers only. This input is available as a clock enable for each GLB register in the device. Use of the clock enable input eliminates the need for the user to gate the clock to the register.
GND	Ground (GND)
GOE0, GOE1, GOE2, GOE3	Global Output Enable inputs.
SET/RESET	Dedicated, reset/preset pin connected to ALL registers in the device, GLB registers and I/O registers. Each register can independently choose to be reset or preset when this signal goes active. The active polarity is user selectable.
IOCLKEN	Dedicated clock enable input for the I/O registers only. This input is available as a clock enable input for all I/O registers in the device. Use of the clock enable input eliminates the need for the user to tie the clock to the I/O register.
I/O	Input/Output – These are the general purpose I/O used by the logic array.
EPEN	Embedded Port Enable Pin – When this pin is high, the port is enabled. When this pin is low, the state machine is held at reset asynchronously and TCK, TMS and TDI are ignored.
TMS	Input – This signal is the Test Mode Select input signal.
QIOCLK0, QIOCLK1, QIOCLK2, QIOCLK3	Dedicated clock inputs for the I/O registers only. These clock inputs are connected to the I/O registers on the same side of the device only, they are not connected to all of the I/O registers. Use of these quadrant I/O clocks gives the fastest tco from the device.
TCK	Input – This signal is the Test Clock input signal.
TDI	Input – This signal is the Test Data input signal.
TDO	Output – This signal is the Test Data Out Output Signal.
TOE	Test Output Enable. Tristates all I/O pins when a logic low is driven.
VCC	Vcc
VCCIO	Power supply for the output drivers. The internal logic of the device is connected to VCC which is always 3.3V. The output drivers are connected to VCCIO which can be equal to VCC or 2.5V. This allows the output drivers to be powered from 2.5V, for example, to interface directly with another 2.5V device.
NC <sup>1</sup>	No connect.

1. NC pins are not to be connected to any active signals, VCC or GND.

## Signal Locations

Signal Name	272-Ball BGA	492-Ball BGA
QIOCLK0, QIOCKL1, QIOCLK2, QIOCLK3	Y8, M20, C8, N2	AE14, P22, A15, N3
CLK0, CLK1, CLK2	Y9, P18, D8	AC15, R24, B15
CLKEN	V9	AB17
IOCLKEN	B9	E16
EPEN	C17	B26
TCK	A4	A2
TDI	U5	AF1
TDO	C4	B3
TMS	W4	AC4
GOE0, GOE1, GOE2, GOE3	Y10, M19, C9, N1	AF15, P23, D16, N5
TOE	L3	L5
SET/RESET	P3	P2
VCC	D9, D10, D11, D12, J4, J17, K4, K17, L4, L17, M4, M17, U9, U10, U11, U12	E9, E12, E15, E18, F5, F10, F17, F22, G5, G22, K5, K22, L22, M5, N22, P5, R22, T5, U5, U22, Y5, Y22, AA5, AA10, AA17, AA22, AB9, AB12, AB15, AB18
VCCIO	A7, A8, A20, B16, C5, C12, E4, G20, H4, M1, N17, U2, U20, V2, V6, W7, W8, W16, W19, Y13	E8, E13, E19, F7, F20, J6, J21, K3, L24, N1, P24, T3, U25, V6, Y23, AA7, AA20, AB8, AB14, AB19
GND	D4, D16, D17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, U4, U17	E5, E11, E14, E22, F6, F21, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, AA6, AA21, AB5, AB13, AB16, AB22
NC <sup>1</sup>	A9, V17, W9	A1, A6, A7, A8, A16, A20, A21, A22, , B1, B2, B7, B8, B9, B20, B21, C1, C2, C3, C7, C8, C9, C19, C20, C21, C24, C25, C26, D1, D2, D3, D4, D7, D8, D9, D19, D20, D21, D24, D25, D26, E6, E17, E20, E21, E23, E24, E25, E26, F8, F9, F18, F19, G6, G21, Y6, Y21, AA8, AA9, AA18, AA19, AB1, AB2, AB3, AB4, AB6, AB10, AB20, AB21, AB23, AC1, AC2, AC3, AC6, AC7, AC8, AC18, AC19, AC20, AC23, AC24, AC25, AC26, AD1, AD2, AD3, AD6, AD7, AD8, AD15, AD19, AD20, AD25, AD26, AE1, AE6, AE7, AE8, AE19, AE20, AE21, AE25, AE26, AF6, AF7, AF8, AF19, AF20, AF21, AF25, AF26

1. NC pins are not to be connected to any active signals, VCC or GND.

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**I/O Pin Locations (272-Ball BGA Package)**

Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA
I/O G0 <0>	V4	I/O G2 <15>	P19	I/O G4 <6>	F1	I/O G5 <21>	E17	I/O B3 <12>	B14
I/O G0 <1>	Y3	I/O G2 <16>	P17	I/O G4 <7>	F2	I/O G5 <22>	B18	I/O B3 <13>	D13
I/O G0 <2>	Y2	I/O G2 <17>	P20	I/O G4 <8>	F4	I/O G5 <23>	A18	I/O B3 <14>	B13
I/O G0 <3>	W3	I/O G2 <18>	R20	I/O G4 <9>	E1	I/O B0 <0>	Y4	I/O B3 <15>	A13
I/O G0 <4>	Y1	I/O G2 <19>	R19	I/O G4 <10>	E2	I/O B0 <1>	V5	I/O B3 <16>	A12
I/O G0 <5>	W2	I/O G2 <20>	R18	I/O G4 <11>	E3	I/O B0 <2>	W5	I/O B3 <17>	B12
I/O G0 <6>	W1	I/O G2 <21>	T20	I/O G4 <12>	D20	I/O B0 <3>	Y5	I/O B3 <18>	B11
I/O G0 <7>	V3	I/O G2 <22>	T19	I/O G4 <13>	F17	I/O B0 <4>	U6	I/O B3 <19>	A11
I/O G0 <8>	V1	I/O G2 <23>	T18	I/O G4 <14>	E19	I/O B0 <5>	U7	I/O B3 <20>	C11
I/O G0 <9>	U3	I/O G3 <0>	H2	I/O G4 <15>	G17	I/O B0 <6>	W6	I/O B3 <21>	B10
I/O G0 <10>	R4	I/O G3 <1>	H1	I/O G4 <16>	G18	I/O B0 <7>	V7	I/O B3 <22>	A10
I/O G0 <11>	T4	I/O G3 <2>	J3	I/O G4 <17>	F18	I/O B0 <8>	Y6	I/O B3 <23>	C10
I/O G0 <12>	U19	I/O G3 <3>	J2	I/O G4 <18>	E20	I/O B0 <9>	Y7	I/O B4 <0>	W14
I/O G0 <13>	R17	I/O G3 <4>	J1	I/O G4 <19>	F19	I/O B0 <10>	U8	I/O B4 <1>	V14
I/O G0 <14>	V20	I/O G3 <5>	K3	I/O G4 <20>	H17	I/O B0 <11>	V8	I/O B4 <2>	U14
I/O G0 <15>	V19	I/O G3 <6>	K2	I/O G4 <21>	F20	I/O B0 <12>	B8	I/O B4 <3>	Y15
I/O G0 <16>	U18	I/O G3 <7>	K1	I/O G4 <22>	H18	I/O B0 <13>	C7	I/O B4 <4>	W15
I/O G0 <17>	V18	I/O G3 <8>	L2	I/O G4 <23>	G19	I/O B0 <14>	D7	I/O B4 <5>	V15
I/O G0 <18>	T17	I/O G3 <9>	L1	I/O G5 <0>	A3	I/O B0 <15>	B7	I/O B4 <6>	U15
I/O G0 <19>	W20	I/O G3 <10>	M2	I/O G5 <1>	B2	I/O B0 <16>	B6	I/O B4 <7>	Y16
I/O G0 <20>	Y20	I/O G3 <11>	M3	I/O G5 <2>	B3	I/O B0 <17>	C6	I/O B4 <8>	V16
I/O G0 <21>	Y19	I/O G3 <12>	M18	I/O G5 <3>	A2	I/O B0 <18>	A6	I/O B4 <9>	U16
I/O G0 <22>	W18	I/O G3 <13>	L20	I/O G5 <4>	A1	I/O B0 <19>	D6	I/O B4 <10>	W17
I/O G0 <23>	Y18	I/O G3 <14>	L19	I/O G5 <5>	B1	I/O B0 <20>	B5	I/O B4 <11>	Y17
I/O G2 <0>	U1	I/O G3 <15>	L18	I/O G5 <6>	D3	I/O B0 <21>	A5	I/O B4 <12>	B17
I/O G2 <1>	T3	I/O G3 <16>	K20	I/O G5 <7>	D2	I/O B0 <22>	D5	I/O B4 <13>	A17
I/O G2 <2>	T2	I/O G3 <17>	K19	I/O G5 <8>	C3	I/O B0 <23>	B4	I/O B4 <14>	C16
I/O G2 <3>	T1	I/O G3 <18>	K18	I/O G5 <9>	C2	I/O B3 <0>	V10	I/O B4 <15>	D15
I/O G2 <4>	R3	I/O G3 <19>	J20	I/O G5 <10>	D1	I/O B3 <1>	W10	I/O B4 <16>	C15
I/O G2 <5>	R2	I/O G3 <20>	H20	I/O G5 <11>	C1	I/O B3 <2>	Y11	I/O B4 <17>	A16
I/O G2 <6>	R1	I/O G3 <21>	J19	I/O G5 <12>	D19	I/O B3 <3>	W11	I/O B4 <18>	B15
I/O G2 <7>	P4	I/O G3 <22>	H19	I/O G5 <13>	E18	I/O B3 <4>	V11	I/O B4 <19>	D14
I/O G2 <8>	P2	I/O G3 <23>	J18	I/O G5 <14>	C20	I/O B3 <5>	Y12	I/O B4 <20>	C14
I/O G2 <9>	N4	I/O G4 <0>	G2	I/O G5 <15>	B20	I/O B3 <6>	W12	I/O B4 <21>	A15
I/O G2 <10>	N3	I/O G4 <1>	G1	I/O G5 <16>	A19	I/O B3 <7>	V12	I/O B4 <22>	A14
I/O G2 <11>	P1	I/O G4 <2>	H3	I/O G5 <17>	C19	I/O B3 <8>	W13	I/O B4 <23>	C13
I/O G2 <12>	N18	I/O G4 <3>	G3	I/O G5 <18>	D18	I/O B3 <9>	U13		
I/O G2 <13>	N19	I/O G4 <4>	G4	I/O G5 <19>	B19	I/O B3 <10>	V13		
I/O G2 <14>	N20	I/O G4 <5>	F3	I/O G5 <20>	C18	I/O B3 <11>	Y14		

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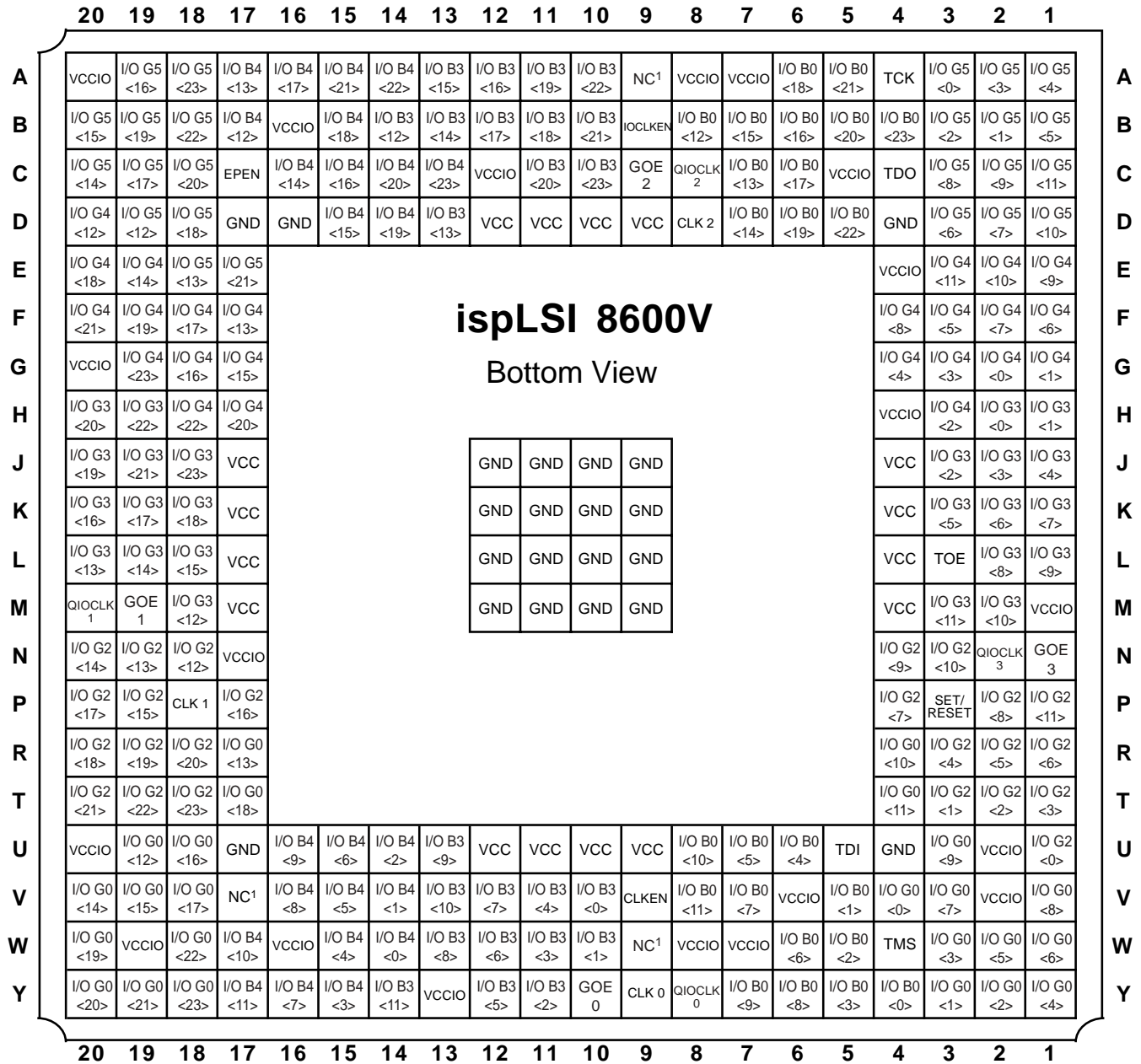
## I/O Pin Locations (492-Ball BGA Package)

Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA
I/O G0 <0>	AA4	I/O G2 <5>	R3	I/O G4 <10>	H4	I/O B0 <15>	D6	I/O B2 <20>	A13
I/O G0 <1>	AA3	I/O G2 <6>	R4	I/O G4 <11>	K6	I/O B0 <16>	A5	I/O B2 <21>	B13
I/O G0 <2>	AA2	I/O G2 <7>	R5	I/O G4 <12>	H26	I/O B0 <17>	B5	I/O B2 <22>	D12
I/O G0 <3>	AA1	I/O G2 <8>	P1	I/O G4 <13>	J23	I/O B0 <18>	C5	I/O B2 <23>	C12
I/O G0 <4>	Y4	I/O G2 <9>	P3	I/O G4 <14>	J24	I/O B0 <19>	D5	I/O B3 <0>	AE15
I/O G0 <5>	Y3	I/O G2 <10>	P4	I/O G4 <15>	J25	I/O B0 <20>	A4	I/O B3 <1>	AF16
I/O G0 <6>	Y2	I/O G2 <11>	N4	I/O G4 <16>	J22	I/O B0 <21>	B4	I/O B3 <2>	AC16
I/O G0 <7>	Y1	I/O G2 <12>	P26	I/O G4 <17>	J26	I/O B0 <22>	C4	I/O B3 <3>	AD16
I/O G0 <8>	W4	I/O G2 <13>	P25	I/O G4 <18>	K23	I/O B0 <23>	A3	I/O B3 <4>	AE16
I/O G0 <9>	W3	I/O G2 <14>	R23	I/O G4 <19>	K24	I/O B1 <0>	AC9	I/O B3 <5>	AF17
I/O G0 <10>	W2	I/O G2 <15>	T22	I/O G4 <20>	K25	I/O B1 <1>	AD9	I/O B3 <6>	AE17
I/O G0 <11>	U6	I/O G2 <16>	R26	I/O G4 <21>	H22	I/O B1 <2>	AE9	I/O B3 <7>	AD17
I/O G0 <12>	U21	I/O G2 <17>	R25	I/O G4 <22>	K26	I/O B1 <3>	AF9	I/O B3 <8>	AC17
I/O G0 <13>	Y26	I/O G2 <18>	T26	I/O G4 <23>	L25	I/O B1 <4>	AC10	I/O B3 <9>	AF18
I/O G0 <14>	Y25	I/O G2 <19>	T23	I/O G5 <0>	E4	I/O B1 <5>	AD10	I/O B3 <10>	AE18
I/O G0 <15>	Y24	I/O G2 <20>	W21	I/O G5 <1>	E3	I/O B1 <6>	AE10	I/O B3 <11>	AD18
I/O G0 <16>	V21	I/O G2 <21>	T24	I/O G5 <2>	E2	I/O B1 <7>	AF10	I/O B3 <12>	B19
I/O G0 <17>	AA26	I/O G2 <22>	T25	I/O G5 <3>	E1	I/O B1 <8>	AE11	I/O B3 <13>	A19
I/O G0 <18>	AA25	I/O G2 <23>	U26	I/O G5 <4>	F4	I/O B1 <9>	AD11	I/O B3 <14>	D18
I/O G0 <19>	AA24	I/O G3 <0>	K2	I/O G5 <5>	F3	I/O B1 <10>	AB11	I/O B3 <15>	C18
I/O G0 <20>	AA23	I/O G3 <1>	K1	I/O G5 <6>	F2	I/O B1 <11>	AC11	I/O B3 <16>	B18
I/O G0 <21>	AB26	I/O G3 <2>	L2	I/O G5 <7>	F1	I/O B1 <12>	A12	I/O B3 <17>	A18
I/O G0 <22>	AB25	I/O G3 <3>	H6	I/O G5 <8>	G4	I/O B1 <13>	E10	I/O B3 <18>	D17
I/O G0 <23>	AB24	I/O G3 <4>	L3	I/O G5 <9>	G3	I/O B1 <14>	B12	I/O B3 <19>	C17
I/O G1 <0>	T2	I/O G3 <5>	L4	I/O G5 <10>	G2	I/O B1 <15>	A11	I/O B3 <20>	B17
I/O G1 <1>	W5	I/O G3 <6>	L1	I/O G5 <11>	G1	I/O B1 <16>	D11	I/O B3 <21>	A17
I/O G1 <2>	U1	I/O G3 <7>	M2	I/O G5 <12>	K21	I/O B1 <17>	C11	I/O B3 <22>	B16
I/O G1 <3>	U2	I/O G3 <8>	M1	I/O G5 <13>	H25	I/O B1 <18>	B11	I/O B3 <23>	C16
I/O G1 <4>	U3	I/O G3 <9>	M3	I/O G5 <14>	H24	I/O B1 <19>	A10	I/O B4 <0>	AD21
I/O G1 <5>	U4	I/O G3 <10>	M4	I/O G5 <15>	H23	I/O B1 <20>	B10	I/O B4 <1>	AC21
I/O G1 <6>	V1	I/O G3 <11>	N2	I/O G5 <16>	G26	I/O B1 <21>	C10	I/O B4 <2>	AF22
I/O G1 <7>	V5	I/O G3 <12>	N23	I/O G5 <17>	G25	I/O B1 <22>	D10	I/O B4 <3>	AE22
I/O G1 <8>	V2	I/O G3 <13>	N24	I/O G5 <18>	G24	I/O B1 <23>	A9	I/O B4 <4>	AD22
I/O G1 <9>	V3	I/O G3 <14>	N26	I/O G5 <19>	G23	I/O B2 <0>	AF11	I/O B4 <5>	AC22
I/O G1 <10>	V4	I/O G3 <15>	N25	I/O G5 <20>	F26	I/O B2 <1>	AE12	I/O B4 <6>	AF23
I/O G1 <11>	W1	I/O G3 <16>	M22	I/O G5 <21>	F25	I/O B2 <2>	AF12	I/O B4 <7>	AE23
I/O G1 <12>	W23	I/O G3 <17>	M23	I/O G5 <22>	F24	I/O B2 <3>	AD12	I/O B4 <8>	AD23
I/O G1 <13>	W24	I/O G3 <18>	M24	I/O G5 <23>	F23	I/O B2 <4>	AC12	I/O B4 <9>	AF24
I/O G1 <14>	W25	I/O G3 <19>	M26	I/O B0 <0>	AE2	I/O B2 <5>	AE13	I/O B4 <10>	AE24
I/O G1 <15>	W26	I/O G3 <20>	H21	I/O B0 <1>	AF2	I/O B2 <6>	AF13	I/O B4 <11>	AD24
I/O G1 <16>	V22	I/O G3 <21>	M25	I/O B0 <2>	AE3	I/O B2 <7>	AD13	I/O B4 <12>	A26
I/O G1 <17>	V23	I/O G3 <22>	L26	I/O B0 <3>	AF3	I/O B2 <8>	AC13	I/O B4 <13>	D23
I/O G1 <18>	V24	I/O G3 <23>	L23	I/O B0 <4>	AD4	I/O B2 <9>	AC14	I/O B4 <14>	B25
I/O G1 <19>	V25	I/O G4 <0>	K4	I/O B0 <5>	AE4	I/O B2 <10>	AD14	I/O B4 <15>	A25
I/O G1 <20>	V26	I/O G4 <1>	H5	I/O B0 <6>	AF4	I/O B2 <11>	AF14	I/O B4 <16>	B24
I/O G1 <21>	W22	I/O G4 <2>	J1	I/O B0 <7>	AC5	I/O B2 <12>	C15	I/O B4 <17>	A24
I/O G1 <22>	U23	I/O G4 <3>	J2	I/O B0 <8>	AD5	I/O B2 <13>	D15	I/O B4 <18>	C23
I/O G1 <23>	U24	I/O G4 <4>	J3	I/O B0 <9>	AE5	I/O B2 <14>	B14	I/O B4 <19>	B23
I/O G2 <0>	T4	I/O G4 <5>	J4	I/O B0 <10>	AB7	I/O B2 <15>	A14	I/O B4 <20>	A23
I/O G2 <1>	T1	I/O G4 <6>	H1	I/O B0 <11>	AF5	I/O B2 <16>	C14	I/O B4 <21>	D22
I/O G2 <2>	W6	I/O G4 <7>	J5	I/O B0 <12>	B6	I/O B2 <17>	D14	I/O B4 <22>	C22
I/O G2 <3>	R2	I/O G4 <8>	H2	I/O B0 <13>	E7	I/O B2 <18>	D13	I/O B4 <23>	B22
I/O G2 <4>	R1	I/O G4 <9>	H3	I/O B0 <14>	C6	I/O B2 <19>	C13		

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**Signal Configuration**

ispLSI 8600V 272-Ball BGA Signal Diagram



1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

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**Signal Configuration**

**ispLSI 8600V 492-Ball BGA Signal Diagram**

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
<b>A</b>	I/O B4 <12>	I/O B4 <15>	I/O B4 <17>	I/O B4 <20>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B3 <13>	I/O B3 <17>	I/O B3 <21>	NC <sup>1</sup>	QIOCLK <sub>2</sub>	I/O B2 <15>	I/O B2 <20>	I/O B1 <12>	I/O B1 <15>	I/O B1 <19>	I/O B1 <23>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B0 <16>	I/O B0 <20>	I/O B0 <23>	TCK	NC <sup>1</sup>	<b>A</b>		
<b>B</b>	EPEN	I/O B4 <14>	I/O B4 <16>	I/O B4 <19>	I/O B4 <23>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B3 <12>	I/O B3 <16>	I/O B3 <20>	I/O B3 <22>	CLK <sub>2</sub>	I/O B2 <14>	I/O B2 <21>	I/O B1 <14>	I/O B1 <18>	I/O B1 <22>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B0 <12>	I/O B0 <17>	I/O B0 <21>	TDO	NC <sup>1</sup>	NC <sup>1</sup>	<b>B</b>		
<b>C</b>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B4 <18>	I/O B4 <22>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B3 <15>	I/O B3 <19>	I/O B3 <23>	I/O B2 <12>	I/O B2 <16>	I/O B2 <19>	I/O B2 <23>	I/O B1 <17>	I/O B1 <21>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B0 <14>	I/O B0 <18>	I/O B0 <22>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	<b>C</b>		
<b>D</b>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B4 <13>	I/O B4 <21>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B3 <14>	I/O B3 <18>	GOE <sub>2</sub>	I/O B2 <13>	I/O B2 <17>	I/O B2 <18>	I/O B2 <22>	I/O B1 <16>	I/O B1 <22>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B0 <15>	I/O B0 <19>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	<b>D</b>		
<b>E</b>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	GND	NC <sup>1</sup>	NC <sup>1</sup>	VCCIO	VCC	NC <sup>1</sup>	IOCKEN	VCC	GND	VCCIO	VCC	GND	I/O B1 <13>	VCC	VCCIO	I/O B0 <13>	NC <sup>1</sup>	GND	I/O G5 <0>	I/O G5 <1>	I/O G5 <2>	I/O G5 <3>	<b>E</b>		
<b>F</b>	I/O G5 <20>	I/O G5 <21>	I/O G5 <22>	I/O G5 <23>	VCC	GND	VCCIO	NC <sup>1</sup>	NC <sup>1</sup>	VCC							VCC	NC <sup>1</sup>	NC <sup>1</sup>	VCCIO	GND	VCC	I/O G5 <4>	I/O G5 <5>	I/O G5 <6>	I/O G5 <7>	<b>F</b>		
<b>G</b>	I/O G5 <16>	I/O G5 <17>	I/O G5 <18>	I/O G5 <19>	VCC	NC <sup>1</sup>															NC <sup>1</sup>	VCC	I/O G5 <8>	I/O G5 <9>	I/O G5 <10>	I/O G5 <11>	<b>G</b>		
<b>H</b>	I/O G4 <12>	I/O G5 <13>	I/O G5 <14>	I/O G5 <15>	I/O G4 <21>	I/O G3 <20>																I/O G3 <3>	I/O G4 <1>	I/O G4 <10>	I/O G4 <9>	I/O G4 <8>	I/O G4 <6>	<b>H</b>	
<b>J</b>	I/O G4 <17>	I/O G4 <15>	I/O G4 <14>	I/O G4 <13>	I/O G4 <16>	VCCIO																VCCIO	I/O G4 <7>	I/O G4 <5>	I/O G4 <4>	I/O G4 <3>	I/O G4 <2>	<b>J</b>	
<b>K</b>	I/O G4 <22>	I/O G4 <20>	I/O G4 <19>	I/O G4 <18>	VCC	I/O G5 <12>																I/O G4 <11>	VCC	I/O G4 <0>	VCCIO	I/O G3 <0>	I/O G3 <1>	<b>K</b>	
<b>L</b>	I/O G3 <23>	I/O G4 <23>	VCCIO	I/O G3 <23>	VCC																		TOE	I/O G3 <5>	I/O G3 <4>	I/O G3 <3>	I/O G3 <6>	<b>L</b>	
<b>M</b>	I/O G3 <19>	I/O G3 <21>	I/O G3 <18>	I/O G3 <17>	I/O G3 <16>																		VCC	I/O G3 <10>	I/O G3 <9>	I/O G3 <7>	I/O G3 <8>	<b>M</b>	
<b>N</b>	I/O G3 <14>	I/O G3 <15>	I/O G3 <13>	I/O G3 <12>	VCC																		GOE <sub>3</sub>	I/O G2 <11>	QIOCLK <sub>3</sub>	I/O G3 <11>	VCCIO	<b>N</b>	
<b>P</b>	I/O G2 <12>	I/O G2 <13>	VCCIO	GOE <sub>1</sub>	QIOCLK <sub>1</sub>																		VCC	I/O G2 <10>	I/O G2 <9>	SET/RESET	I/O G2 <8>	<b>P</b>	
<b>R</b>	I/O G2 <16>	I/O G2 <17>	CLK <sub>1</sub>	I/O G2 <14>	VCC																		I/O G2 <7>	I/O G2 <6>	I/O G2 <5>	I/O G2 <3>	I/O G2 <4>	<b>R</b>	
<b>T</b>	I/O G2 <18>	I/O G2 <22>	I/O G2 <21>	I/O G2 <19>	I/O G2 <15>																		VCC	I/O G2 <0>	VCCIO	I/O G1 <0>	I/O G2 <1>	<b>T</b>	
<b>U</b>	I/O G2 <23>	VCCIO	I/O G1 <23>	I/O G1 <22>	VCC	I/O G0 <12>																	I/O G0 <11>	VCC	I/O G1 <5>	I/O G1 <4>	I/O G1 <3>	I/O G1 <2>	<b>U</b>
<b>V</b>	I/O G1 <20>	I/O G1 <19>	I/O G1 <18>	I/O G1 <17>	I/O G1 <16>	I/O G0 <16>																	VCCIO	I/O G1 <7>	I/O G1 <10>	I/O G1 <9>	I/O G1 <8>	I/O G1 <6>	<b>V</b>
<b>W</b>	I/O G1 <15>	I/O G1 <14>	I/O G1 <13>	I/O G1 <12>	I/O G1 <21>	I/O G2 <20>																	I/O G2 <2>	I/O G1 <1>	I/O G0 <8>	I/O G0 <9>	I/O G0 <10>	I/O G1 <11>	<b>W</b>
<b>Y</b>	I/O G0 <13>	I/O G0 <14>	I/O G0 <15>	VCCIO	VCC	NC <sup>1</sup>																	NC <sup>1</sup>	VCC	I/O G0 <4>	I/O G0 <5>	I/O G0 <6>	I/O G0 <7>	<b>Y</b>
<b>AA</b>	I/O G0 <17>	I/O G0 <18>	I/O G0 <19>	I/O G0 <20>	VCC	GND	VCCIO	NC <sup>1</sup>	NC <sup>1</sup>	VCC							VCC	NC <sup>1</sup>	NC <sup>1</sup>	VCCIO	GND	VCC	I/O G0 <0>	I/O G0 <1>	I/O G0 <2>	I/O G0 <3>	<b>AA</b>		
<b>AB</b>	I/O G0 <21>	I/O G0 <22>	I/O G0 <23>	NC <sup>1</sup>	GND	NC <sup>1</sup>	NC <sup>1</sup>	VCCIO	VCC	CLKEN	GND	VCC	VCCIO	GND	VCC	I/O B1 <10>	NC <sup>1</sup>	VCC	VCCIO	I/O B0 <10>	NC <sup>1</sup>	GND	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	<b>AB</b>		
<b>AC</b>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B4 <5>	I/O B4 <1>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B3 <8>	I/O B3 <2>	CLK <sub>0</sub>	I/O B2 <9>	I/O B2 <8>	I/O B2 <4>	I/O B1 <11>	I/O B1 <4>	I/O B1 <0>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B0 <7>	TMS	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	<b>AC</b>		
<b>AD</b>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B4 <11>	I/O B4 <8>	I/O B4 <4>	I/O B4 <0>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B3 <11>	I/O B3 <7>	I/O B3 <3>	NC <sup>1</sup>	I/O B2 <10>	I/O B2 <7>	I/O B2 <3>	I/O B1 <9>	I/O B1 <5>	I/O B1 <1>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B0 <8>	I/O B0 <4>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	<b>AD</b>		
<b>AE</b>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B4 <10>	I/O B4 <7>	I/O B4 <3>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B3 <10>	I/O B3 <6>	I/O B3 <4>	I/O B3 <0>	QIOCLK <sub>0</sub>	I/O B2 <10>	I/O B2 <5>	I/O B2 <1>	I/O B1 <8>	I/O B1 <6>	I/O B1 <2>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B0 <9>	I/O B0 <5>	I/O B0 <2>	I/O B0 <0>	NC <sup>1</sup>	<b>AE</b>	
<b>AF</b>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B4 <9>	I/O B4 <6>	I/O B4 <2>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B3 <9>	I/O B3 <5>	I/O B3 <1>	GOE <sub>0</sub>	I/O B2 <11>	I/O B2 <6>	I/O B2 <2>	I/O B2 <0>	I/O B1 <7>	I/O B1 <3>	NC <sup>1</sup>	NC <sup>1</sup>	NC <sup>1</sup>	I/O B0 <11>	I/O B0 <6>	I/O B0 <3>	I/O B0 <1>	TDI	<b>AF</b>		

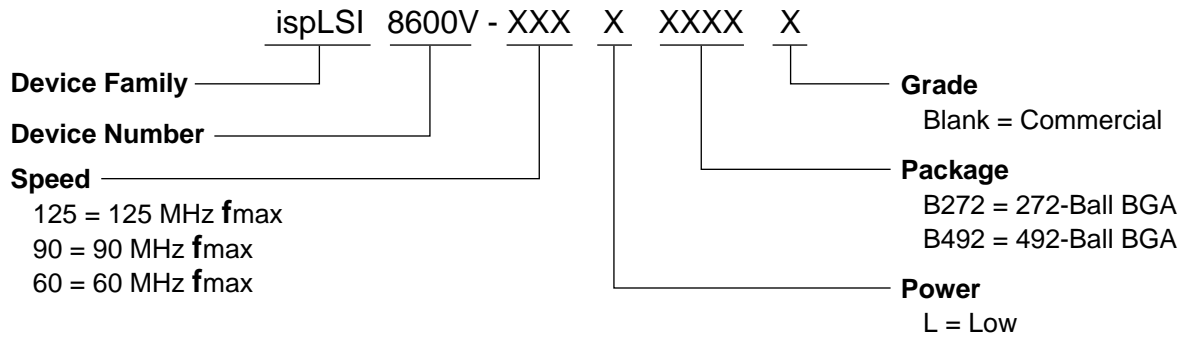
**ispLSI 8600V**  
Bottom View

1. NC pins are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability. [www.latticesemi.com/sales/discontinueddevicesales.cfm](http://www.latticesemi.com/sales/discontinueddevicesales.cfm)

**Part Number Description**



0212/8600V

**Ordering Information**

**COMMERCIAL**

FAMILY	f <sub>max</sub> (MHz)	t <sub>pd</sub> (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	8.5	ispLSI 8600V-125LB272	272-Ball BGA
	125	8.5	ispLSI 8600V-125LB492	492-Ball BGA
	90	10	ispLSI 8600V-90LB272	272-Ball BGA
	90	10	ispLSI 8600V-90LB492	492-Ball BGA
	60	15	ispLSI 8600V-60LB272	272-Ball BGA
	60	15	ispLSI 8600V-60LB492	492-Ball BGA

Table 2-0041/8600V

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.  
[www.latticesemi.com/sales/discontinueddevicesales.cfm](http://www.latticesemi.com/sales/discontinueddevicesales.cfm)