HARRIS

IRF350/351/352/353
IRF350R/351R/352R/353R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 13A and 15.0A, 350V - 400V
- $r_{DS}(on)$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

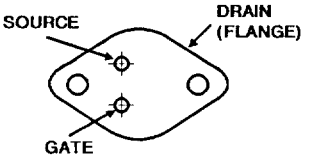
Description

The IRF350, IRF351, IRF352, and IRF353 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF350R, IRF351R, IRF352R and IRF353R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

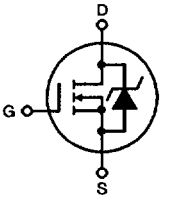
Package

TO-204AA



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF350 IRF350R	IRF351 IRF351R	IRF352 IRF352R	IRF353 IRF353R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	15	15	13	13	A
T_C = +100°C ..... I_D	9.0	9.0	8.0	8.0	A
Pulsed Drain Current (3) ..... I_{DM}	60	60	52	52	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	60	60	52	52	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	700	700	700	700	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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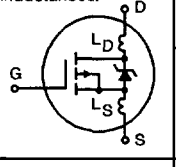
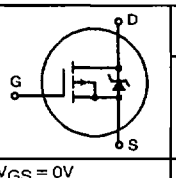
File Number 1826.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF350/352, IRF350R/352R	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	400	-	-	V
IRF351/353, IRF351R/353R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF350/351, IRF350R/351R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	15	-	-	A
IRF352/353, IRF352R/353R			13	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF350/351, IRF350R/351R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.0A	-	0.25	0.3	Ω
IRF352/353, IRF352R/353R			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)Max}$, I_D = 8.0A	8.0	10	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	2000	-	pF
Output Capacitance	C_{OSS}		-	400	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 180V, I_D = 8.0A, Zo = 4.7Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	-	35	ns
Rise Time	t_r		-	-	65	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	150	ns
Fall Time	t_f		-	-	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	79	120	nC
Gate-Source Charge	Q_{gs}		-	38	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	41	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	15	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	60	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 15A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/μs	-	1000	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/μs	-	6.6	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 40V, Start T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A (See Figure 15)

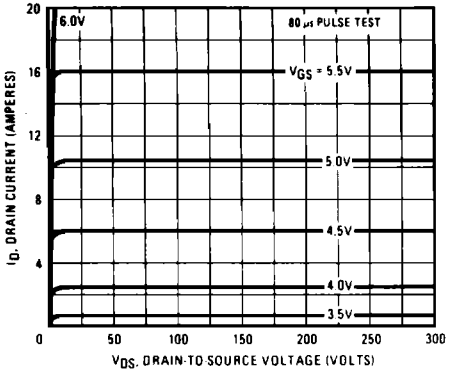


Fig. 1 – Typical Output Characteristics

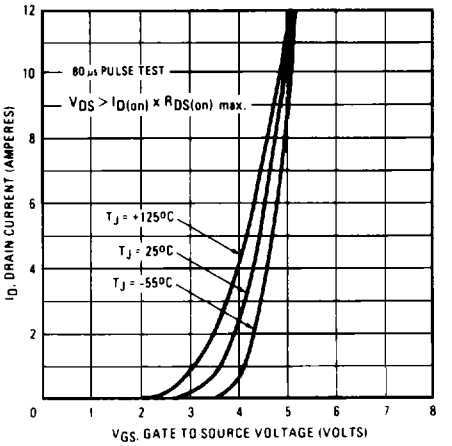


Fig. 2 – Typical Transfer Characteristics

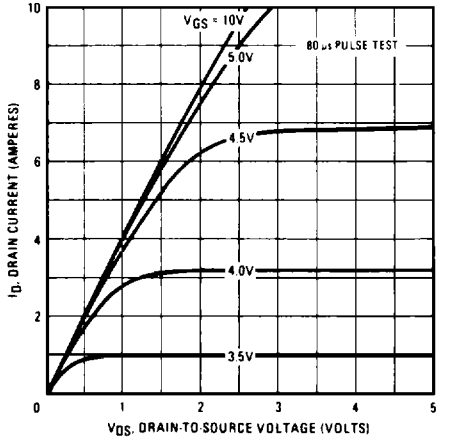


Fig. 3 – Typical Saturation Characteristics

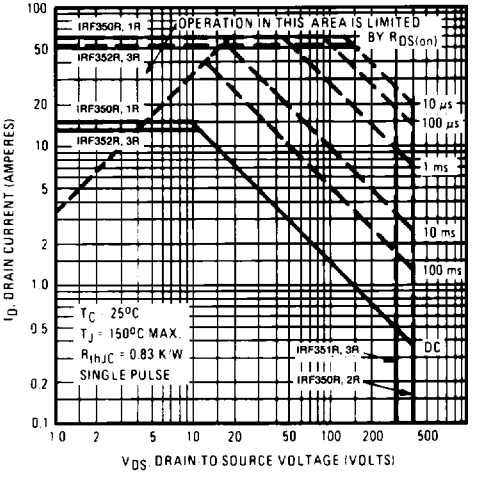


Fig. 4 – Maximum Safe Operating Area

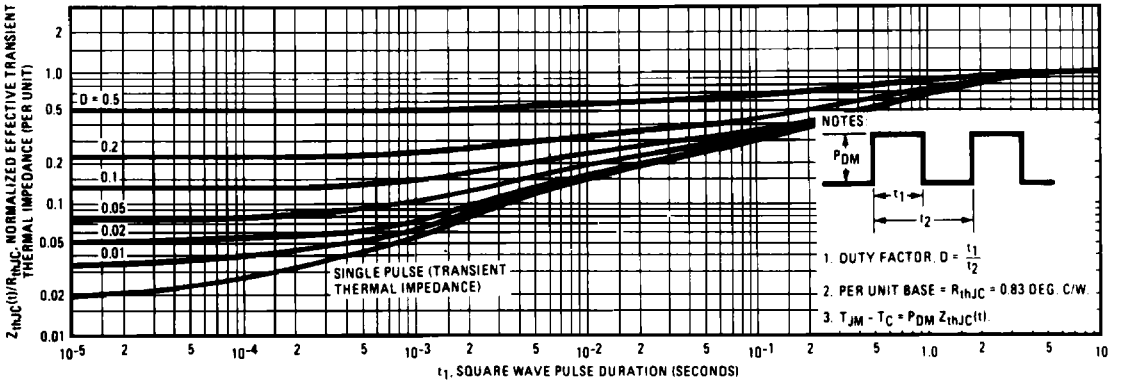


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

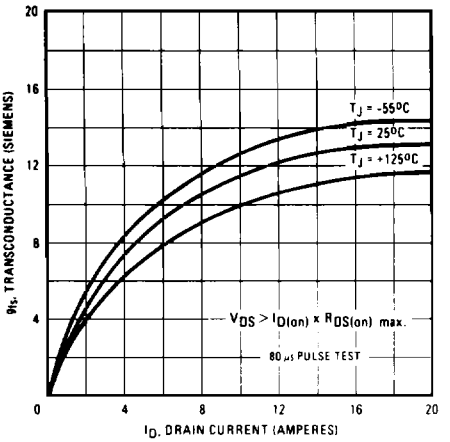


Fig. 6 – Typical Transconductance Vs. Drain Current

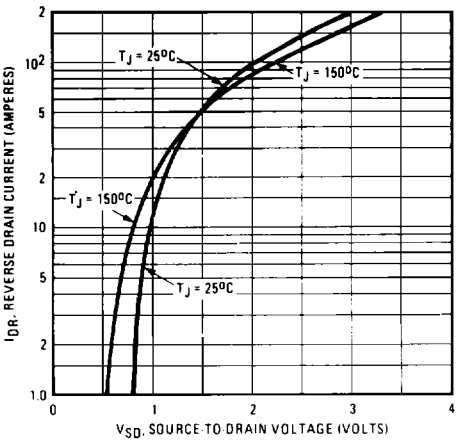


Fig. 7 – Typical Source-Drain Diode Forward Voltage

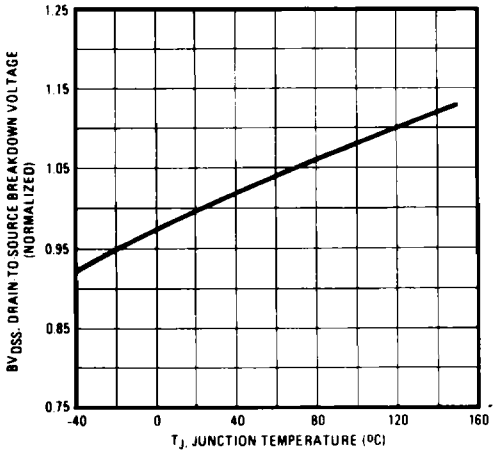


Fig. 8 – Breakdown Voltage Vs. Temperature

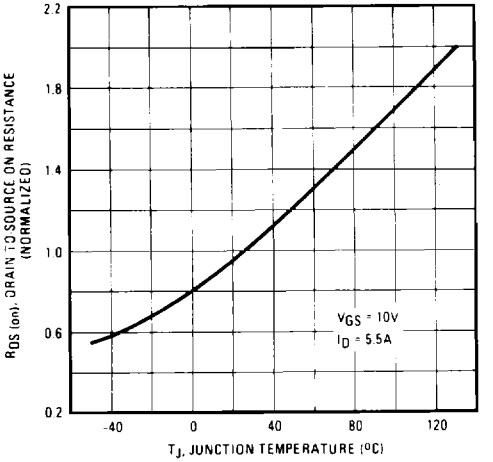


Fig. 9 – Normalized On-Resistance Vs. Temperature

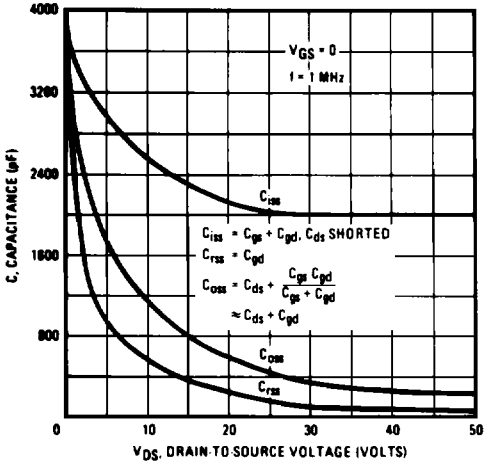


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

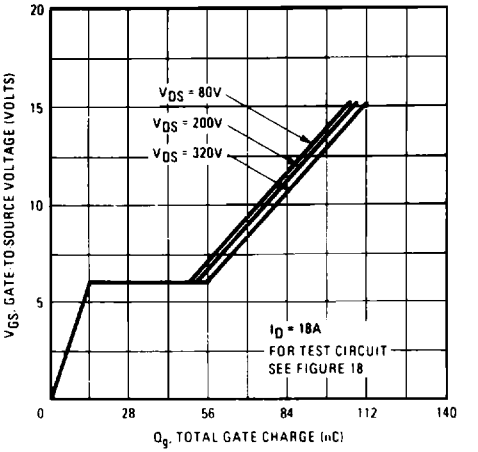


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

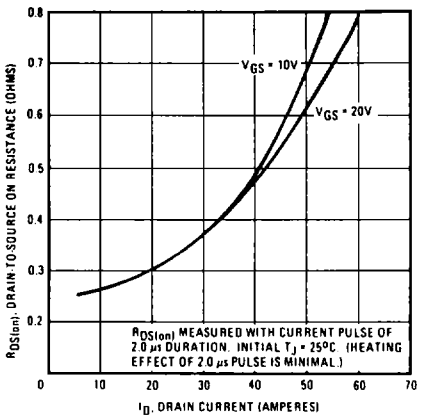


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

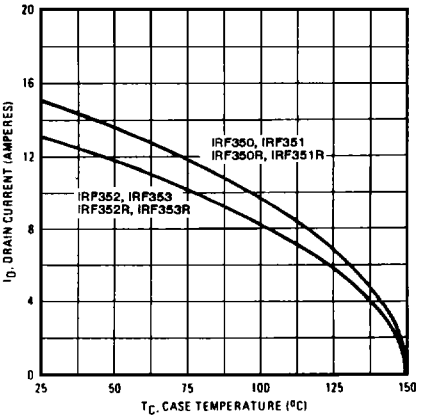


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

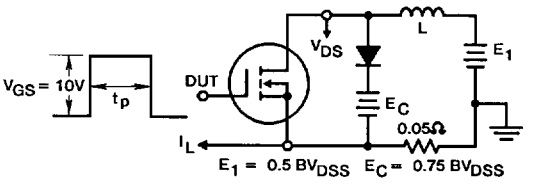


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

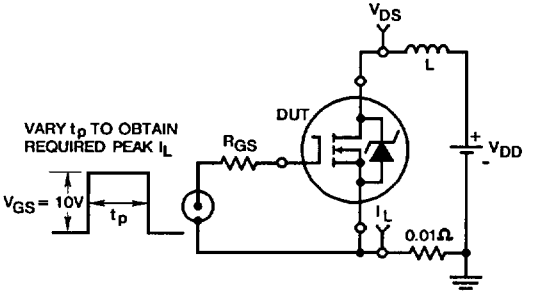


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

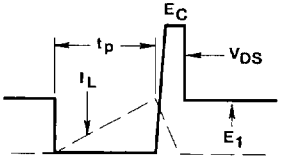


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

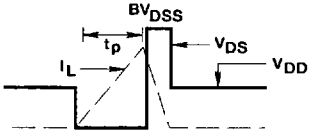


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

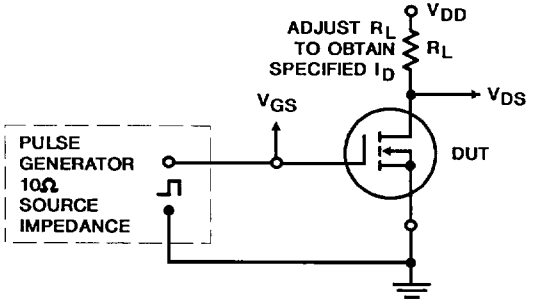


FIGURE 16. SWITCHING TIME TEST CIRCUIT

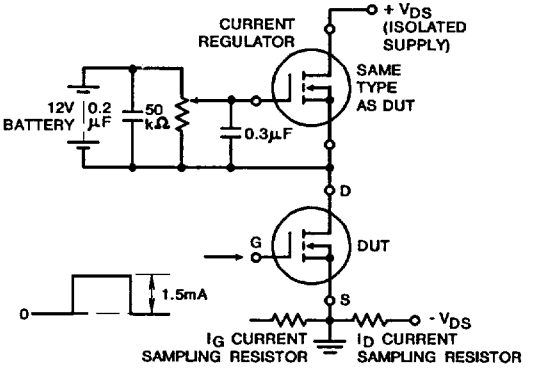


FIGURE 17. GATE CHARGE TEST CIRCUIT