IRFU9110, IRFR9110

3.1A, 100V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

January 1996

Features

- 3.1A, 100V
- $r_{DS(ON)}$ = 1.200Ω
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The IRFU9110 and IRFR9110 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specific level of energy in the avalanche breakdown mode of operation. These are P-Channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

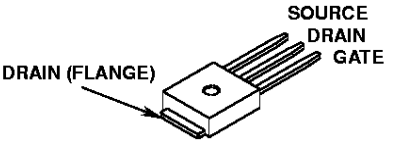
PART NUMBER	PACKAGE	BRAND
IRFU9110	TO-251AA	IF9110
IRFR9110	TO-252AA	IF9110

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., IRFR91109A.

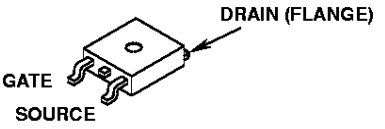
Formerly developmental type TA17541.

Packaging

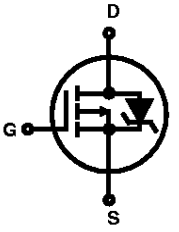
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings T_C = +25°C

		IRFU9110, IRFR9110	UNITS
Drain Source Voltage	V_{DSS}	-100	V
Drain Gate Voltage	V_{DGR}	-100	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	3.1	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
T_C = +25°C	P_D	25	W
Derate above +25°C		0.2	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4001.2**

Electrical Specifications

T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		-100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100V, V_{GS} = 0V	T_C = +25°C	-	-	-1	μA
			T_C = +150°C	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 1.9A, V_{GS} = -10V		-	-	1.200	Ω
Turn-On Time	t_{ON}	V_{DD} = -50V, I_D = 4A, R_L = 11Ω, V_{GS} = -10V, R_{GS} = 24Ω		-	-	50	ns
Turn-On Delay Time	$t_{D(ON)}$			-	10	-	ns
Rise Time	t_R			-	27	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	15	-	ns
Fall Time	t_F			-	17	-	ns
Turn-Off Time	t_{OFF}			-	-	50	ns
Total Gate Charge	Q_G	V_{GS} = 0 to -10V	V_{DD} = -80V, I_D = 3.1A, R_L = 25.8Ω	-	-	8.7	nC
Gate-to-Drain Charge	Q_{GD}			-	-	4.1	nC
Gate-to-Source Charge	Q_{GS}			-	-	2.2	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz		-	290	-	pF
Output Capacitance	C_{OSS}			-	94	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	18	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	5.00	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	100	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = -3.1A	-	-	-5.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = -4.0A, dI_{SD}/dt = -100A/μs	-	105	160	ns
Reverse Recovery Charge	Q_{RR}			0.51	1.0	μC

Typical Performance Curves

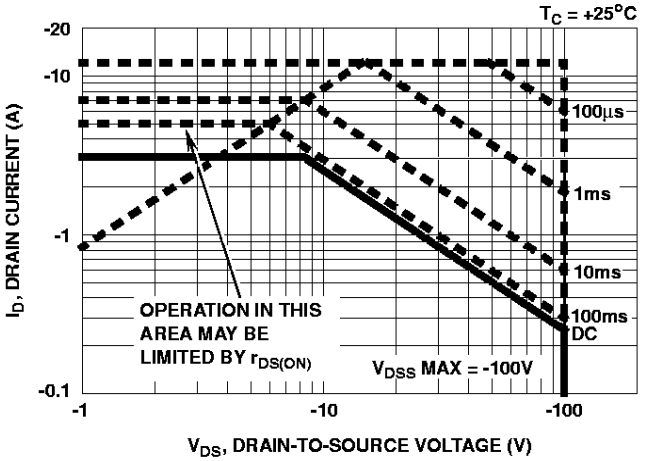


FIGURE 1. SAFE OPERATING AREA CURVE

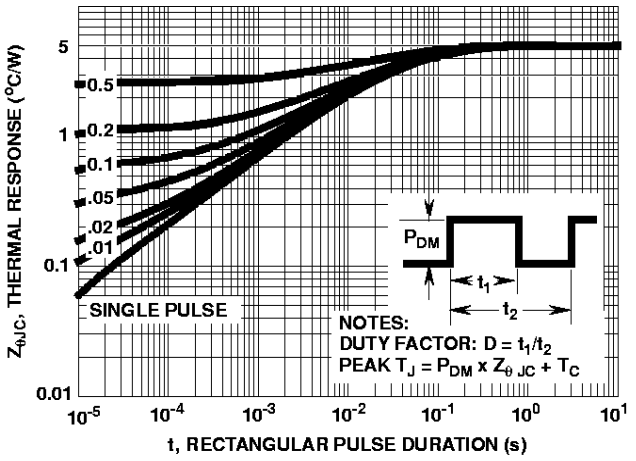


FIGURE 2. MAXIMUM TRANSIENT THERMAL IMPEDANCE

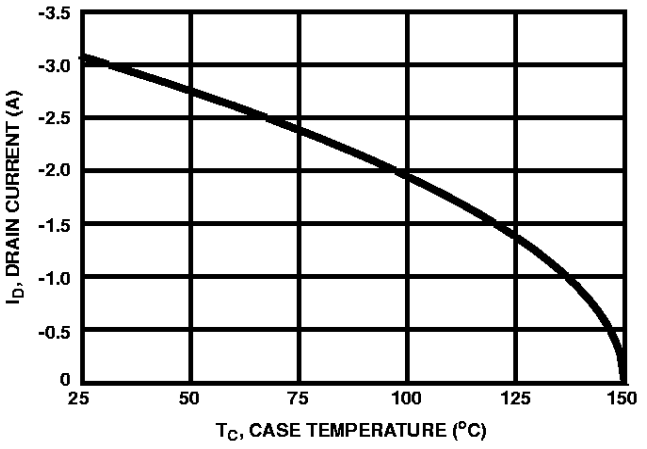


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

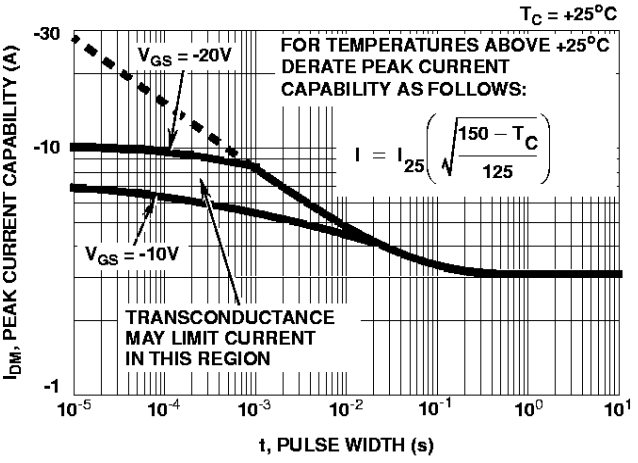


FIGURE 4. PEAK CURRENT CAPABILITY

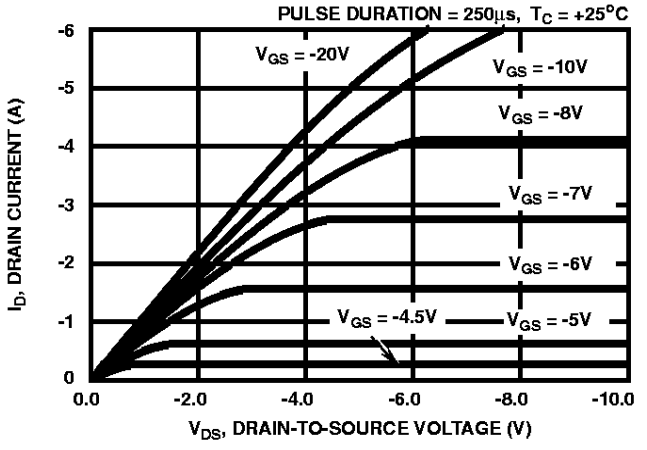


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

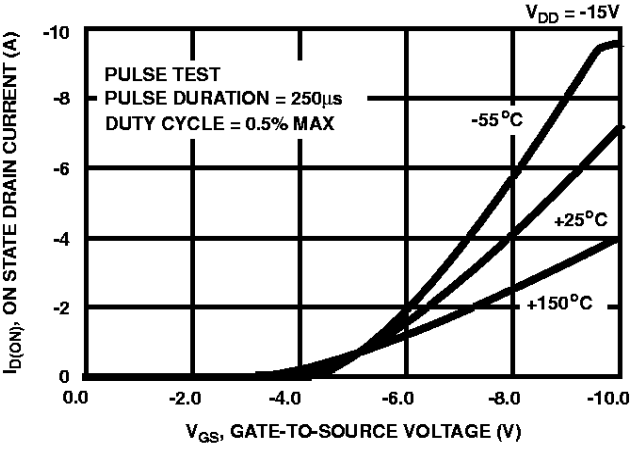


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

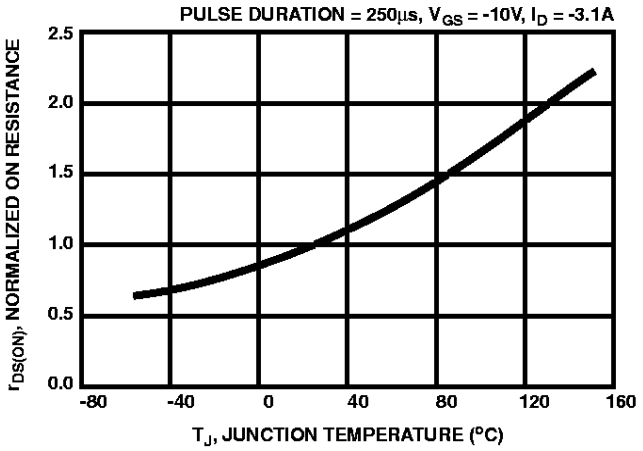


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

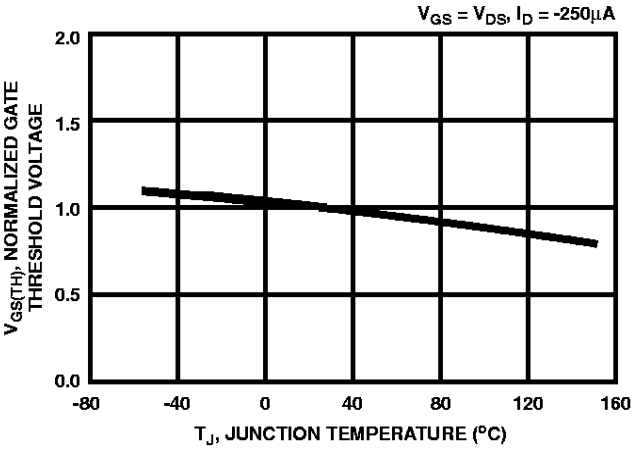


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

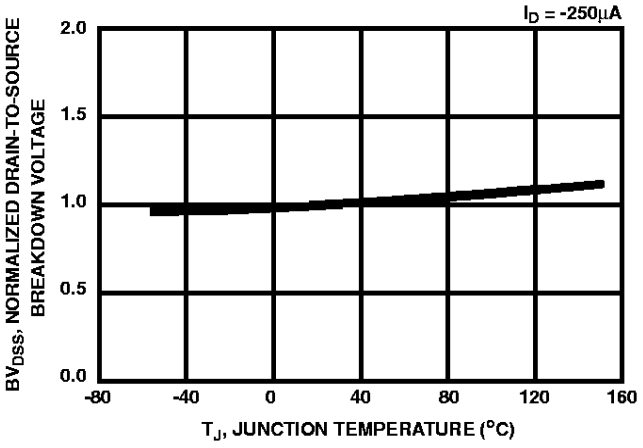


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

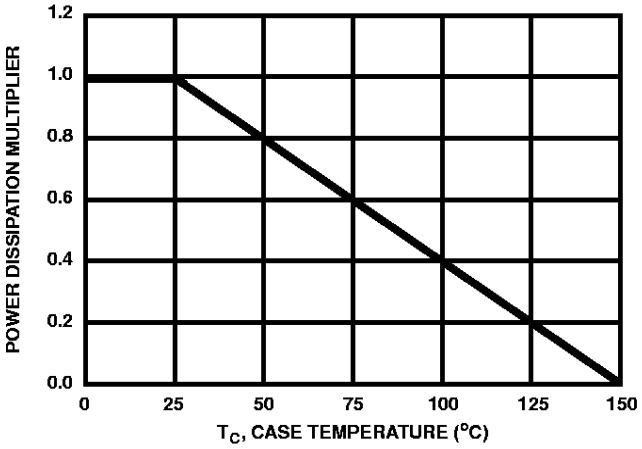


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

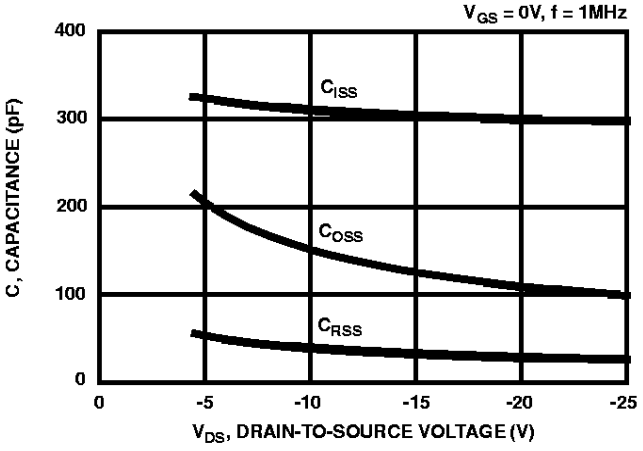


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

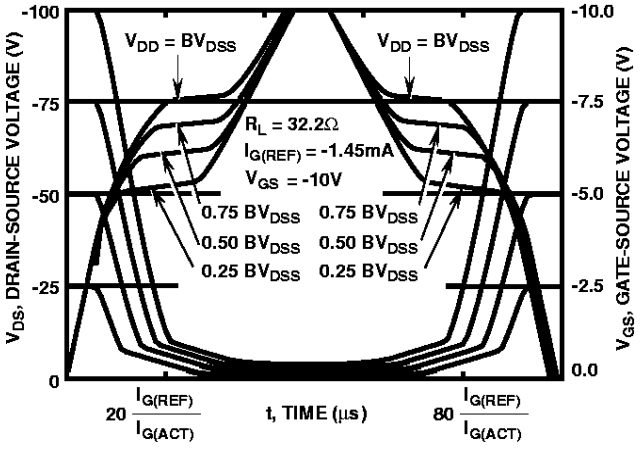


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

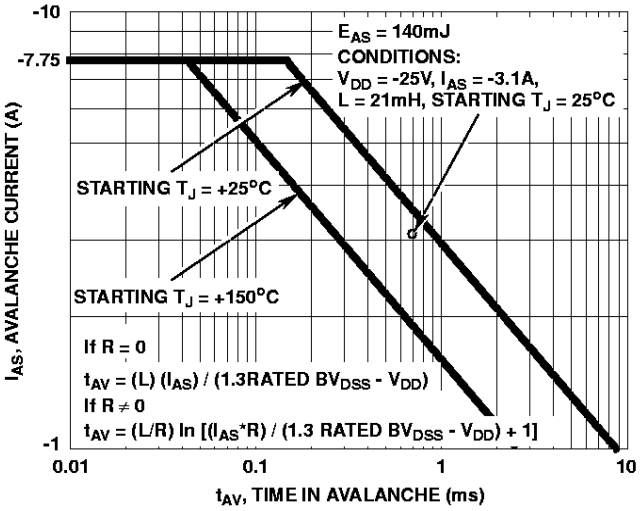


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

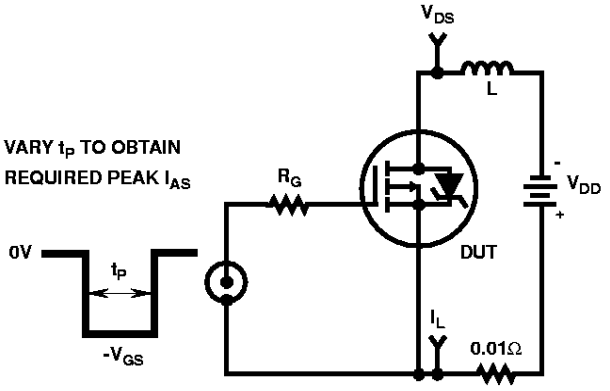


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

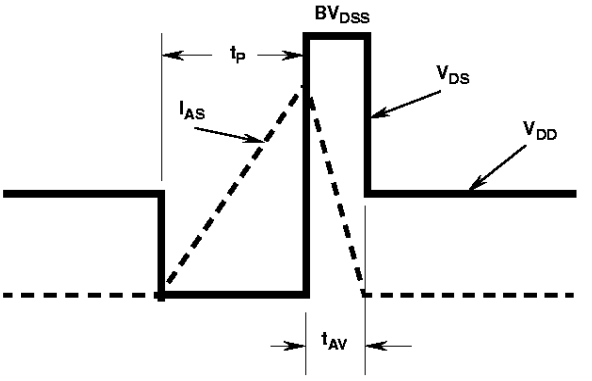


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

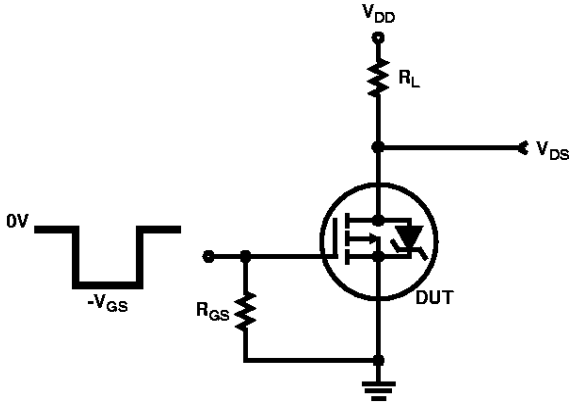


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

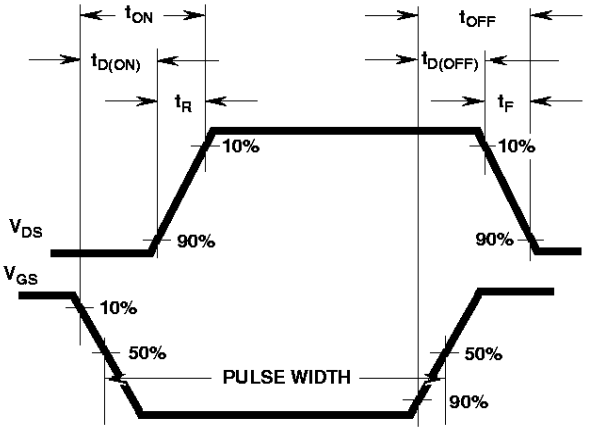


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSpice Model Listing for the IRFU9110, IRFR9110

.SUBCKT IRFU9110 2 1 3 REV 9/21/94

CA 12 8 3.49e-10
CB 15 14 3.52e-10
CIN 6 8 2.71e-10
DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -131.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

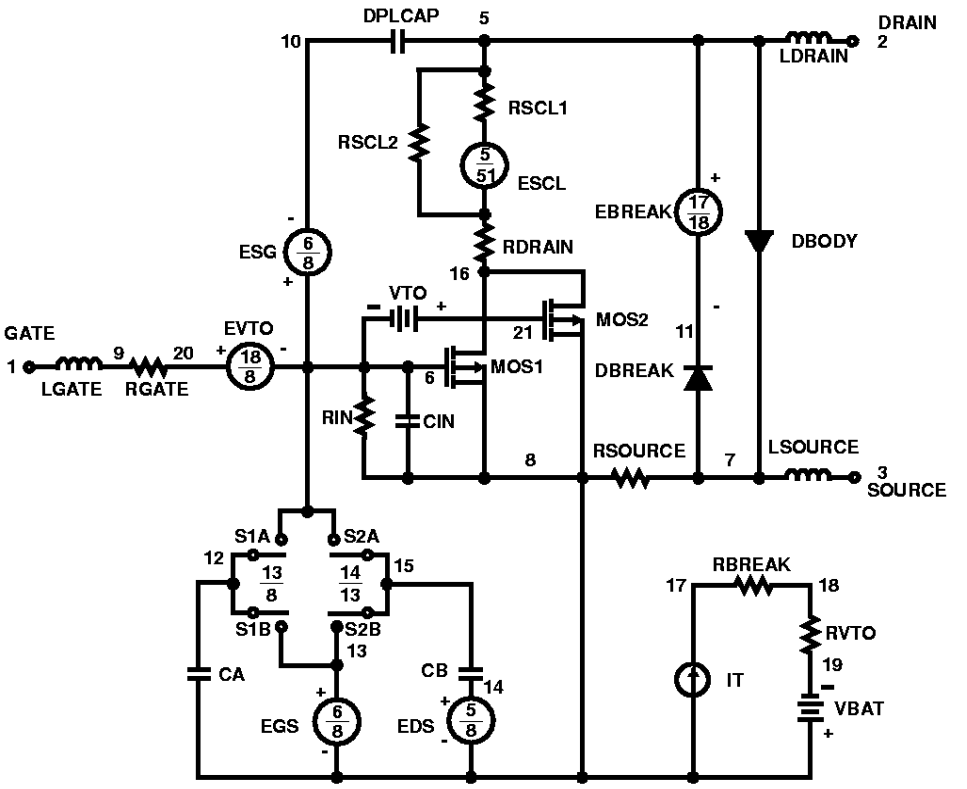
LDRAIN 2 5 1e-9
LGATE 1 9 2.9e-9
LSOURCE 3 7 2.9e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 497e-3
RGATE 9 20 2.68
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 348e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.9



ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/6.3,6))}

.MODEL DBDMOD D (IS=1.23e-14 RS=8.74e-2 TRS1=-1.95e-3 TRS2=-9.30e-6 CJO=3.72e-10 TT=1.45e-7)
.MODEL DBKMOD D (RS=2.76 TRS1=8.39e-4 TRS2=-1.87e-5)
.MODEL DPLCAPMOD D (CJO=1.31e-10 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.68 KP=0.98 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=7.25e-4 TC2=2.03e-6)
.MODEL RDSMOD RES (TC1=6.95e-3 TC2=3.07e-5)
.MODEL RSCLMOD RES (TC1=1e-3 TC2=0)
.MODEL RVTOMOD RES (TC1=3.46e-3 TC2=5.67e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=5.03 VOFF=3.03)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.03 VOFF=5.03)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.30 VOFF=-5.30)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.30 VOFF=-0.30)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.