HARRIS

RFG75N05E
RFH75N05E

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

January 1993

Features

- 75A, 50V
- $r_{DS(on)} = 0.008\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

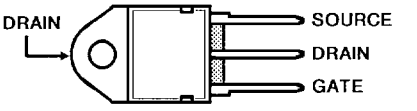
Description

The RFG75N05E and RFH75N05E n-channel ESD rated power MOSFET's are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

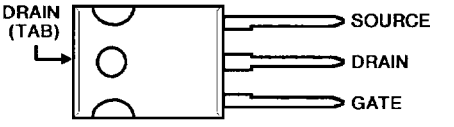
The RFG75N05E is supplied in the TO-247 style (3 lead) plastic package and the RFH75N05E is supplied in the TO-218 (3 lead) plastic package.

Package

TO-218
TOP VIEW

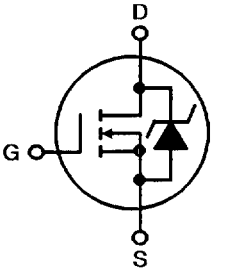


TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFG75N05E RFH75N05E	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	V
Continuous Drain Current	I_D	75*	A
Pulsed Drain Current	I_{DM}	200	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	240	W
Derated Above +25°C		1.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C
Electrostatic Discharge Rating			
MIL-STD-883, Category B(2)	E_{SD}	2	kV
Single-Pulse Avalanche Rating		Refer to UIS SOA Curves	

*I_D Current Limited by Package

File Number 2275.3

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V		-	-	1	µA
		T_C =+150°C		-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 75A, V_{GS} = 10V		-	-	0.008	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 37.5A		-	-	125	ns
Turn-On Delay Time	$t_{d(on)}$	R_L = 0.67Ω		-	17	-	ns
Rise Time	t_r	$I_{G1} = I_{G2}$ = 3A		-	75	-	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS(clamp)}$ = +10V, -0.6V		-	70	-	ns
Fall Time	t_f			-	17	-	ns
Turn-Off Time	$t_{(off)}$			-	-	125	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0, 20V	V_{DD} = 40V	-	-	400	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0, 10V	I_D = 75A	-	-	220	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0, 2V	R_L = 0.53Ω	-	-	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 75A, V_{DS} = 15V		-	-	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 37.5A, $I_{G1} = I_{G2}$ = 3A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 0.67Ω		-	-	300	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.625	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 75A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 75A, dI_f/dt = 100A/µs	-	-	125	ns

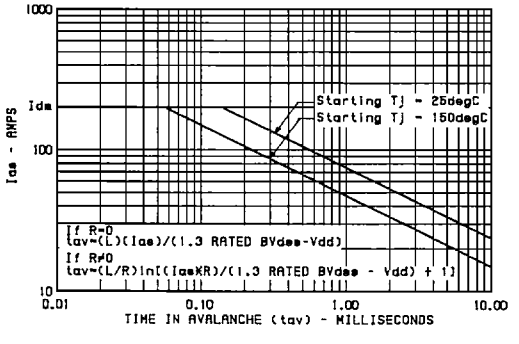


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

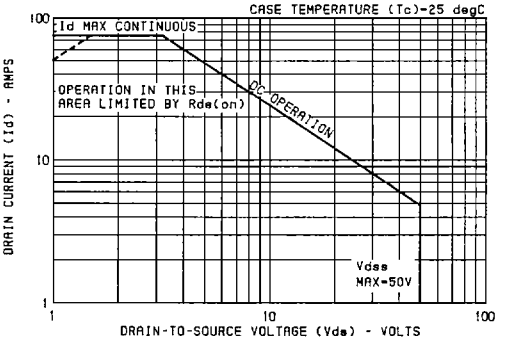


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

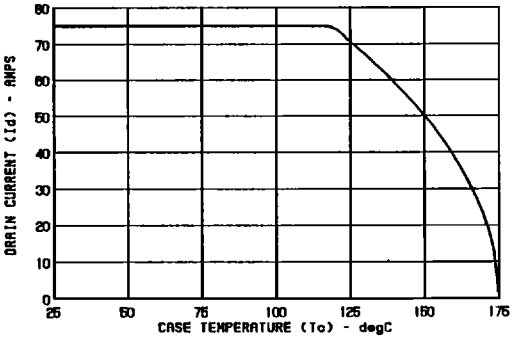


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

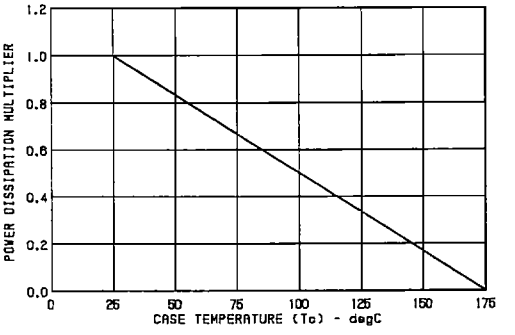


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

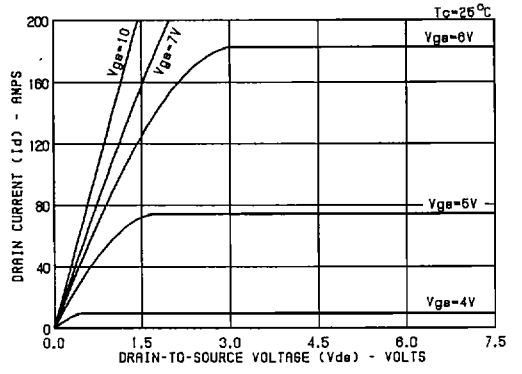


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

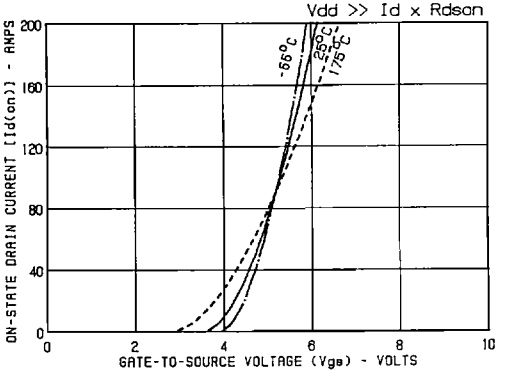


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

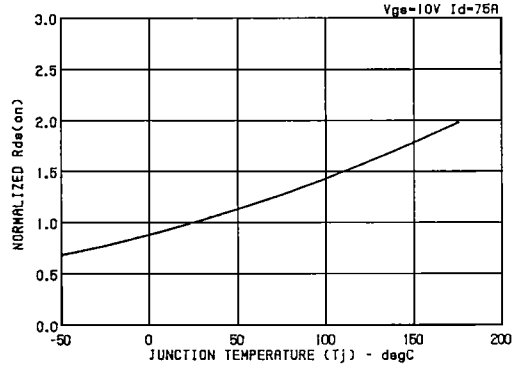


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

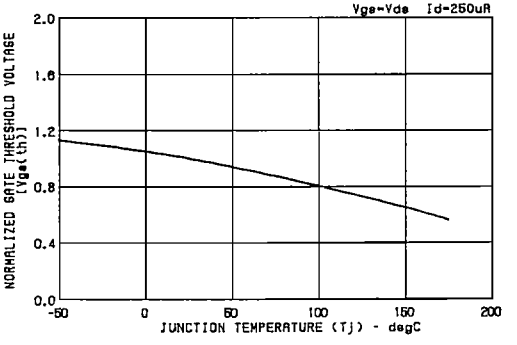


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

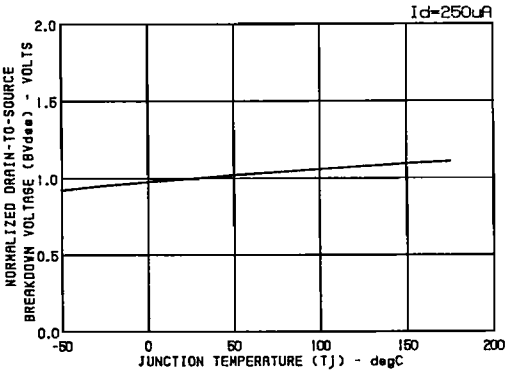


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

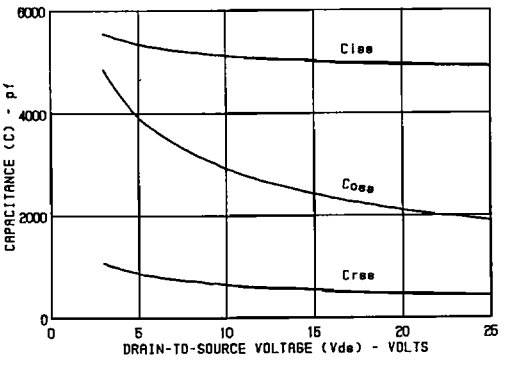


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

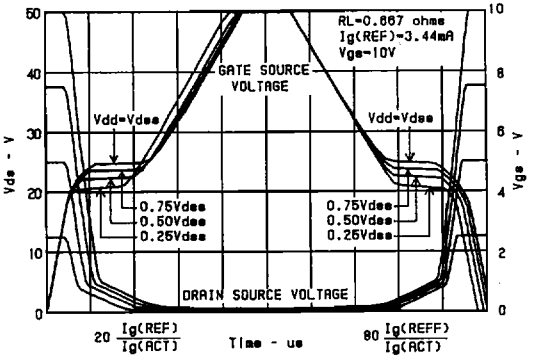


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)

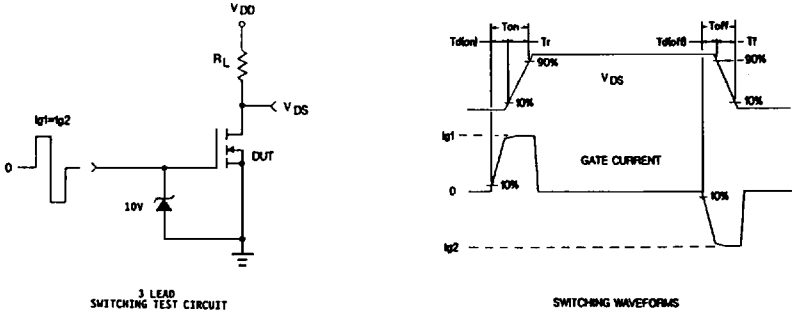


FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)

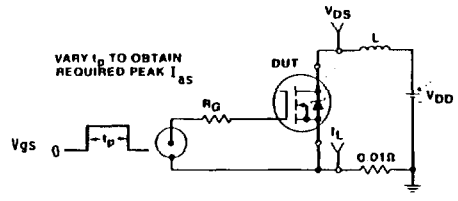


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

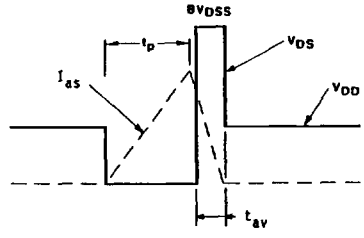
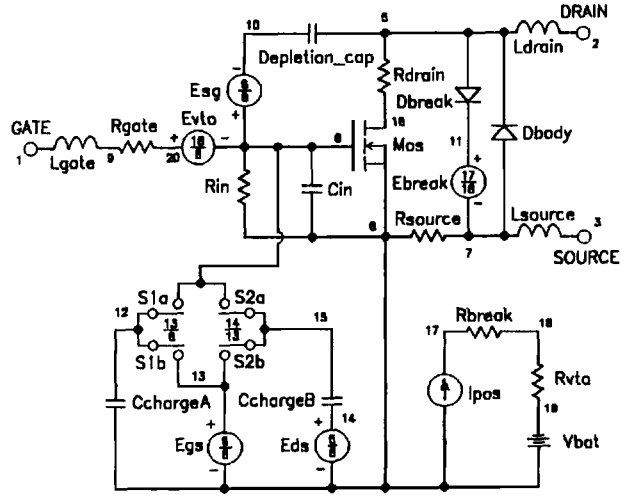


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

Spice Model

```
.SUBCKT RFH75N05  2  1  3  ;  rev 10/30/90
*Nominal Temperature = 25°C
CchargeA  12  8  8.98e-9
CchargeB  15  14  8.81e-9
Cin  6  8  4.48e-9
Depletion_cap  10  5  DPLCAPMOD
Dbody  7  5  DBODYMOD
Dbreak  5  11  DBREAKMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Ebreak  11  7  17  18  58.4
Evto  20  6  18  8  1
Ipos  8  17  1
Ldrain  2  5  e-10
Lgate  1  9  5e-9
Lsource  3  7  3e-9
Mos  16  6  8  8  MOSMOD
Rbreak  17  18  RBREAKMOD  1
Rdrain  5  16  RSOURCEMOD  3.07e-3
Rgate  9  20  1.2
Rin  6  8  1e9
Rsource  8  7  RSOURCEMOD  2.e-3
Rvto  18  19  RVTONEGMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.MODEL  S1AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.48  VOFF=-0.48)
.MODEL  S1BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-0.48  VOFF=-2.48)
.MODEL  S2AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=2.75)
.MODEL  S2BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=2.75  VOFF=-2.25)
.MODEL  DBODYMOD  D  (IS=2.23e-12  RS=249e-3  TRS1=2.5e-3  CJO=7.55e-9  TT=4e-8)
.MODEL  DBREAKMOD  D  (RS=8e-2  TRS1=2.5e-3)
.MODEL  DPLCAPMOD  D  (IS=1e-30  N=10  CJO=2.14e-9)
.MODEL  RBREAKMOD  RES  (TC1=9.5e-4  TC2=-1.17e-6)
.MODEL  RSOURCEMOD  RES  (TC1=5.2e-3  TC2=1.37e-5)
.MODEL  RVTONEGMOD  RES  (TC1=-3.78e-3  TC2=-7.51e-7)
.MODEL  MOSMOD  NMOS  (VTO=3.48  N=10  IS=1e-30  KP=78.5  TOX=1  L=1u  W1u)
.ENDS
```



4 N-CHANNEL POWER MOSFETs