

January 1998

Features

- 20A and 23A, 400V
- $r_{DS(ON)} = 0.2\Omega$ and 0.25Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFP360	TO-247	IRFP360
IRFP362	TO-247	IRFP362

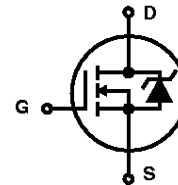
NOTE: When ordering, use the entire part number.

Description

These are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. They can be operated directly from integrated circuits.

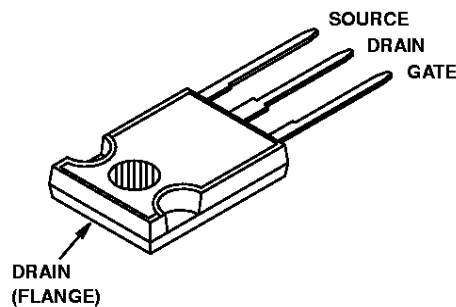
Formerly developmental type TA17464.

Symbol



Packaging

JEDEC STYLE TO-247



IRFP360, IRFP362

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	IRFP360	IRFP362	UNITS
Drain to Source Voltage (Note 1)	400	400	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	400	400	V
Continuous Drain Current	23	20	A
$T_C = 100^\circ\text{C}$	14	13	A
Pulsed Drain Current (Note 3)	92	80	A
Gate to Source Voltage	± 20	± 20	V
Maximum Power Dissipation	250	250	W
Linear Derating Factor	2	2	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4)	1200	1200	mJ
Operating and Storage Temperature	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from case for 10s	300	300	300
Package Body for 10s, see Techbrief 334	260	260	260

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

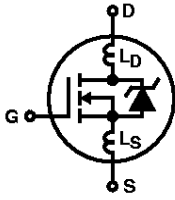
1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

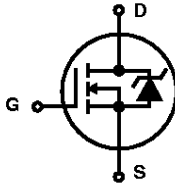
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, (Figure 10)	400	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2	-	4	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$	-	-	25	μA	
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$	-	-	250	μA	
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = 10\text{V}$	IRFP360	23	-	-	A
			IRFP362	20	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA	
On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 13\text{A}$, $V_{GS} = 10\text{V}$, (Figures 8, 9)	IRFP360	-	0.18	0.20	Ω
			IRFP362	-	0.20	0.25	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50\text{V}$, $I_{DS} > 13\text{A}$, (Figure 12)	14	21	-	S	
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 200\text{V}$, $I_D \approx 25\text{A}$, $R_{GS} = 4.3\Omega$, $V_{GS} = 10\text{V}$ $R_L = 7.5\Omega$, (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	22	33	ns	
Rise Time	t_r		-	94	140	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns	
Fall Time	t_f		-	66	99	ns	
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 10\text{V}$, $I_D = 25\text{A}$, $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $I_{G(REF)} = 1.5\text{mA}$, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	68	100	nC	
Gate to Source Charge	Q_{gs}		-	17	-	nC	
Gate to Drain "Miller" Charge	Q_{gd}		-	24	-	nC	

IRFP360, IRFP362

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$, (Figure 11)		-	4000	-	pF
Output Capacitance	C_{OSS}			-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	97	-	pF
Internal Drain Inductance	L_D	Measured Between the Contact Screw on Header closer to Source and Gate Pins and Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 6mm (0.25in) from Header and Source Bonding Pad		-	13	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.50	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	30	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier 	-	-	23	A	
Pulse Source to Drain Current (Note 2)	I_{SDM}		-	-	92	A	
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 23\text{A}$, $V_{GS} = 0\text{V}$, (Figure 13)		-	-	1.8	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_{SD} = 25\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		200	460	1000	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^\circ\text{C}$, $I_{SD} = 25\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		3.1	7.1	16	μC

NOTES:

2. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 50\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 4\text{mH}$, $R_G = 25\Omega$, Peak $I_{AS} = 23\text{A}$ (Figures 15, 16).

IRFP360, IRFP362

Typical Performance Curves Unless Otherwise Specified

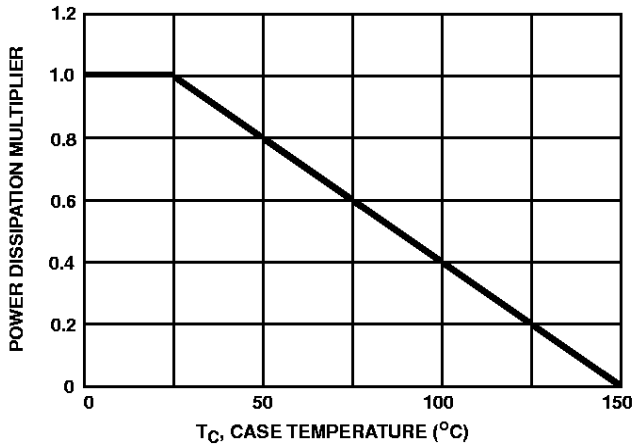


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

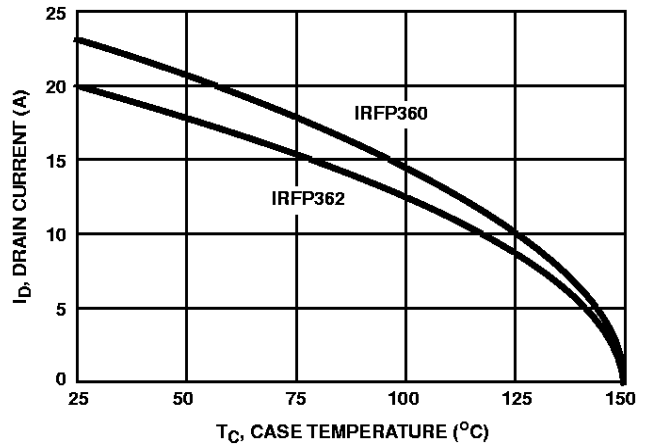


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

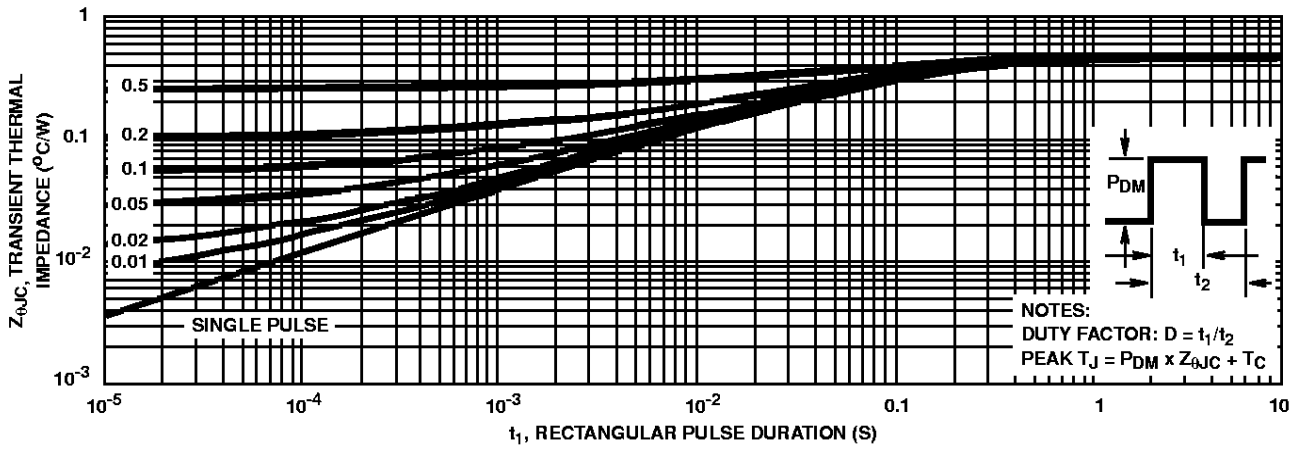


FIGURE 3. TRANSIENT THERMAL IMPEDANCE

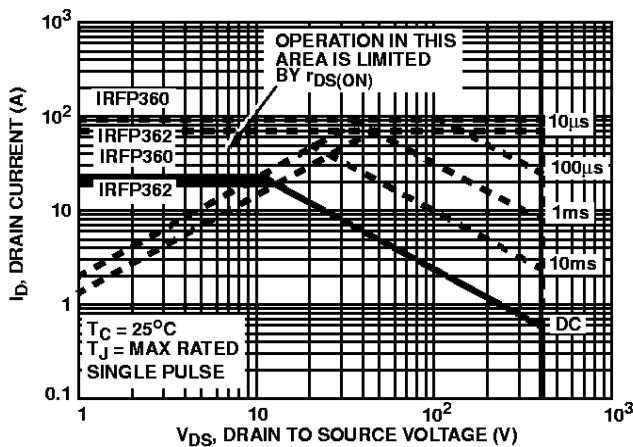


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

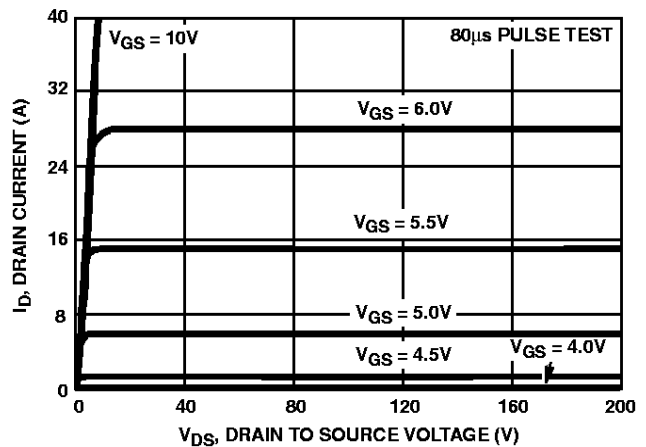


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

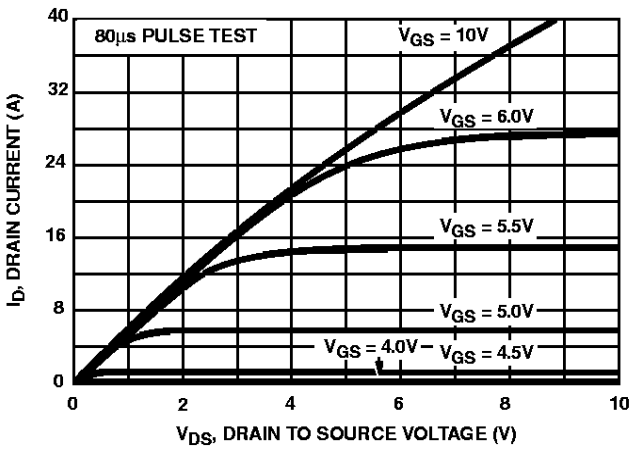


FIGURE 6. SATURATION CHARACTERISTICS

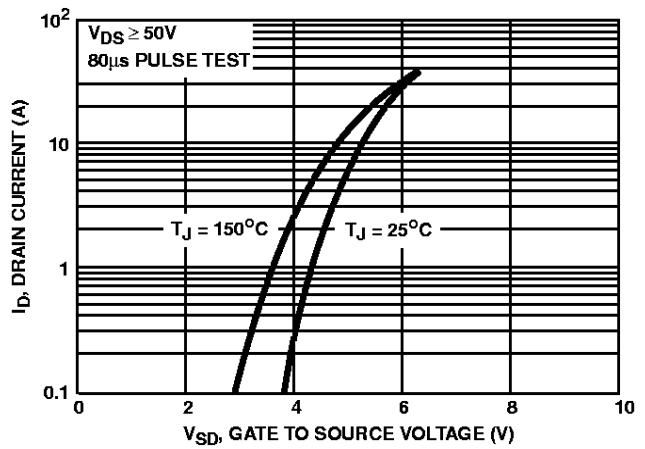


FIGURE 7. TRANSFER CHARACTERISTICS

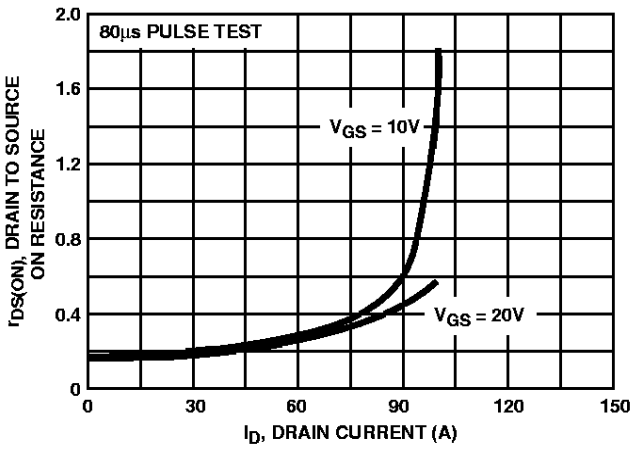


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

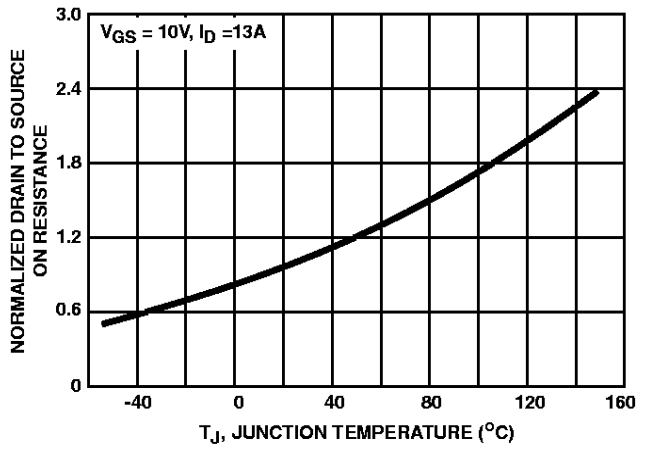


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

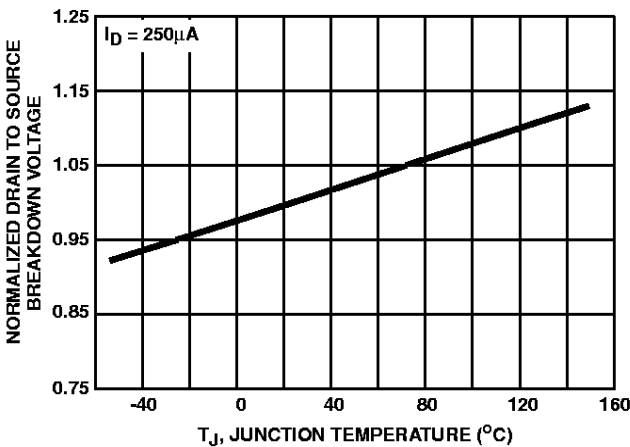


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

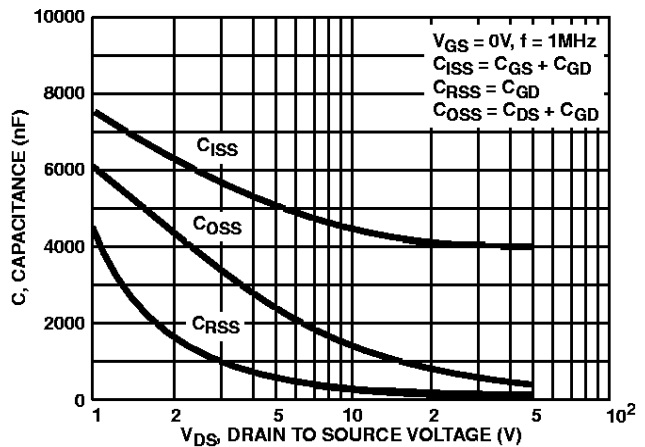


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

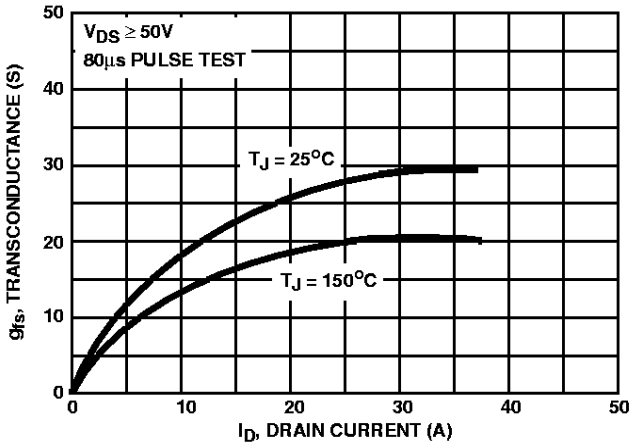


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

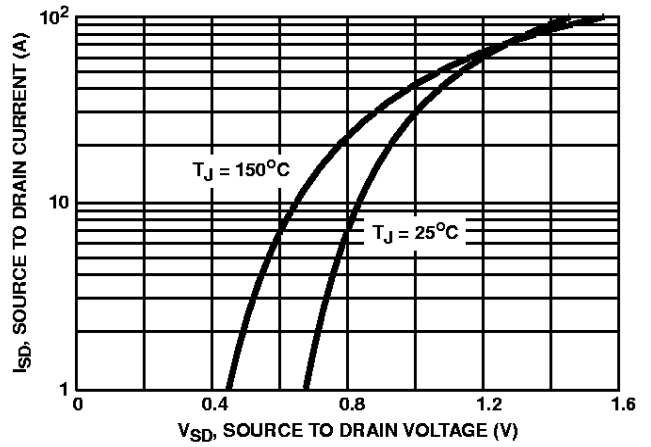


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

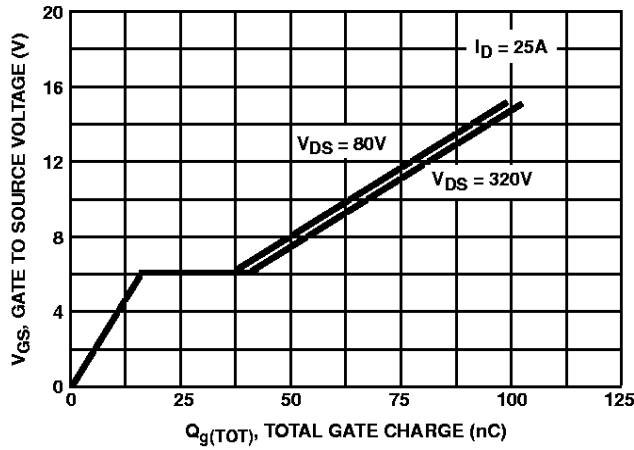


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

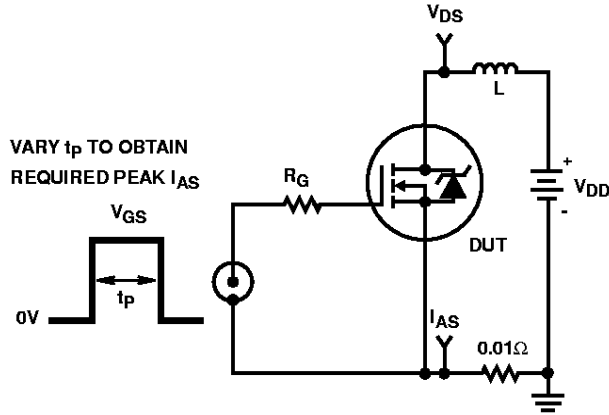


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

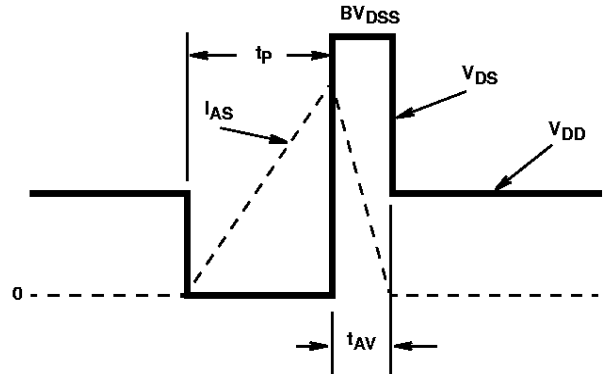


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

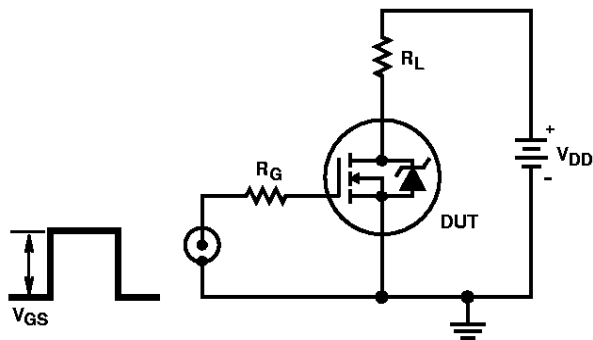


FIGURE 17. SWITCHING TIME TEST CIRCUIT

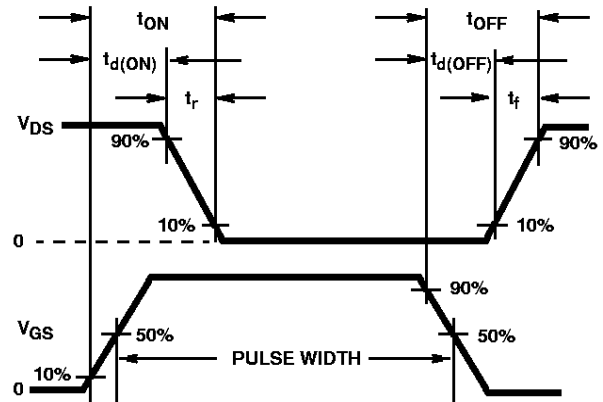


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

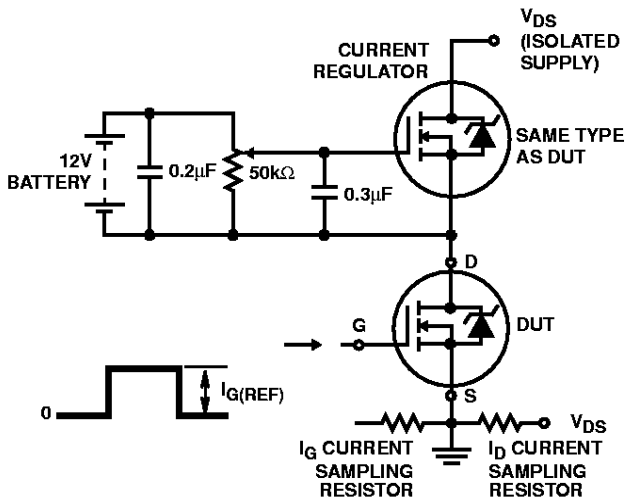


FIGURE 19. GATE CHARGE TEST CIRCUIT

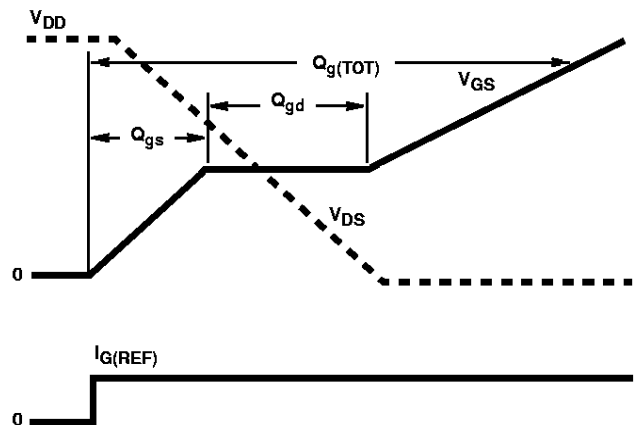


FIGURE 20. GATE CHARGE WAVEFORMS