HARRIS

IRF830/831/832/833
IRF830R/831R/832R/833R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- **4.0A and 4.5A, 450V - 500V**
- **$r_{DS}(on) = 1.5\Omega$ and 2.0Ω**
- **Single Pulse Avalanche Energy Rated***
- **SOA is Power-Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**

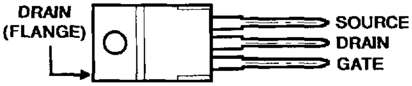
Description

The IRF830, IRF831, IRF832, and IRF833 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF830R, IRF831R, IRF832R and IRF833R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

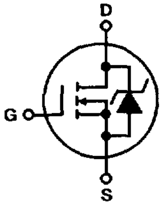
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

		IRF830 IRF830R	IRF831 IRF831R	IRF832 IRF832R	IRF833 IRF833R	UNITS
Drain-Source Voltage (1)	V_{DS}	500	450	500	450	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR}	500	450	500	450	V
Continuous Drain Current						
$T_C = +25^oC$	I_D	4.5	4.5	4.0	4.0	A
$T_C = +100^oC$	I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3)	I_{DM}	18	18	16	16	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
$T_C = +25^oC$	P_D	75	75	75	75	W
Linear Derating Factor		0.6	0.6	0.6	0.6	W/^oC
Inductive Current, Clamped (See Figure 14, L = 100µH)	I_{LM}	18	18	16	16	A
Single Pulse Avalanche Energy Rating (4)	E_{AS}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^oC
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	^oC

NOTES:

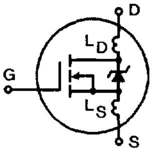
1. $T_J = +25^oC$ to $+150^oC$.
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. $V_{DD} = 50V$, starting $T_J = +25^oC$, $L = 25mH$, $R_{GS} = 25\Omega$, $I_{PEAK} = 4.5A$. See Figure 15.

*R Suffix Types Only

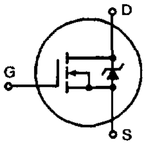
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **1582.1**

Electrical Characteristics $T_C = 25^oC$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF830/832, IRF830R/832R	BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	500	-	-	V
IRF831/833, IRF831R/833R			450	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = -20V$	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, $V_{GS} = 0V$	-	-	250	µA
		V_{DS} = Max Rating x 0.8, $V_{GS} = 0V$, $T_J = +125^oC$	-	-	1000	µA
On-State Drain Current (Note 2) IRF830/831, IRF830R/831R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times R_{DS(ON)}$ Max, $V_{GS} = 10V$	4.5	-	-	A
IRF832/833, IRF832R/833R			4.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF830/831, IRF830R/831R	$r_{DS(ON)}$	$V_{GS} = 10V$, $I_D = 2.5A$	-	1.3	1.5	Ω
IRF832/833, IRF832R/833R			-	1.5	2.0	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, $I_D = 2.5A$	2.7	4.2	-	S(℧)
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 250V$, $I_D = 4.5A$, $R_G = 12\Omega$ See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	10	17	ns
Rise Time	t_r		-	15	23	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	33	53	ns
Fall Time	t_f		-	16	23	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = 10V$, $I_D = 4.5A$, $V_{DS} = 0.8V$ Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	22	32	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	11	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die Modified MOSFET symbol showing the internal device inductances. 	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	4.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	18	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_J = +25^oC$, $I_S = 4.5A$, $V_{GS} = 0V$	-	-	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = +25^oC$, $I_F = 4.5A$, $dI_F/dt = 100A/\mu s$	180	350	760	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +25^oC$, $I_F = 4.5A$, $dI_F/dt = 100A/\mu s$	0.96	2.2	4.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. $T_J = +25^oC$ to $+150^oC$

2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

4. $V_{DD} = 50V$, Start $T_J = +25^oC$, $L = 25mH$, $R_{GS} = 25\Omega$, $I_{PEAK} = 4.5A$ (See Figure 15)

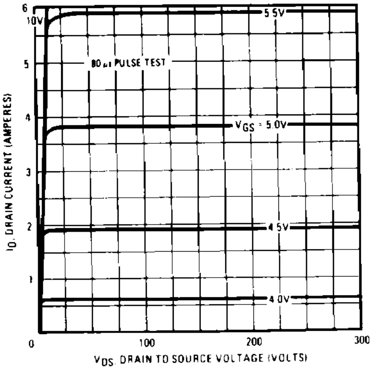


Fig. 1 – Typical Output Characteristics

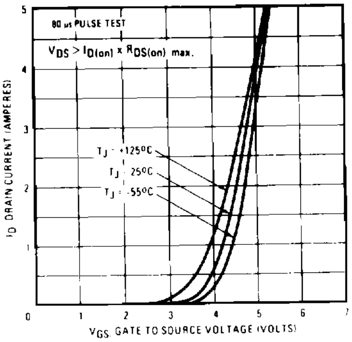


Fig. 2 – Typical Transfer Characteristics

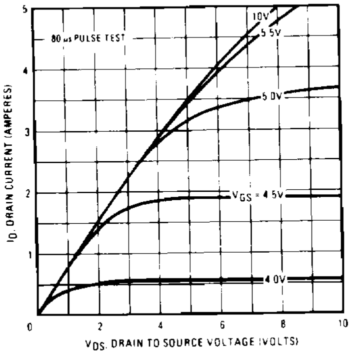


Fig. 3 – Typical Saturation Characteristics

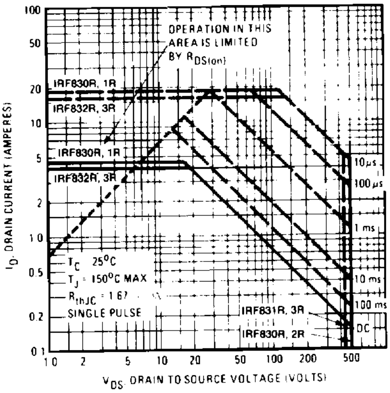


Fig. 4 – Maximum Safe Operating Area

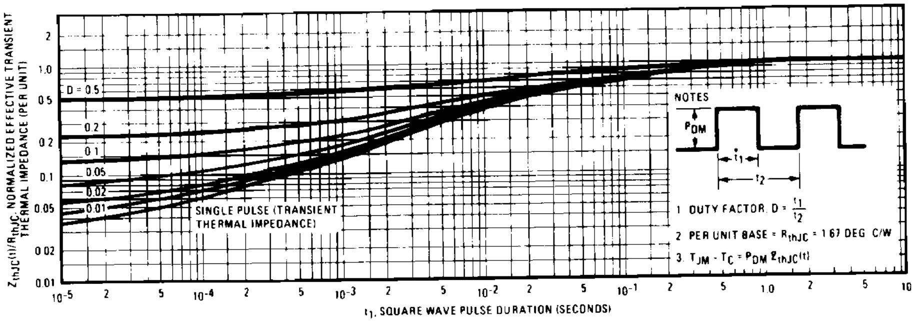


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

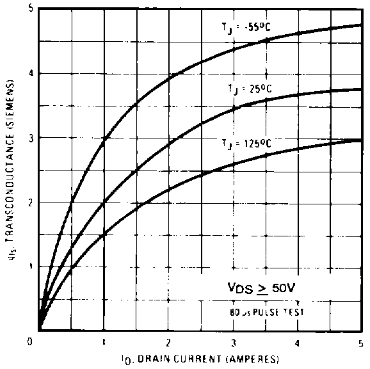


Fig. 6 – Typical Transconductance Vs. Drain Current

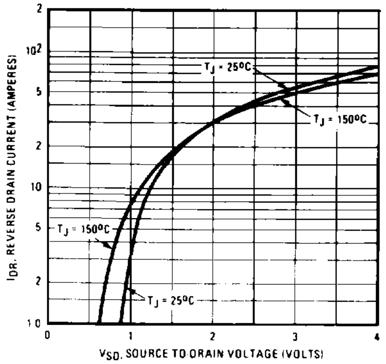


Fig. 7 – Typical Source-Drain Diode Forward Voltage

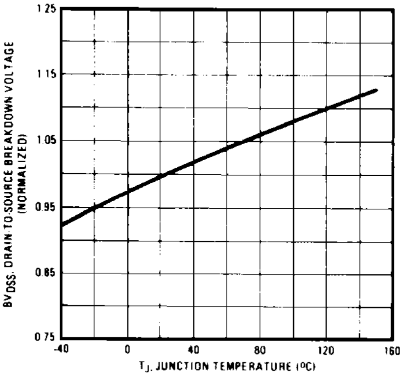


Fig. 8 – Breakdown Voltage Vs. Temperature

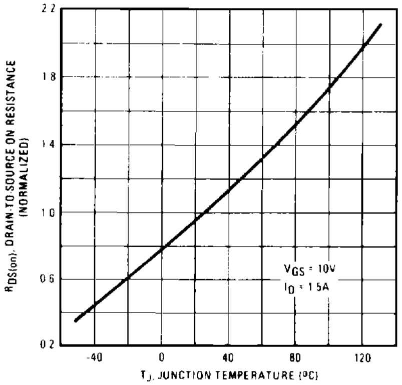


Fig. 9 – Normalized On-Resistance Vs. Temperature

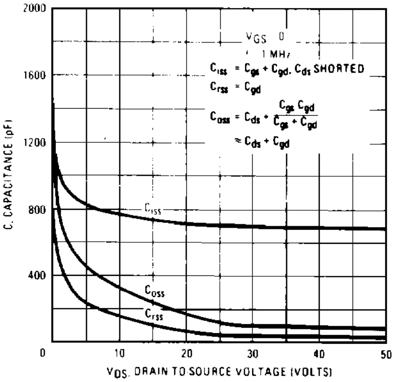


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

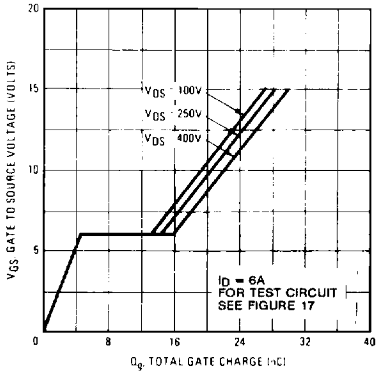


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

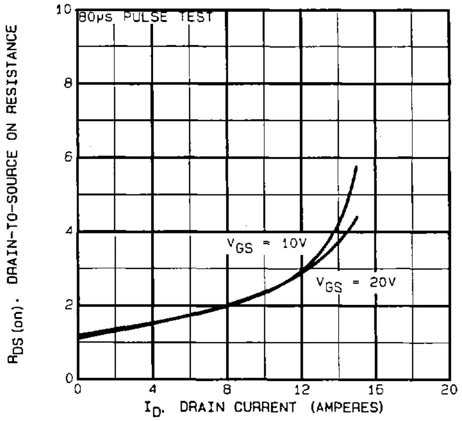


Fig. 12 — Typical On-Resistance Vs. Drain Current

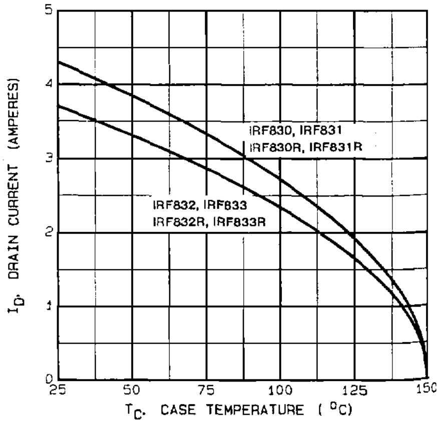


Fig. 13 — Maximum Drain Current Vs. Case Temperature

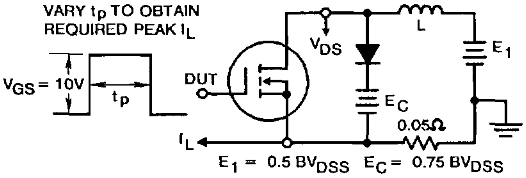


Fig. 14a — Clamped Inductive Test Circuit

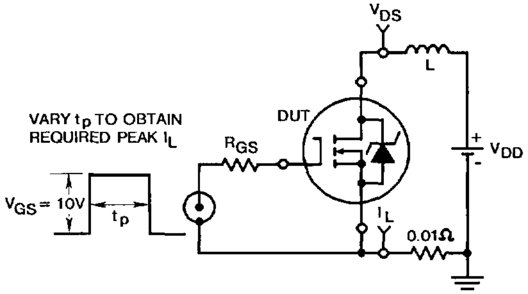


Fig. 15a — Unclamped Energy Test Circuit

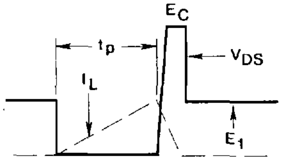


Fig. 14b — Clamped Inductive Waveforms

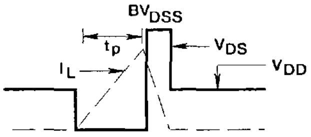


Fig. 15b — Unclamped Energy Waveforms

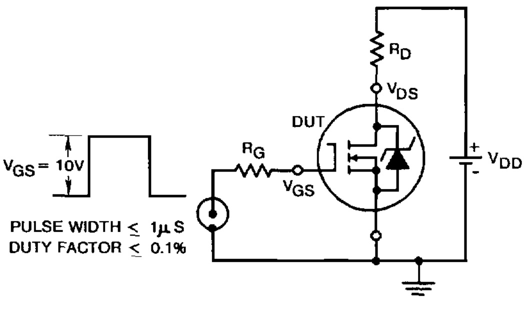


Fig. 16 — Switching Time Test Circuit

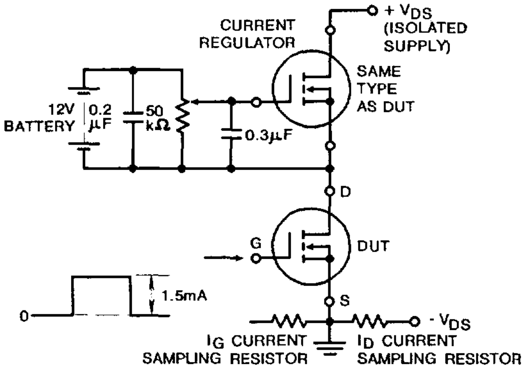


Fig. 17 — Gate Charge Test Circuit