

January 1998

Features

- 7A, 100V
- $r_{DS(ON)} = 0.300\Omega$
- 2kV ESD Protected
- *Temperature Compensating PSPICE Model*
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFD7N10LE	TO-251AA	7N10LE
RFD7N10LESM	TO-252AA	7N10LE
RFP7N10LE	TO-220AB	FP7N10LE

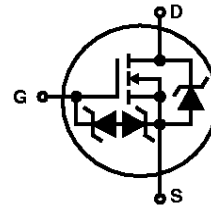
NOTE: When ordering, use the entire part number. Add suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD7N10LESM9A.

Description

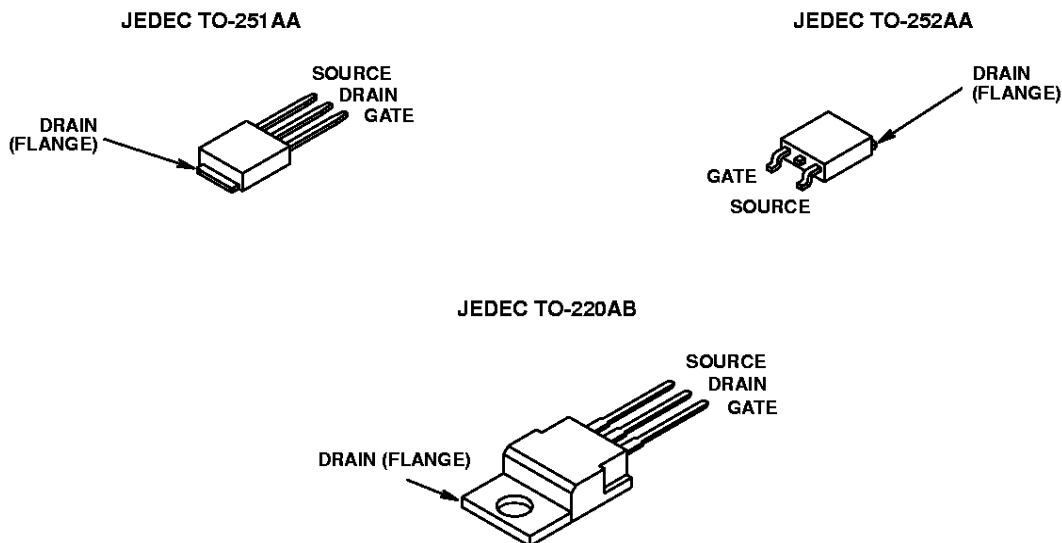
These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V to 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

Formerly developmental type TA49046.

Symbol



Packaging



RFD7N10LE, RFD7N10LESM, RFP7N10LE

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

	RFD7N10LE, RFD7N10LESM, RFP7N10LE	UNITS
Drain to Source Voltage	100	V
Drain to Gate Voltage	100	V
Gate to Source Voltage	+10, -8	V
Drain Current		
Continuous	7	A
Pulsed Drain Current	Refer to Peak Current Curve	
Pulsed Avalanche Rating	Refer to UIS Curve	
Power Dissipation	47	W
Derate Above 25°C	0.318	W/ $^\circ\text{C}$
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	2	kV
Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	100	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1	-	2	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$	$T_C = 25^\circ\text{C}$	-	-	1	μA
			$T_C = 150^\circ\text{C}$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = +10, -8\text{V}$	-	-	10	μA	
On Resistance	$r_{DS(ON)}$	$I_D = 7\text{A}$, $V_{GS} = 5\text{V}$	-	-	0.300	Ω	
Turn-On Time	t_{ON}	$V_{DD} = 50\text{V}$, $I_D = 7\text{A}$ $R_L = 7.1\Omega$, $V_{GS} = 5\text{V}$ $R_{GS} = 2.5\Omega$	-	-	110	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	10	-	ns	
Rise Time	t_r		-	65	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	23	-	ns	
Fall Time	t_f		-	18	-	ns	
Turn-Off Time	t_{OFF}		-	-	60	ns	
Total Gate Charge	$Q_{g(TOT)}$		$V_{GS} = 0$ to 10V	$V_{DD} = 80\text{V}$ $I_D = 7\text{A}$, $R_L = 11.4\Omega$	-	125	150
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0$ to 5V	-		67	80	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0$ to 1V	-		3.7	4.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	360	-	pF	
Output Capacitance	C_{OSS}		-	70	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	3.15	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251 and TO-252 Package	-	-	100	$^\circ\text{C/W}$	
		TO-220 Package	-	-	62	$^\circ\text{C/W}$	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 7\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 7\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	130	ns

RFD7N10LE, RFD7N10LESM, RFP7N10LE

Typical Performance Curves Unless Otherwise Specified

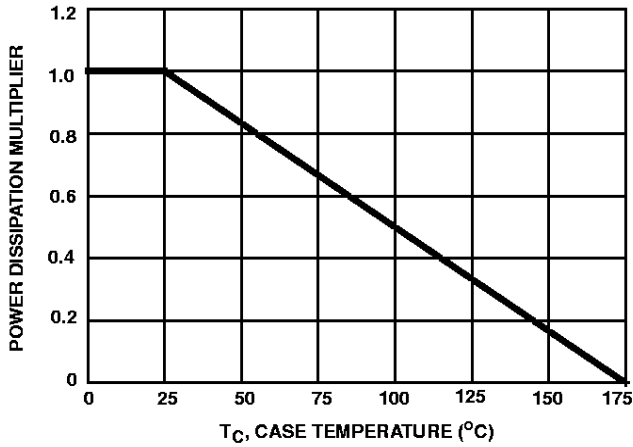


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

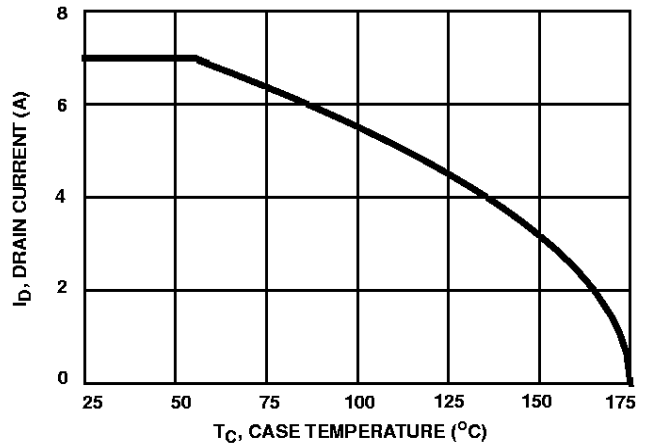


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

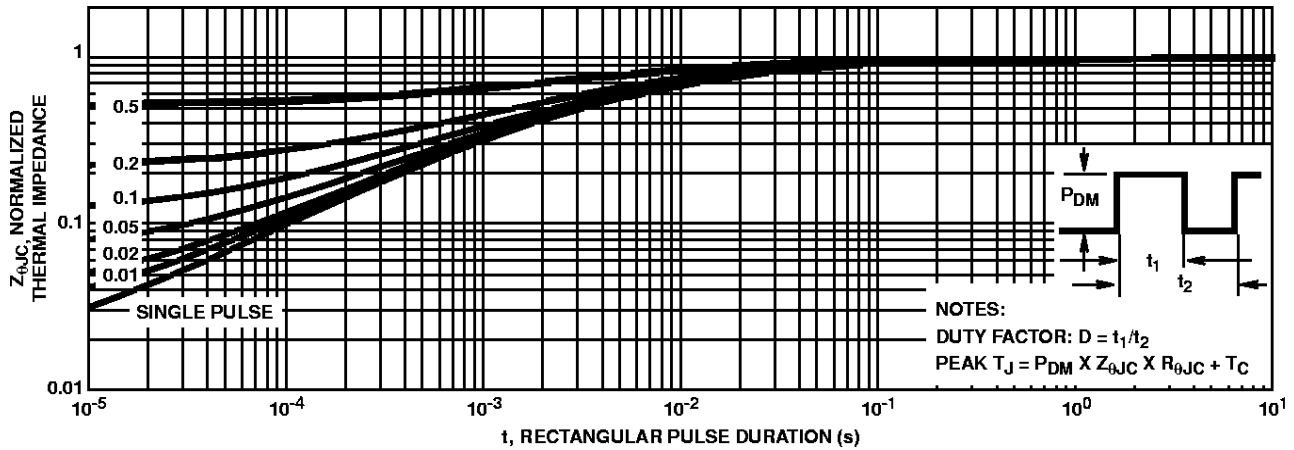


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

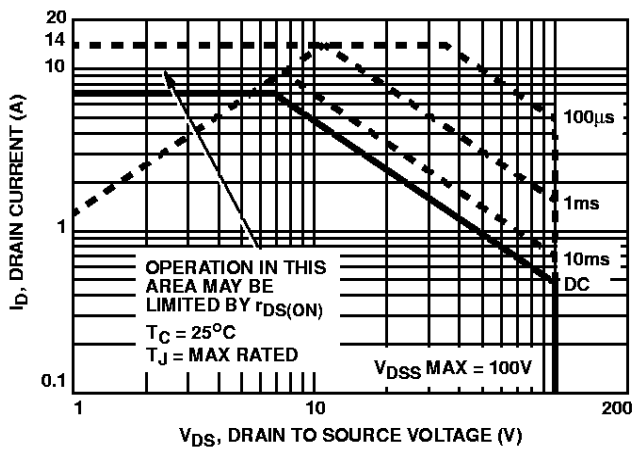


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

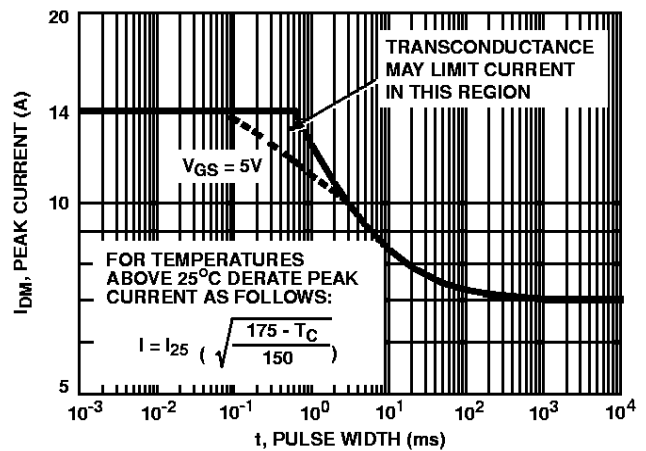


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)

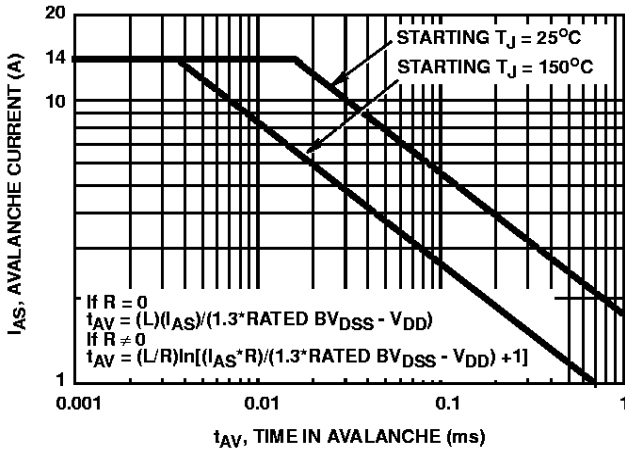


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

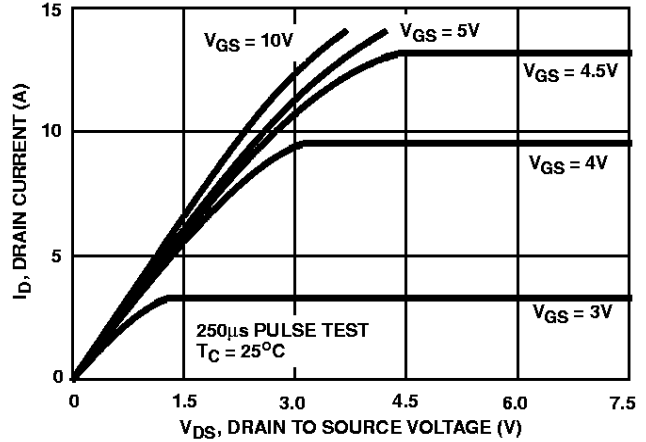


FIGURE 7. SATURATION CHARACTERISTICS

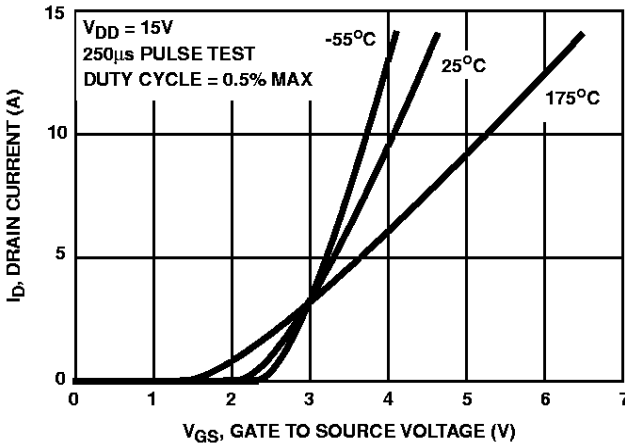


FIGURE 8. TRANSFER CHARACTERISTICS

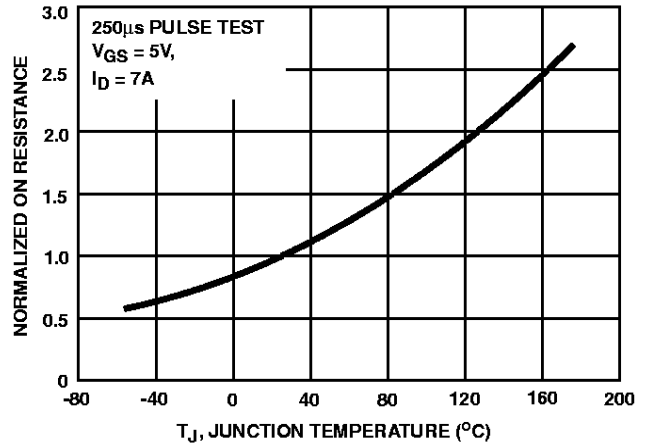


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

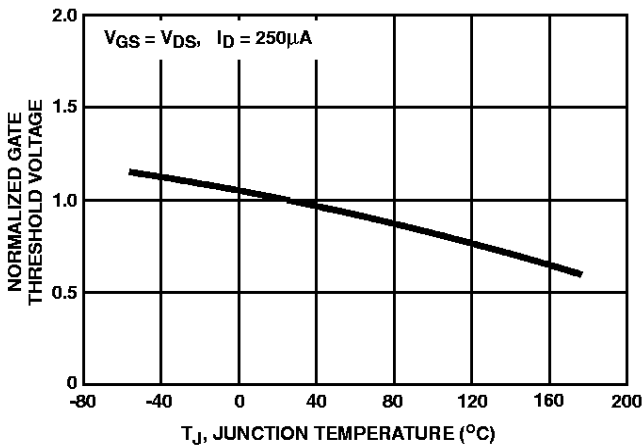


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

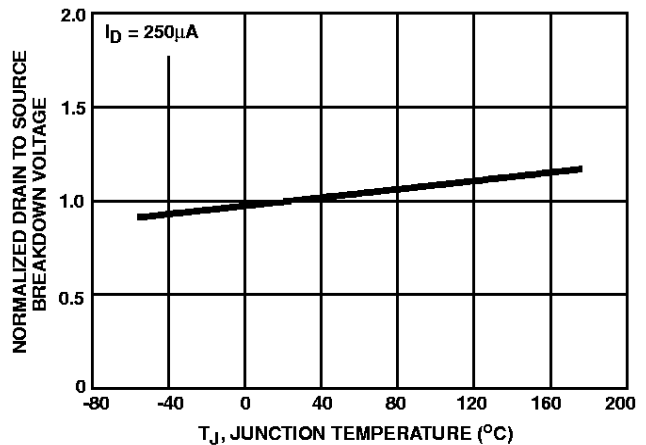


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

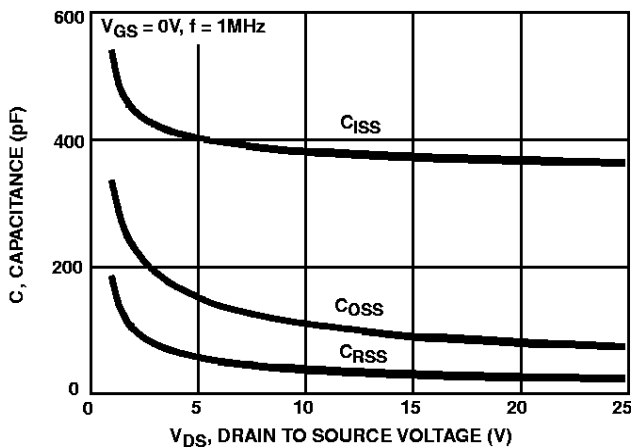
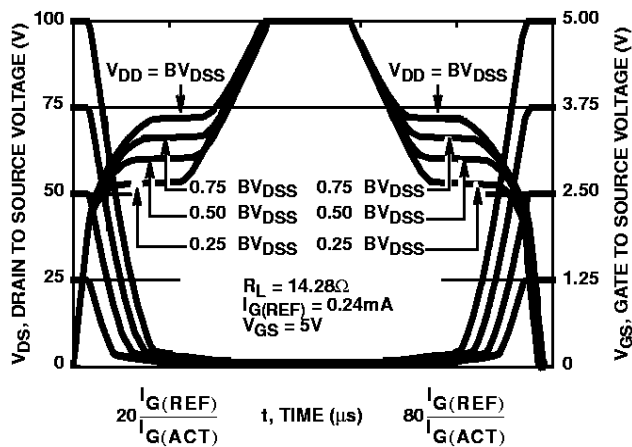


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.
FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

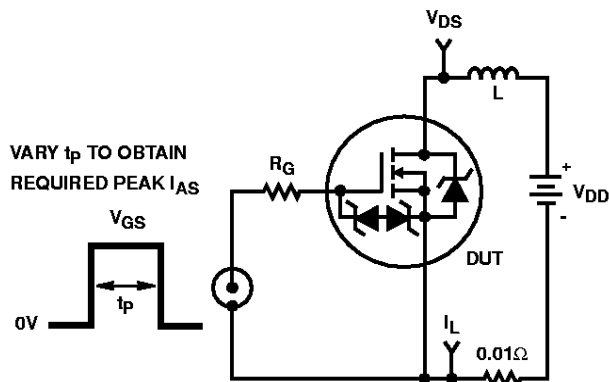


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

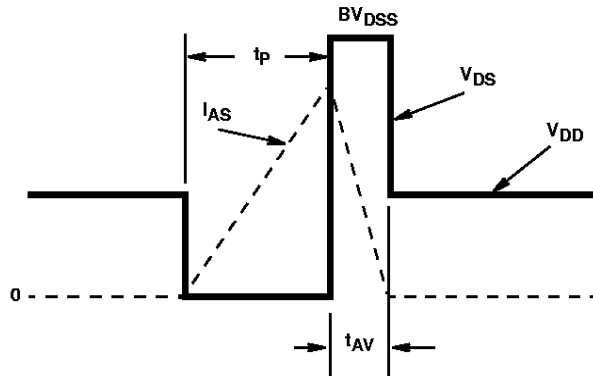


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

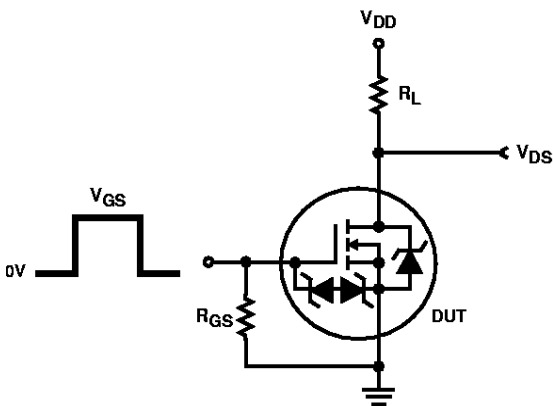


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

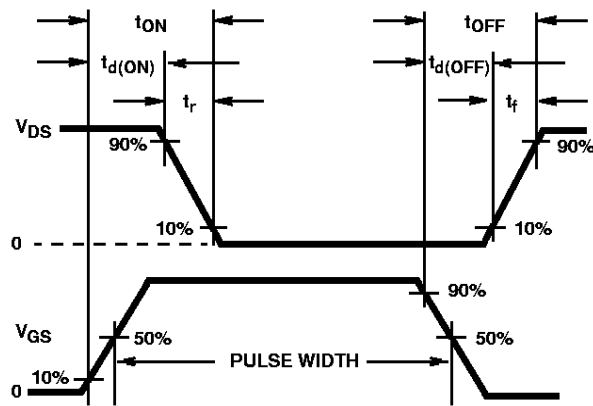


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

RFD7N10LE, RFD7N10LESM, RFP7N10LE

PSPICE Electrical Model

SUBCKT RFD7N10LE 2 1 3; rev 6/2/93

CA 12 8 1.102e-9
 CB 15 14 1.157e-9
 CIN 6 8 0.370e-9

DBODY 7 5 DBDMOD
 DBREAK 5 11 DBKMOD
 DESD1 91 9 DESD1MOD
 DESD2 91 7 DESD2MOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 115.8
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
 LGATE 1 9 3.58e-9
 LSOURCE 3 7 3.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
 MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
 RDRAIN 50 16 RDSMOD 136.9e-3
 RGATE 9 20 7.61
 RIN 6 8 1e9
 RSCL1 5 51 RSLVCMOD 1e-6
 RSCL2 5 50 1e3
 RSOURCE 8 7 RDSMOD 84.4e-3
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
 VTO 21 6 0.444

ESCL 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/(15.5),7.25))}}

.MODEL DBDMOD D (IS=5.07e-14 RS=1.37e-2 TRS1=1.72e-3 TRS2=-1.59e-6 CJO=2.57e-10 TT=3.84e-8)
 .MODEL DBKMOD D (RS=2.32e-1 TRS1=6.50e-4 TRS2=1.72e-6)
 .MODEL DESD1MOD D (BV=13.0 TBV1=2.2e-4 TBV2=0 RS=49 TRS1=0 TRS2=0)
 .MODEL DESD2MOD D (BV=11.7 TBV1=-5.5e-4 TBV2=-8.5e-7 RS=0 TRS1=0 TRS2=0)
 .MODEL DPLCAPMOD D (CJO=0.184e-9 IS=1e-30 N=10)
 .MODEL MOSMOD NMOS (VTO=2.045 KP=14.07 IS=1e-30 N=10 TOX=1 L=1u W=1u)
 .MODEL RBKMOD RES (TC1=1.13e-3 TC2=4.74e-8)
 .MODEL RDSMOD RES (TC1=7.45e-3 TC2=2.68e-5)
 .MODEL RSLVCMOD RES (TC1=1.75e-3 TC2=0)
 .MODEL RVTOMOD RES (TC1=-2.73e-3 TC2=-5.46e-6)
 .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.35 VOFF=-1.75)
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.75 VOFF=-4.35)
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.75 VOFF=3.50)
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.50 VOFF=-1.75)

ENDS

NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records 1991.

