HARRIS

RFP4N05
RFP4N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 50A, 50V and 60V
- $r_{DS}(on) = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

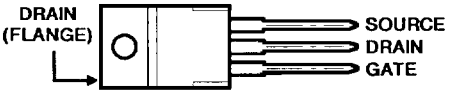
Description

The RFP4N05 and RFP4N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP-series types are supplied in the JEDEC TO-220AB plastic package.

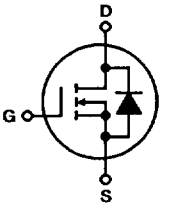
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP4N05	RFP4N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Continuous Drain Current	I_D	4	4	A
Pulsed Drain Current	I_{DM}	10	10	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	25	25	W
Linear Derating Factor		0.2	0.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2880**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP4N05 MIN	LIMITS RFP4N05 MAX	LIMITS RFP4N06 MIN	LIMITS RFP4N06 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 1mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.8	–	0.8	V
		I_D = 2A, V_{GS} = 10V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 10V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.8	–	0.8	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	85	–	85	pF
Reverse-Transfer Capacitance	C_{RSS}		–	30	–	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, $R_{GEN} = R_{GS}$ = 50Ω, V_{GS} = 10V	6 (typ)	15	6 (typ)	15	ns
Rise Time	t_r		14 (typ)	30	14 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		16 (typ)	30	16 (typ)	30	ns
Fall Time	t_f		14 (typ)	25	14 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP4N05 MIN	LIMITS RFP4N05 MAX	LIMITS RFP4N06 MIN	LIMITS RFP4N06 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration ≤ 300μs max., duty cycle ≤ 2%.

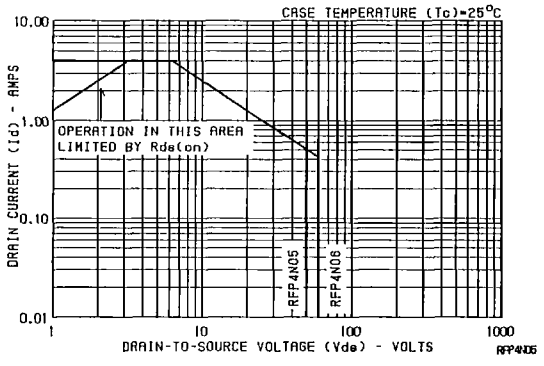


Fig. 1 — Maximum operating areas for all types.

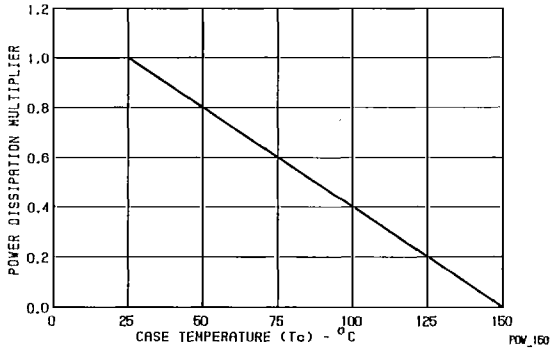


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

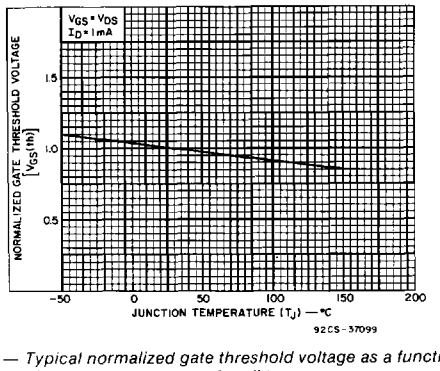


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

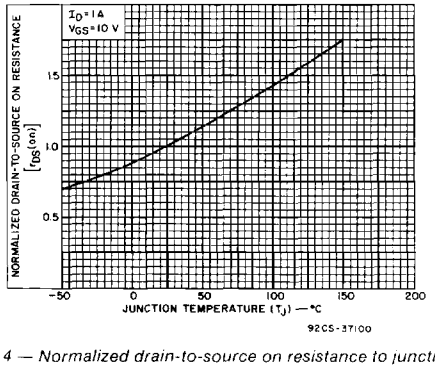


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

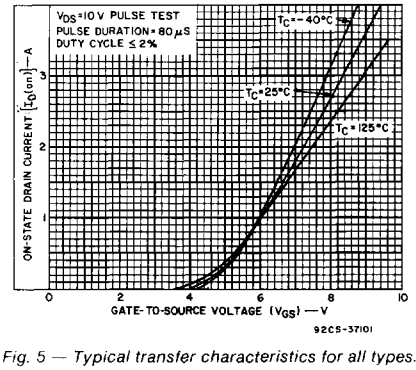


Fig. 5 — Typical transfer characteristics for all types.

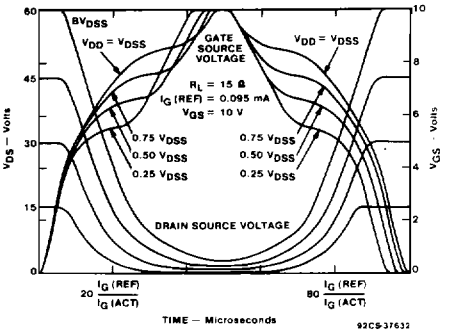


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

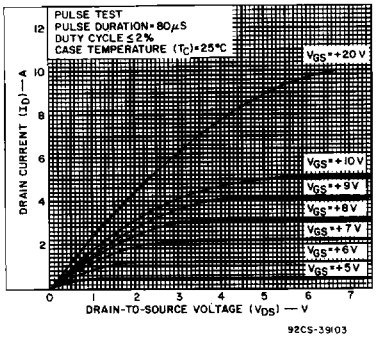


Fig. 7 — Typical saturation characteristics for all types.

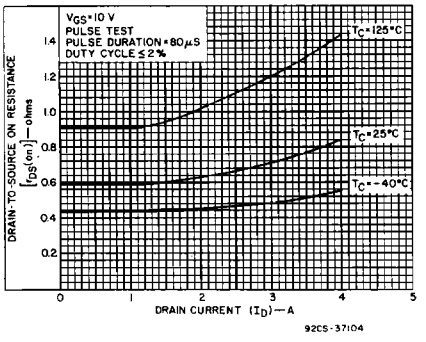


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

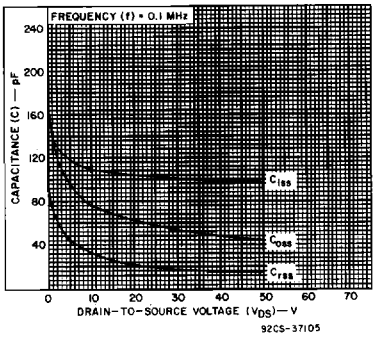


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types

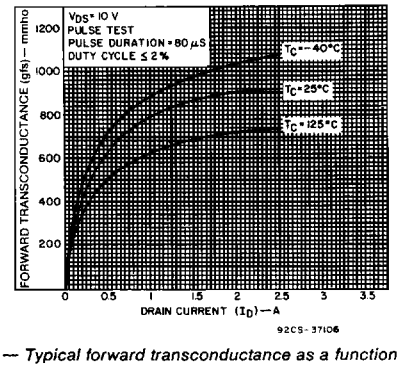


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

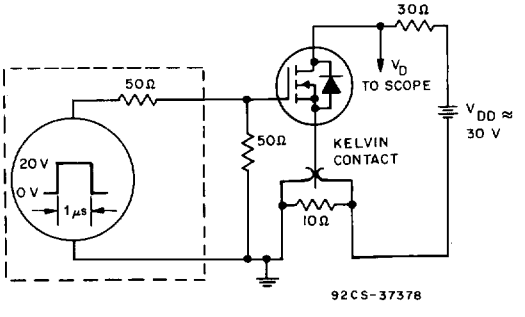


Fig. 11 — Switching Time Test Circuit