HARRIS

RFP25N05L

June 1992

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor (MegaFETs)

Features

- **25A, 50V**
- **$r_{DS(ON)} = 0.047\Omega$**
- **UIS SOA Rating Curve (Single Pulse)**
- **Design Optimized for 5V Gate Drives**
- **Can be Driven Directly from CMOS, NMOS, TTL Circuits**
- **Compatible with Automotive Drive Requirements**
- **SOA is Power-Dissipation Limited**
- **Nanoscecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Majority Carrier Device**
- **Operating Temperature .... +150°C**

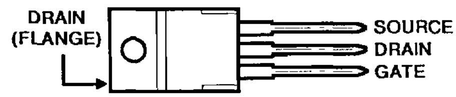
Description

The RFP25N05L is an N-Channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFP25N05L was designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP25N05L is supplied in the JEDEC TO-220AB plastic package.

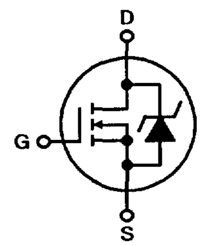
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	25	A
Pulsed Drain Current	I_{DM}	65	A
Single Pulse Avalanche Energy Rating		Refer to UIS SOA Curve*	
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60	W
Above T_C = +25°C, Derate Linearly		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

* See Figures 13, 14 and 15

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2270.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V	50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS} = V_{DS}$, I_D = 0.25 mA	1	2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150° C	—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 25 A, V_{GS} = 5 V I_D = 25 A, V_{GS} = 4 V	—	0.047 0.056	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 12.5 A $I_{g1} = I_{g2}$ = 1 A V_{GS} (clamp) + 5 V, − 0.6 V R_L = 2 Ω	—	60	ns
Turn-On Delay Time	$t_d(on)$		—	15 (typ.)	
Rise Time	t_r		—	35 (typ.)	
Turn-Off Delay Time	$t_d(off)$		—	40 (typ.)	
Fall Time	t_f		—	14 (typ.)	
Turn-Off Time	t(off)		—	100	
Total Gate Charge	$Q_g(total)$	V_{GS} = 0-10 V; V_{DD} = 40 V	—	80	nC
Gate Charge at 5 V	$Q_g(5)$	V_{GS} = 0-5 V; I_D = 25 A	—	45	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 0-1 V; R_L = 1.6 Ω	—	3	
Plateau Voltage	V(plateau)	I_D = 25 A, V_{DS} = 15 V	—	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 12.5 A, R_L = 2 Ω L = 0.2 μH, $I_{g1} = I_{g2}$ = 1 A V_{GS} (clamp) + 5 V, −0.6 V	—	30	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		—	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD} = 25 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 25 A, dI_F/d_t = 100 A/μs	—	125	ns

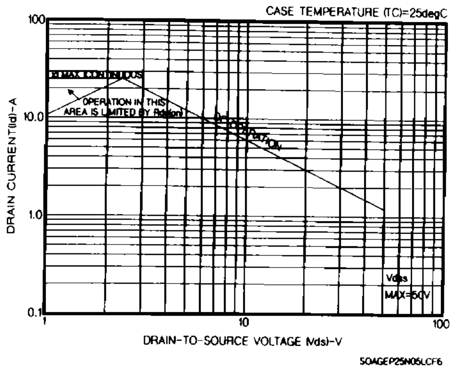


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

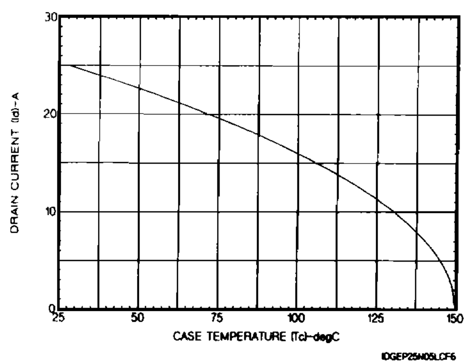


Fig. 2 - Maximum continuous drain current vs. temperature.

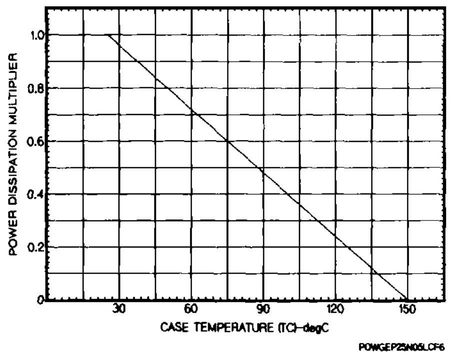


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

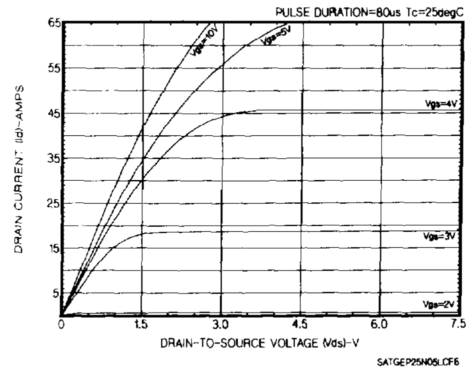


Fig. 4 - Typical saturation characteristics.

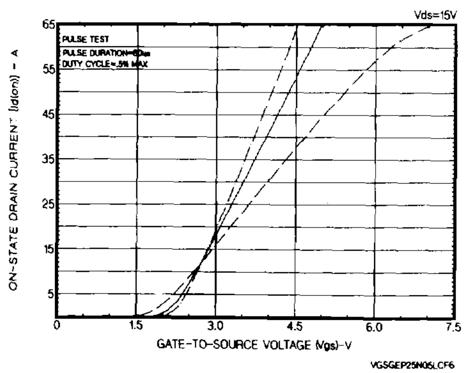


Fig. 5 - Typical transfer characteristics.

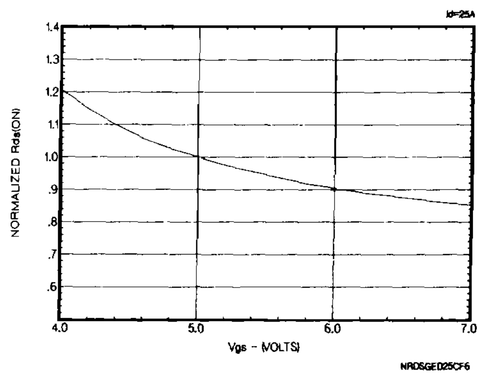


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

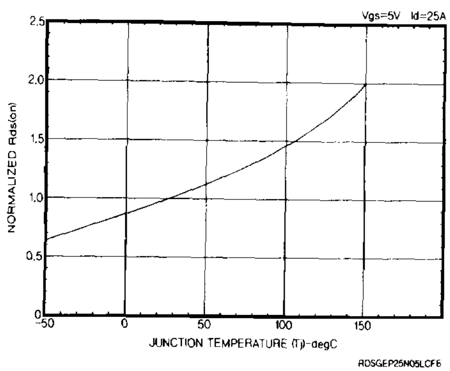


Fig. 7 - Normalized $r_{ds}(on)$ vs. junction temperature.

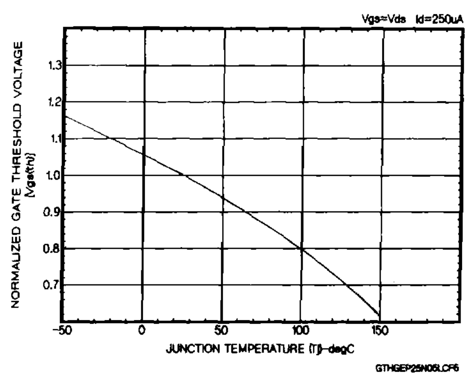


Fig. 8 - Typical normalized gate threshold voltage.

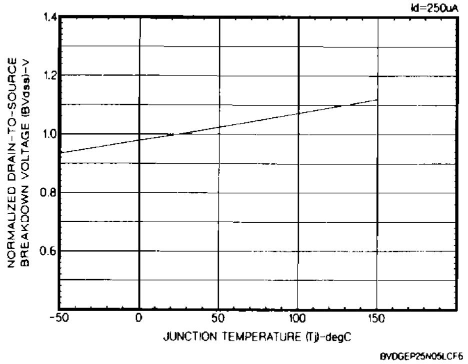


Fig. 9 - Drain source breakdown voltage vs. temperature.

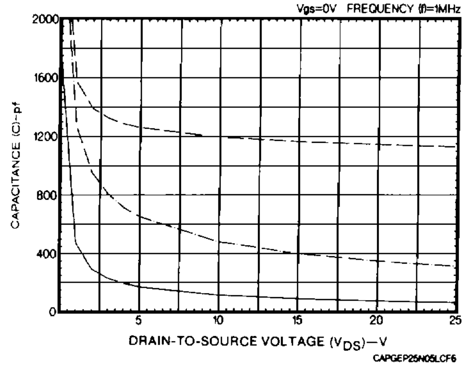


Fig. 10 - Typical capacitance vs. voltage

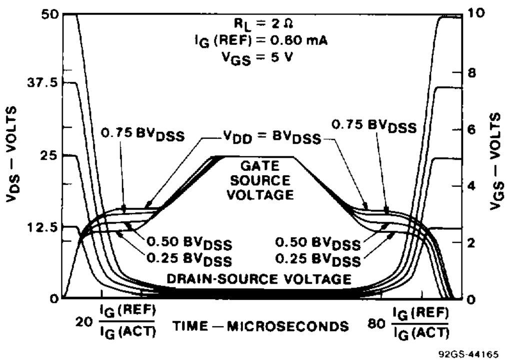


Fig. 11 - Normalized switching waveforms for constant gate-current (Refer to Harris application notes AN-7254 and AN-7260)

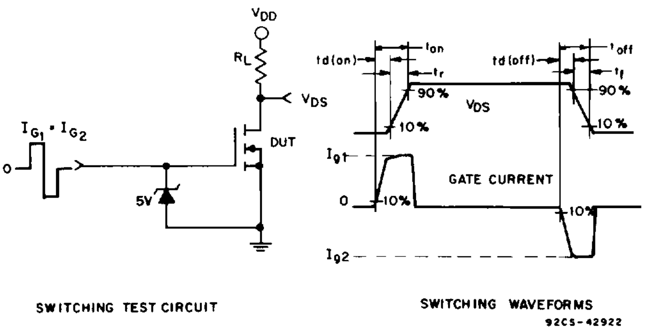


Fig. 12 - Resistive switching.

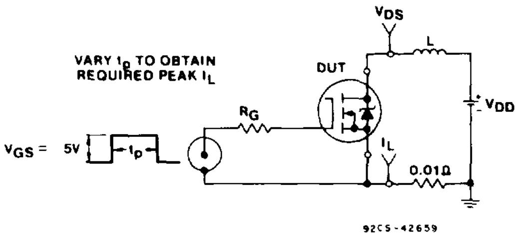


Fig. 13 - Unclamped energy test circuit.

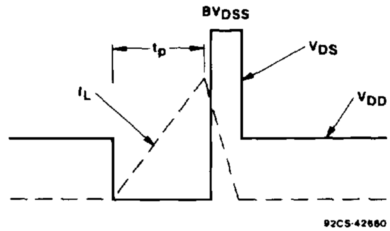


Fig. 14 - Unclamped energy waveforms.

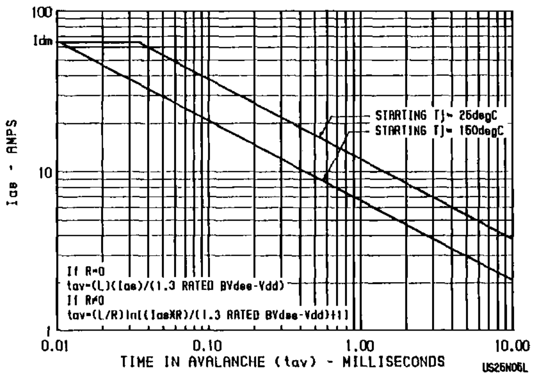


Fig. 15 - Unclamped-Inductive-Switching SOA
(Single Pulse UIS SOA)