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Vishay Siliconix

Automotive P-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	-30
$R_{DS(on)}$ (Ω) at $V_{GS} = -10 \text{ V}$	0.0085
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.0200
I _D (A)	-30 ^a
Configuration	Single
Package	PowerPAK SO-8L

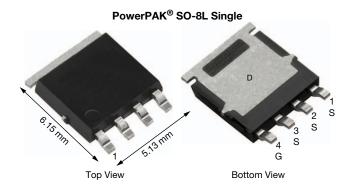
FEATURES

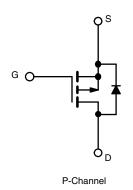
- TrenchFET® power MOSFET
- AEC-Q101 qualified ^d
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE





ABSOLUTE MAXIMUM RATING	S (T _C = 25 °C, unles	s otherwise noted	l)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	-30	V	
Gate-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current a	T _C = 25 °C	1	-30		
Continuous Drain Current	T _C = 125 °C	I _D	-30		
Continuous Source Current (Diode Conduction) ^a		I _S	-30	Α	
Pulsed Drain Current ^b		I _{DM}	-84		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	-32		
Single Pulse Avalanche Energy	L = 0.1 IIII	E _{AS}	51	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	В	68	W	
Maximum Fower Dissipation -	T _C = 125 °C	- P _D	22	VV	
Operating Junction and Storage Temperature Range Soldering Recommendations (Peak Temperature) e, f		T _J , T _{stg}	-55 to +175	°C	
			260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount c	R_{thJA}	68	°C/W
Junction-to-Case (Drain)		R_{thJC}	2.2	G/VV

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.
- e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static					•	I.		
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	: 0 V, I _D = -250 μA	-30	-	-	V	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = -250 μA	-1.5	-2.0	-2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$		-	-	± 100	nA	
Gate-Source Leakage		V _{DS} =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 300		
		$V_{GS} = 0 V$	V _{DS} = -30 V	-	-	-1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = -30V, T _J = 125 °C	-	-	-50	μΑ	
		V _{GS} = 0 V	V _{DS} = -30V, T _J = 175 °C	-	-	-250		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = -10 V	$V_{DS} \le -5 \text{ V}$	-30	-	-	Α	
		V _{GS} = -10 V	I _D = -10 A	-	0.0070	0.0085		
Drain Source On State Besistance 8	В	V _{GS} = -10 V	I _D = -10 A, T _J = 125 °C	-	-	0.0130	0	
Drain-Source On-State Resistance a	R _{DS(on)}	V _{GS} = -10 V	I _D = -10 A, T _J = 175 °C	-	-	0.0150	Ω	
		V _{GS} = -4.5 V	I _D = -7 A	-	0.0120	0.0200		
Forward Transconductance b	9 _{fs}	V _{DS} =	= -10 V, I _D = 10 A	-	32	=.	S	
Dynamic ^b								
Input Capacitance	C _{iss}			-	3400	4500		
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = -15 \text{ V}, f = 1 \text{ MHz}$	-	750	1000	pF	
Reverse Transfer Capacitance	C _{rss}			-	580	770		
Total Gate Charge ^c	Qg			-	73	109		
Gate-Source Charge ^c	Q _{gs}	$V_{GS} = -10 \text{ V}$	$V_{DS} = -15 \text{ V}, I_{D} = -10 \text{ A}$	-	11	=.	nC	
Gate-Drain Charge ^c	Q _{gd}			-	21	=.		
Gate Resistance	Rg		f = 1 MHz	1	2	3	Ω	
Turn-On Delay Time ^c	t _{d(on)}			-	20	25		
Rise Time ^c	t _r	V _{DD} =	$-15 \text{ V}, \text{ R}_{\text{L}} = 1.5 \Omega$	-	146	189		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong -10 \text{ A},$	$V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$	-	57	75	ns	
Fall Time ^c	t _f			-	20	25		
Source-Drain Diode Ratings and Chara	cteristics ^b				•			
Pulsed Current ^a	I _{SM}			-	-	-84	Α	
Forward Voltage	V _{SD}	lr =	-3 A, V _{GS} = 0 V	_	-0.75	-1.2	V	

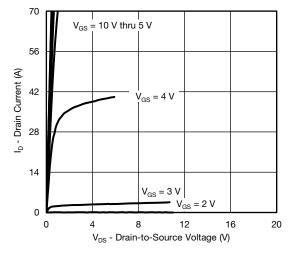
Notes

- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

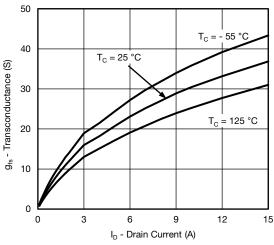
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



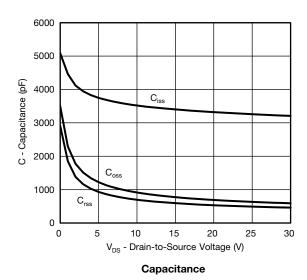
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

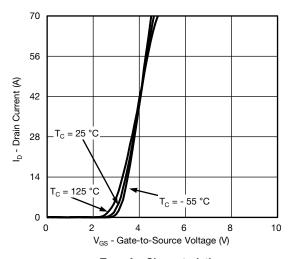


Output Characteristics

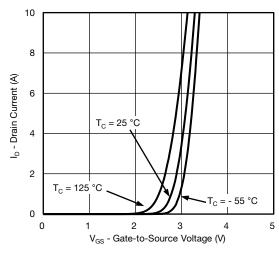


Transconductance

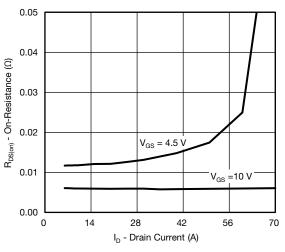




Transfer Characteristics



Transfer Characteristics

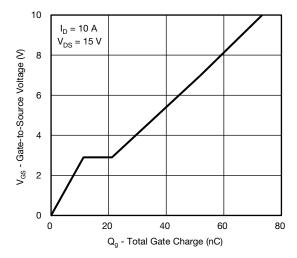


On-Resistance vs. Drain Current

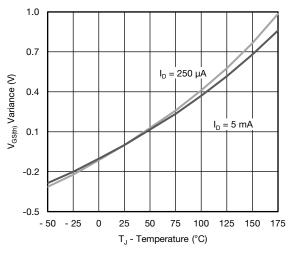
For technical questions, contact: automostechsu



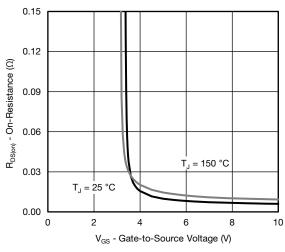
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



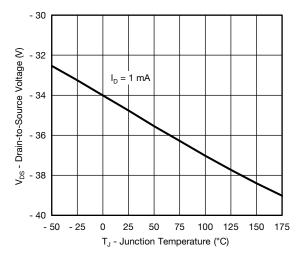
Gate Charge



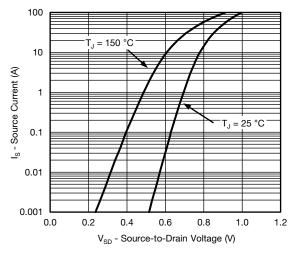
Threshold Voltage



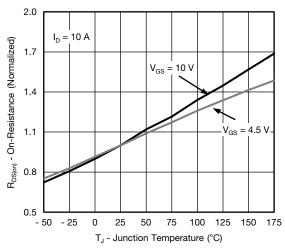
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



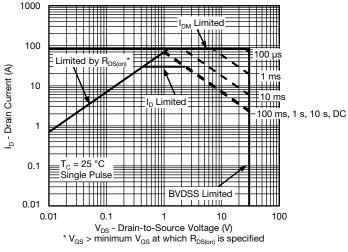
Source Drain Diode Forward Voltage



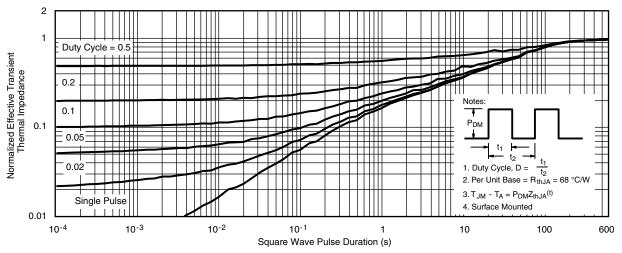
On-Resistance vs. Junction Temperature



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Safe Operating Area

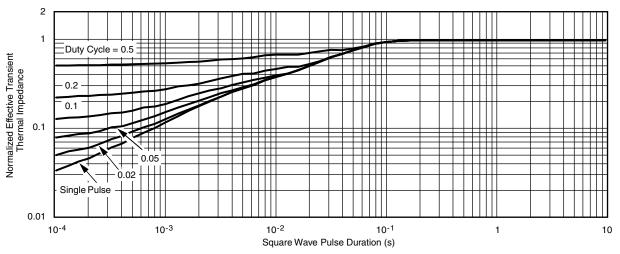


Normalized Thermal Transient Impedance, Junction-to-Ambient

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

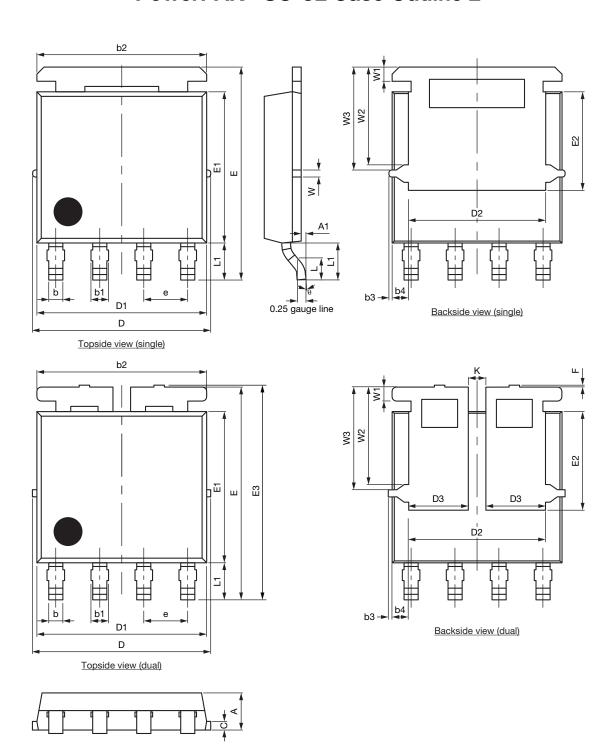
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg267109.



PowerPAK® SO-8L Case Outline 2





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DIM		MILLIMETERS		INCHES			
DIM.	MIN.	NOM.	MAX.	MIN. NOM.		MAX	
Α	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094		0.004			
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC		0.050 BSC			
Е	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	2.75	2.85	2.95	0.108	0.112	0.116	
E3	6.05	6.22	6.40	0.238	0.245	0.252	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51			0.020		
W	0.23			0.009			
W1		0.41			0.016		
W2	2.82		0.111				
W3		2.96			0.117		
θ	0°	-	10°	0°	-	10°	

DWG: 6044

Note

• Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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