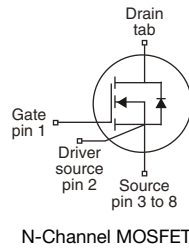


## E Series Power MOSFET



### FEATURES

- 4<sup>th</sup> generation E series technology
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low effective capacitance ( $C_{o(er)}$ )
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Solar (PV inverters)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.043
$Q_g$ max. (nC)	98	
$Q_{gs}$ (nC)	28	
$Q_{gd}$ (nC)	14	
Configuration	Single	

### ORDERING INFORMATION

Package	PowerPAK 10 x 12
Lead (Pb)-free and halogen-free	SIHK045N60E-T1-GE3


### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	600	V	
Gate-source voltage	$V_{GS}$	$\pm 30$		
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	48	A
		$T_C = 100$ °C	31	
Pulsed drain current <sup>a</sup>	$I_{DM}$	138		
Linear derating factor		2.22	W/°C	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	286	mJ	
Maximum power dissipation	$P_D$	278	W	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Drain-source voltage slope	$dv/dt$	100	V/ns	
Reverse diode $dv/dt$ <sup>d</sup>				17

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 4.5$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $di/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C

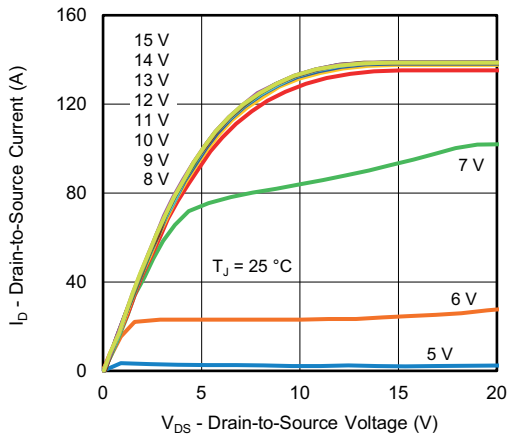
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	50 °C	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.45	

SPECIFICATIONS ( $T_J = 25\text{ °C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}$		-	0.64	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$		-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}$	-	0.043	0.049	$\Omega$
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 35\text{ A}$		-	22	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$		-	4013	-	pF
Output capacitance	$C_{oss}$			-	148	-	
Reverse transfer capacitance	$C_{rss}$			-	6	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$		-	117	-	pF
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$			-	744	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}, V_{DS} = 480\text{ V}$	-	65	98	nC
Gate-source charge	$Q_{gs}$			-	28	-	
Gate-drain charge	$Q_{gd}$			-	14	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480\text{ V}, I_D = 17\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	35	70	ns
Rise time	$t_r$			-	40	80	
Turn-off delay time	$t_{d(off)}$			-	67	101	
Fall time	$t_f$			-	14	28	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$		0.4	0.8	1.6	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	48	A
Pulsed diode forward current	$I_{SM}$			-	-	148	
Diode forward voltage	$V_{SD}$	$T_J = 25\text{ °C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse recovery time	$t_{rr}$	$T_J = 25\text{ °C}, I_F = I_S = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	403	806	ns
Reverse recovery charge	$Q_{rr}$			-	6.5	13	$\mu\text{C}$
Reverse recovery current	$I_{RRM}$			-	26	-	A

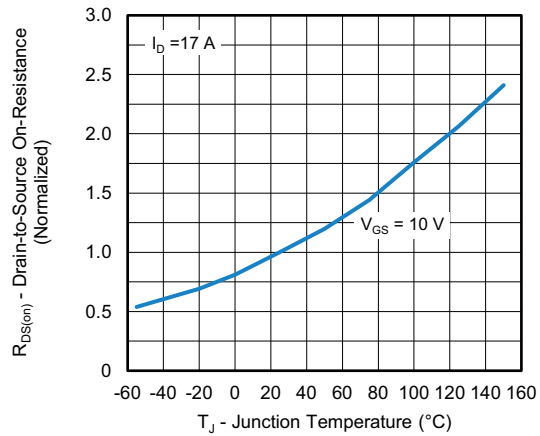
**Notes**

- $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$
- $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$
- When mounted on 1" x 1" FR4 board

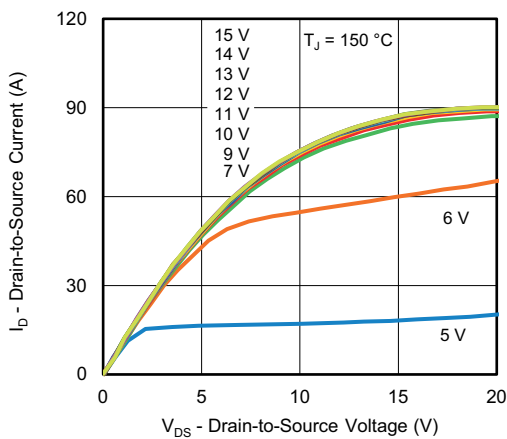
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



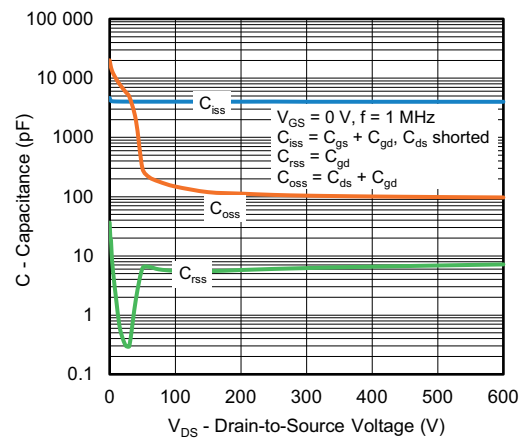
**Fig. 1 - Typical Output Characteristics**



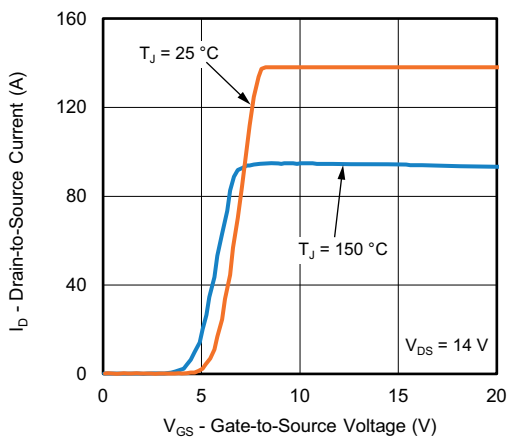
**Fig. 4 - Normalized On-Resistance vs. Temperature**



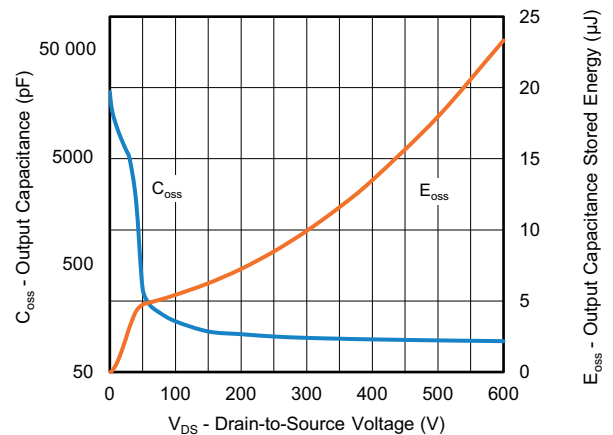
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - C<sub>oss</sub> and E<sub>oss</sub> vs. V<sub>DS</sub>**

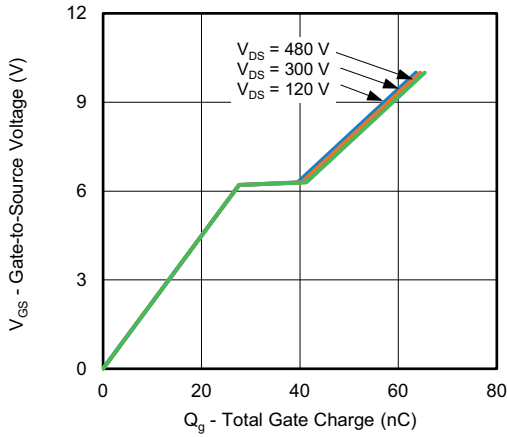


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

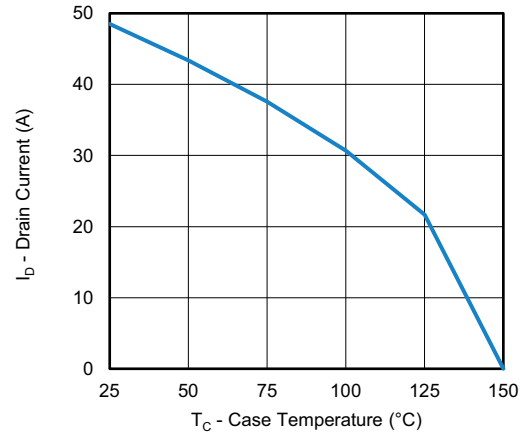


Fig. 10 - Maximum Drain Current vs. Case Temperature

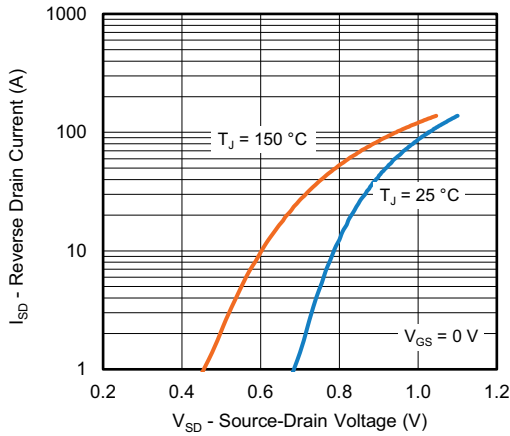


Fig. 8 - Typical Source-Drain Diode Forward Voltage

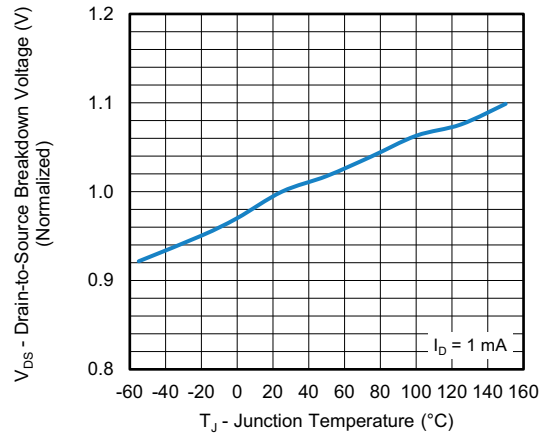


Fig. 11 - Temperature vs. Drain-to-Source Voltage

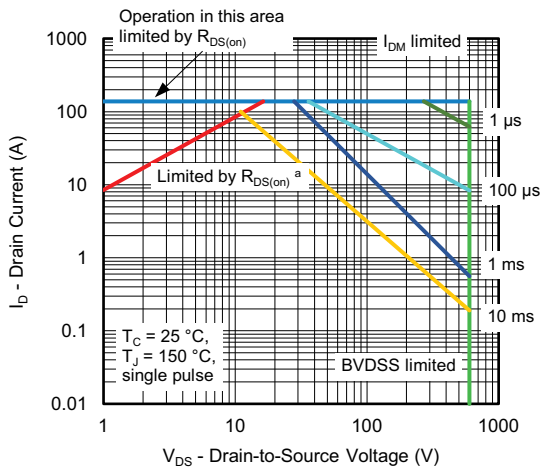


Fig. 9 - Maximum Safe Operating Area

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

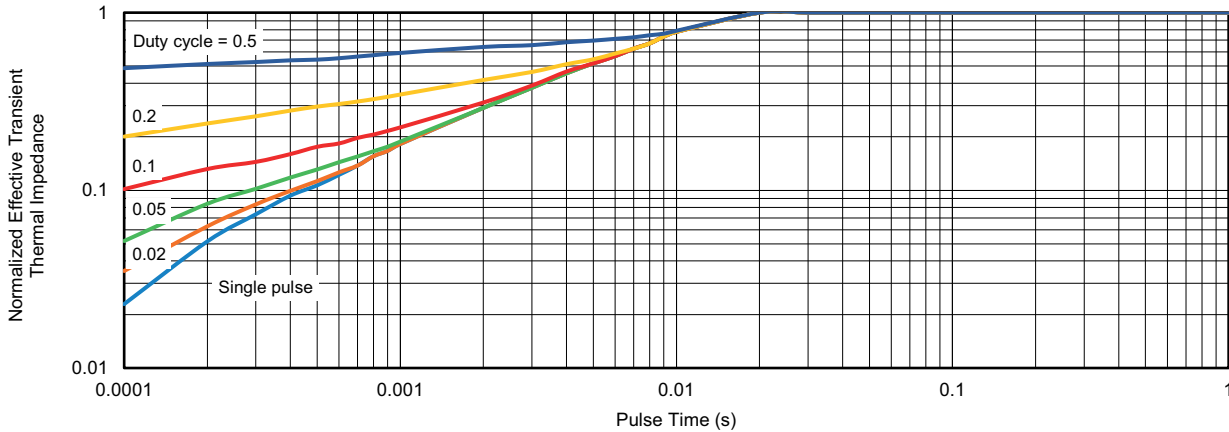


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

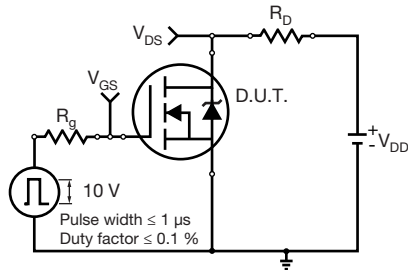


Fig. 13 - Switching Time Test Circuit

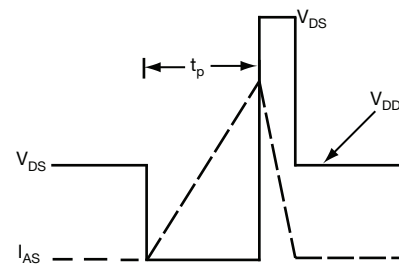


Fig. 16 - Unclamped Inductive Waveforms

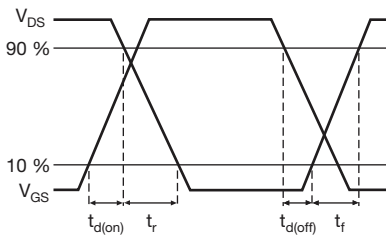


Fig. 14 - Switching Time Waveforms

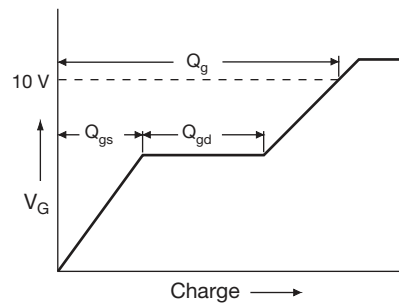


Fig. 17 - Basic Gate Charge Waveform

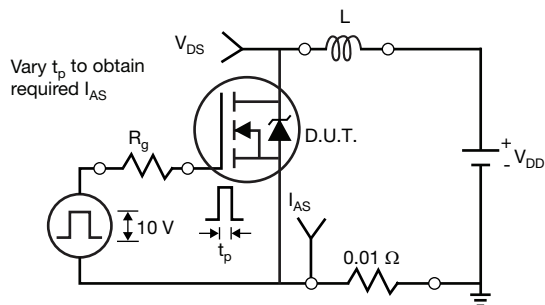


Fig. 15 - Unclamped Inductive Test Circuit

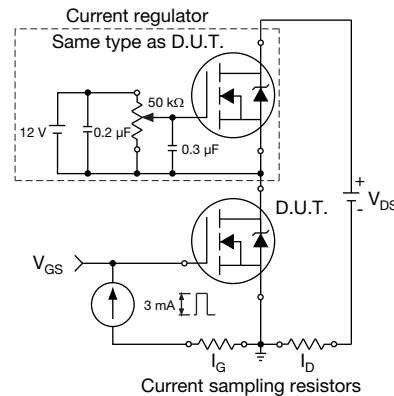


Fig. 18 - Gate Charge Test Circuit



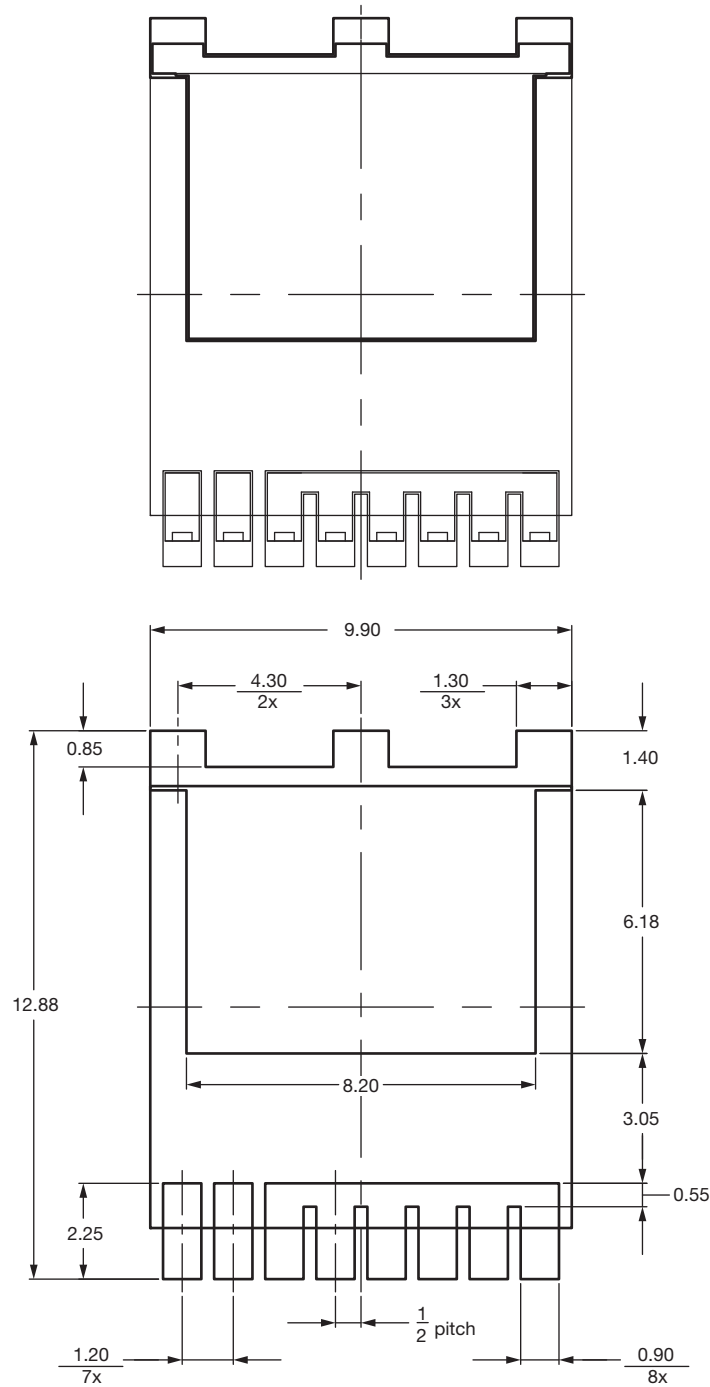
**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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# Recommended Land Pattern PowerPAK® 10 x 12 (TOLL) (High Voltage)



**Note**

- Dimensions in mm

ECN: S22-1061-Rev. C, 26-Dec-2022  
DWG: 3013



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