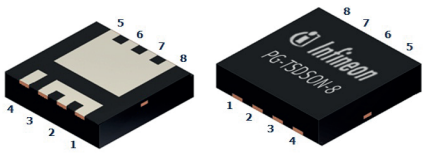
MOSFET

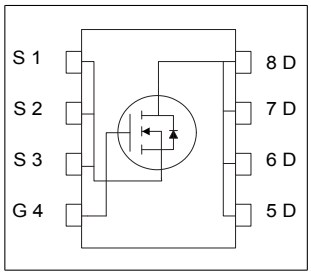
OptiMOS™5 Power-Transistor, 25 V

TSDSON-8 FL
(enlarged source interconnection)



Features

- Optimized for high performance buck converters
- Monolithic integrated Schottky-like diode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5V
- 100% avalanche tested
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	25	V
$R_{DS(on),max}$	1.1	mΩ
I_D	202	A
Q_{oss}	29	nC
Q_G(0V..4.5V)	17	nC

Type / Ordering Code	Package	Marking	Related Links
BSZ011NE2LS5I	PG-TSDSON-8 FL	11NE25I	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - - -	- - - - -	202 128 173 109 35	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{THJA}=60 °C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	808	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	119	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-16	-	16	V	-
Power dissipation	P_{tot}	- -	- -	69 2.1	W	T_C=25 °C T_A=25 °C, R_{THJA}=60 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.8	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Device on PCB, 6 cm² cooling area	R_{thJA}	-	-	60	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	V_{GS}=0 V, I_D=10 mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/°C	I_D=10 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	- 0.9	0.5 -	mA	V_{DS}=20 V, V_{GS}=0 V, T_j=25 °C V_{DS}=20 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.82 1.1	1.1 1.5	mΩ	V_{GS}=10 V, I_D=20 A V_{GS}=4.5 V, I_D=20 A
Gate resistance	R_G	-	0.7	1.2	Ω	-
Transconductance	g_{fs}	80	160	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	2500	3400	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	1200	1600	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	92	-	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	4	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	26	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	3	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω

[1)] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5.6	-	nC	V_{DD}=12 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	3.5	-	nC	V_{DD}=12 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	3.5	-	nC	V_{DD}=12 V, I_D=20 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	5.7	-	nC	V_{DD}=12 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total[2)]	Q_g	-	17	23	nC	V_{DD}=12 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.3	-	V	V_{DD}=12 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total[2)]	Q_g	-	37	50	nC	V_{DD}=12 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	16	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge[2)]	Q_{oss}	-	29	38	nC	V_{DD}=12 V, V_{GS}=0 V

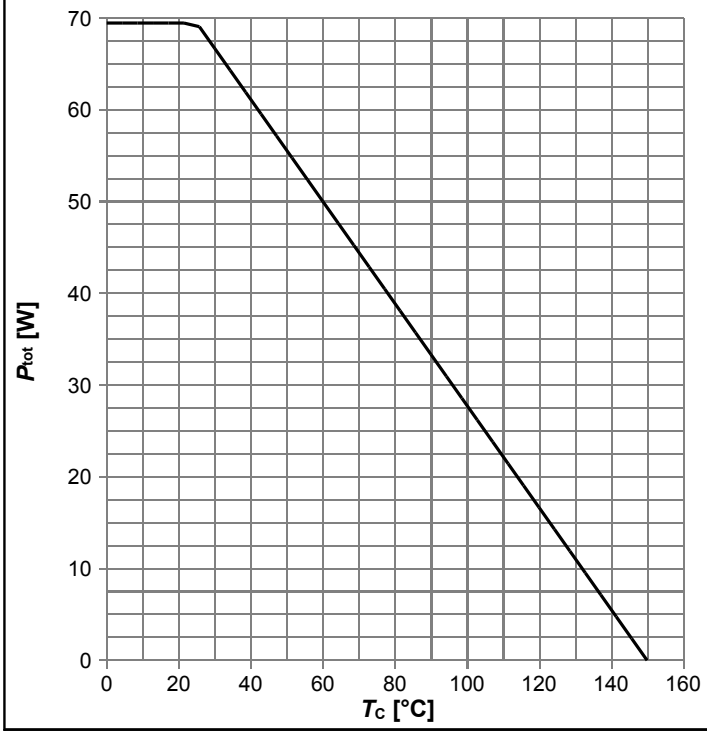
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	107	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	808	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.50	0.65	V	V_{GS}=0 V, I_F=11 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	19	-	ns	V_R=20 V, I_F=20 A, di_F/dt=400 A/µs
Reverse recovery charge	Q_{rr}	-	20	-	nC	V_R=20 V, I_F=20 A, di_F/dt=400 A/µs

[1)] See ″Gate charge waveforms″ for parameter definition
[2)] Defined by design. Not subject to production test.

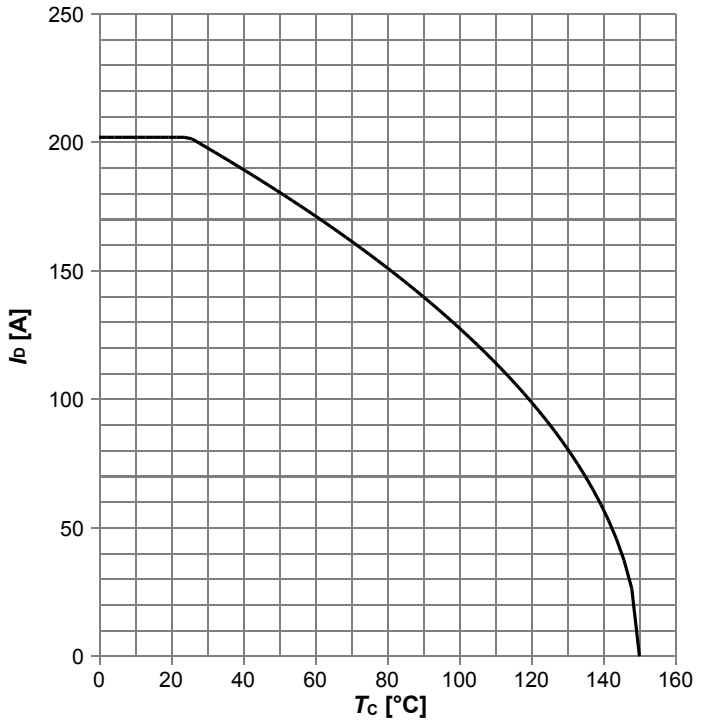
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



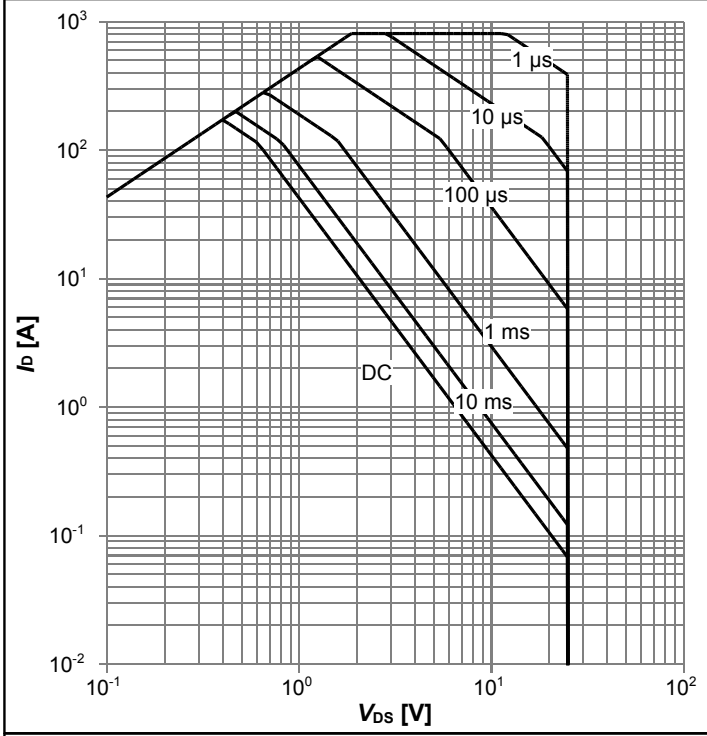
$P_{tot}=f(T_C)$

Diagram 2: Drain current



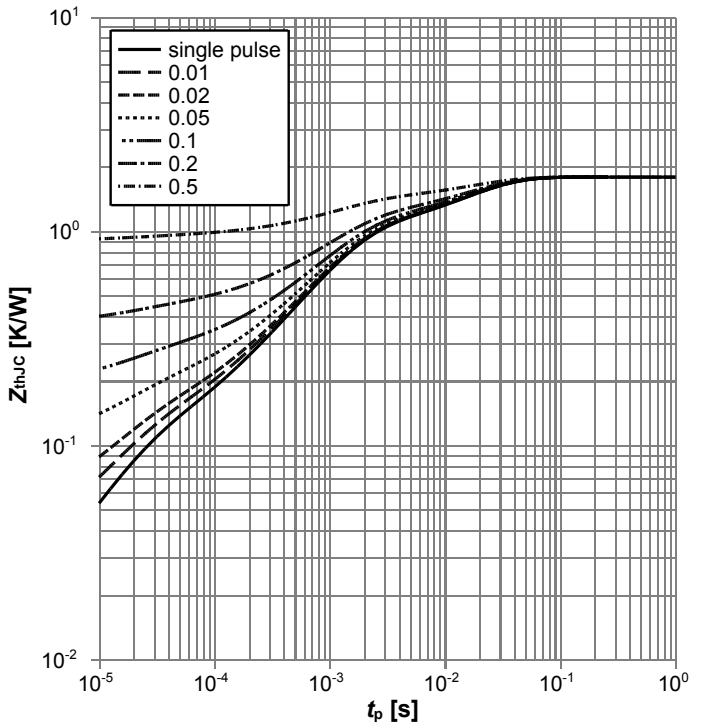
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



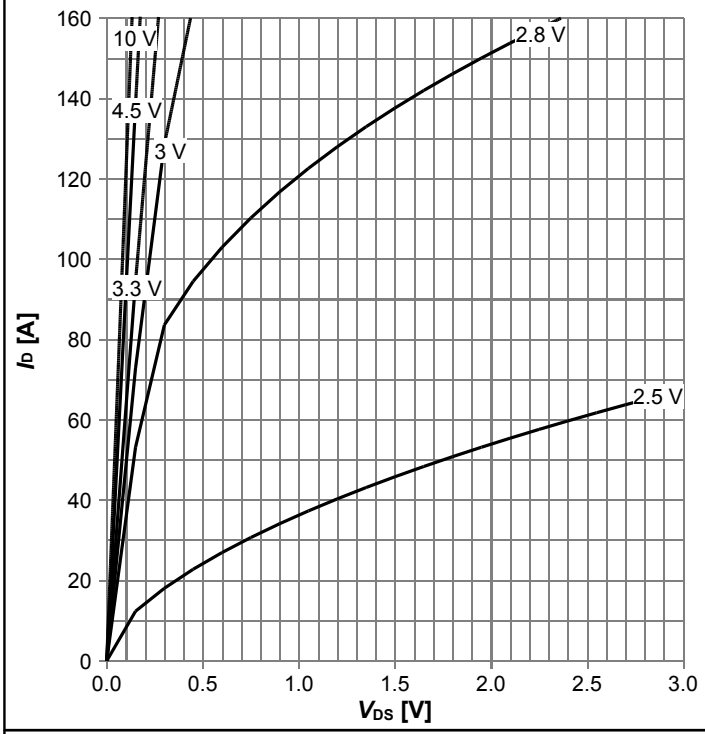
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



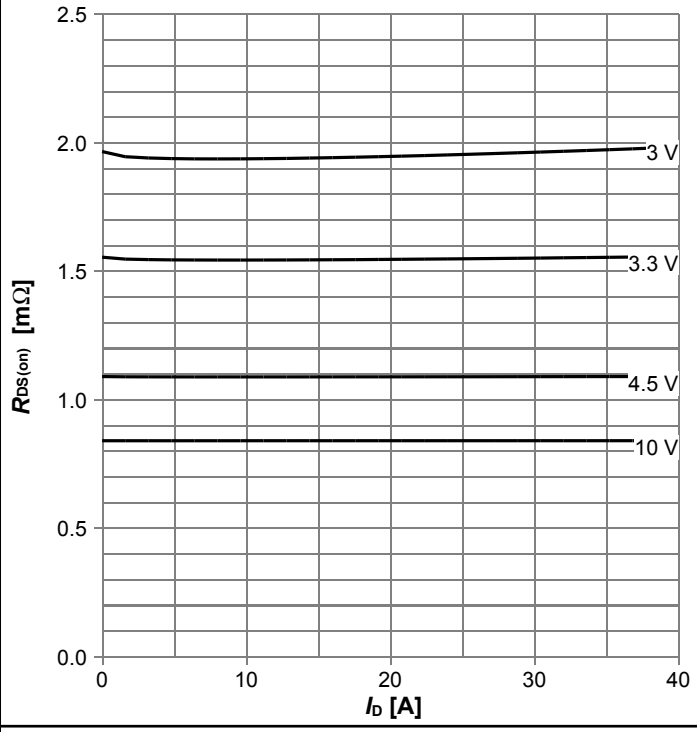
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



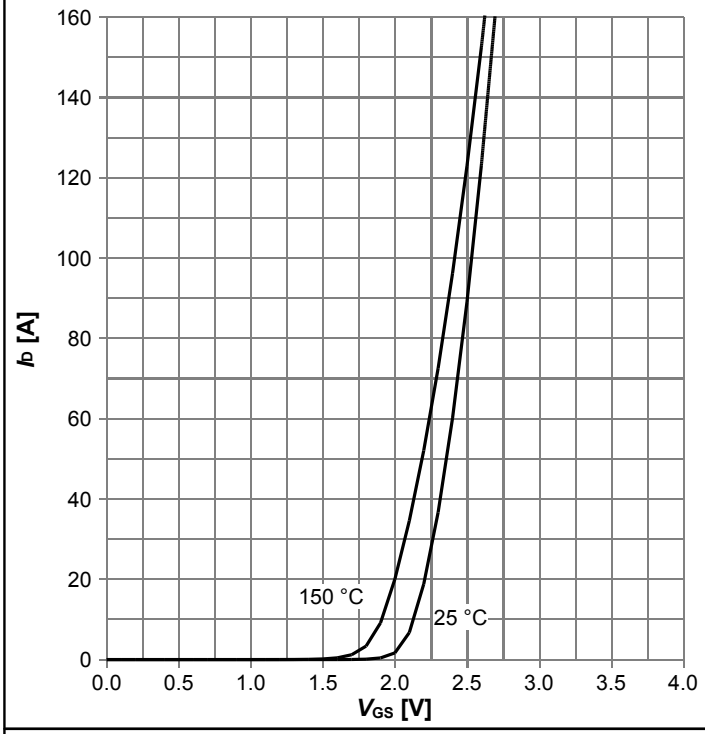
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



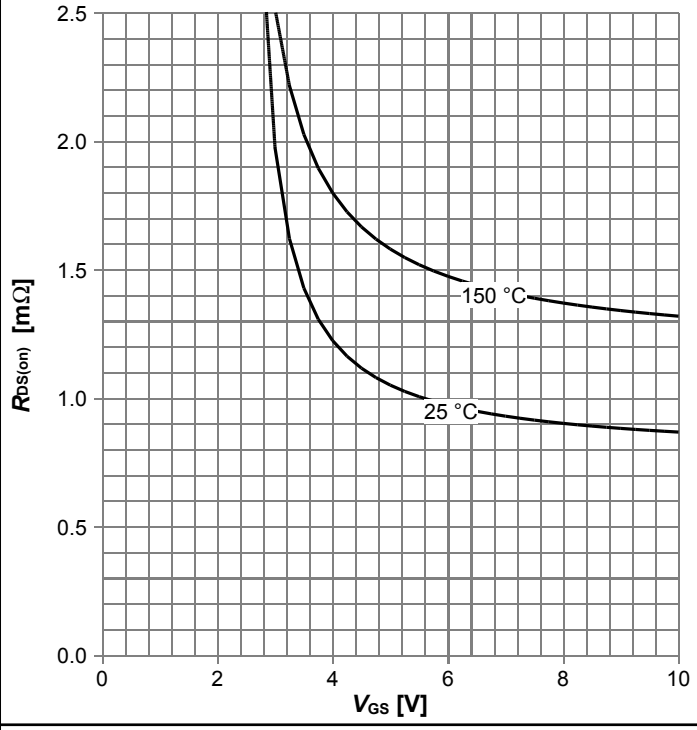
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



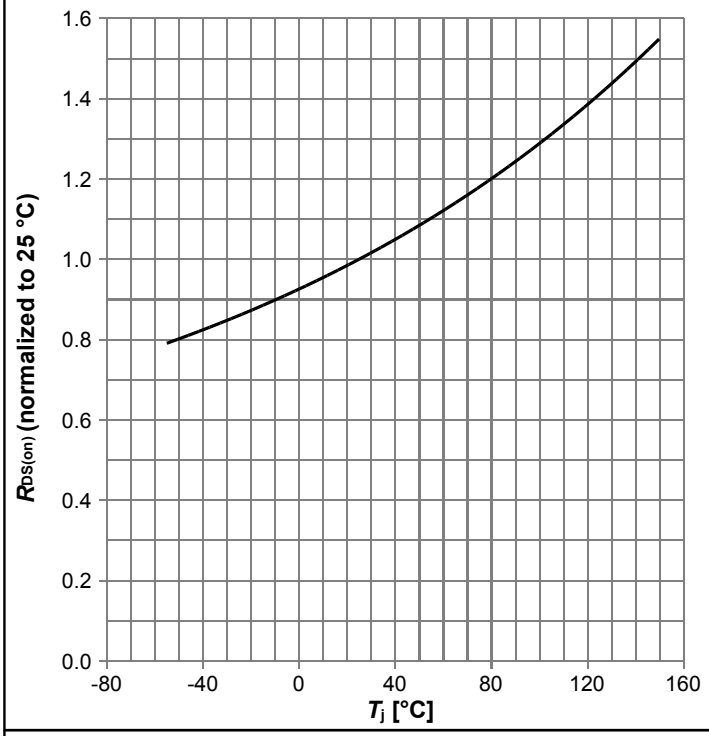
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



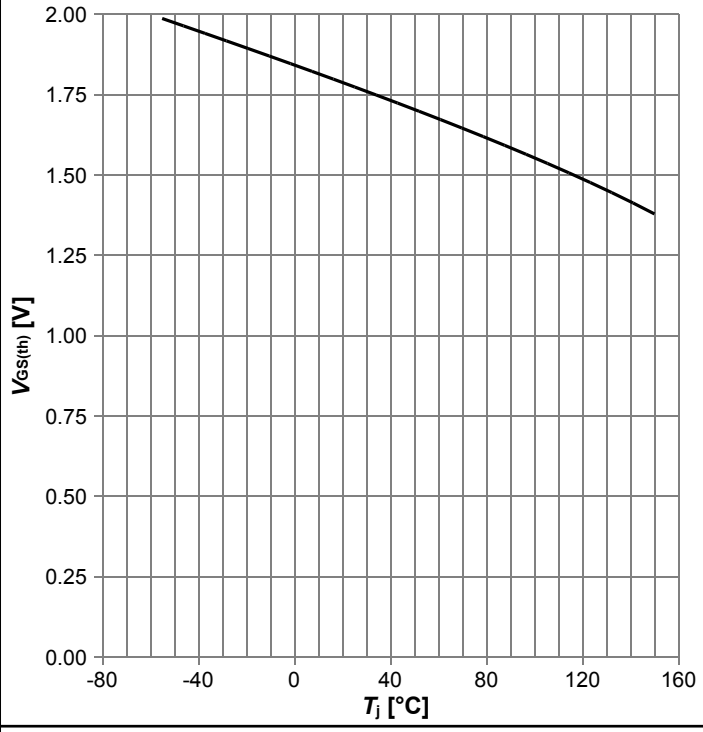
$R_{DS(on)}=f(V_{GS})$, $I_D=20$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



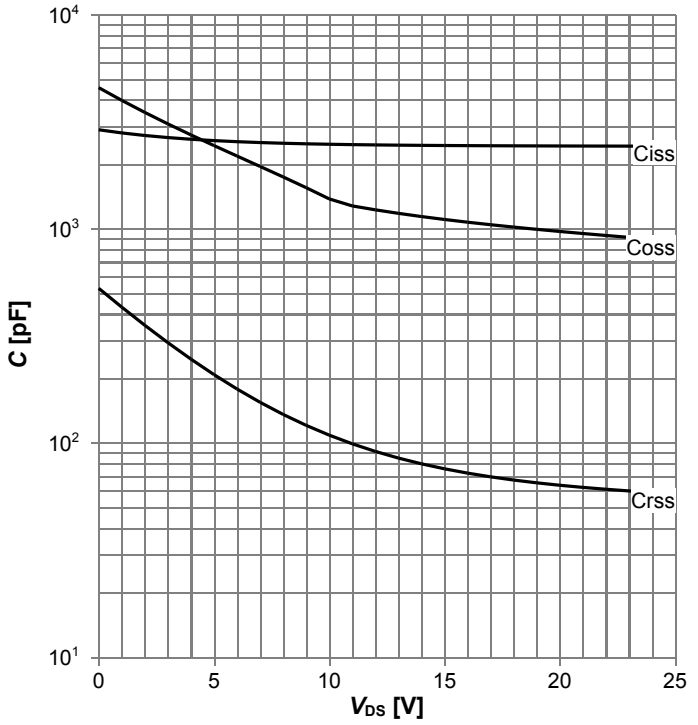
$R_{DS(on)}$=f(T_j), I_D=20 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



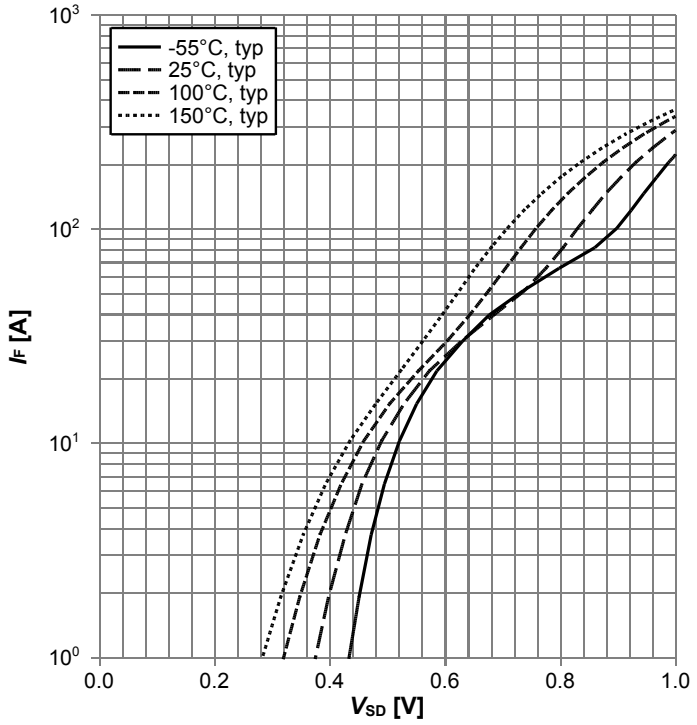
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}, I_D=10 mA

Diagram 11: Typ. capacitances



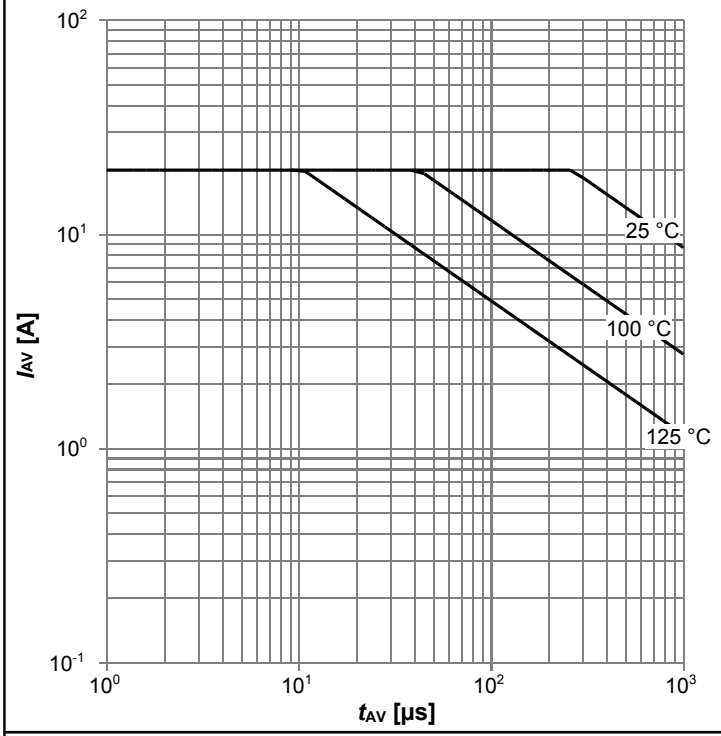
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



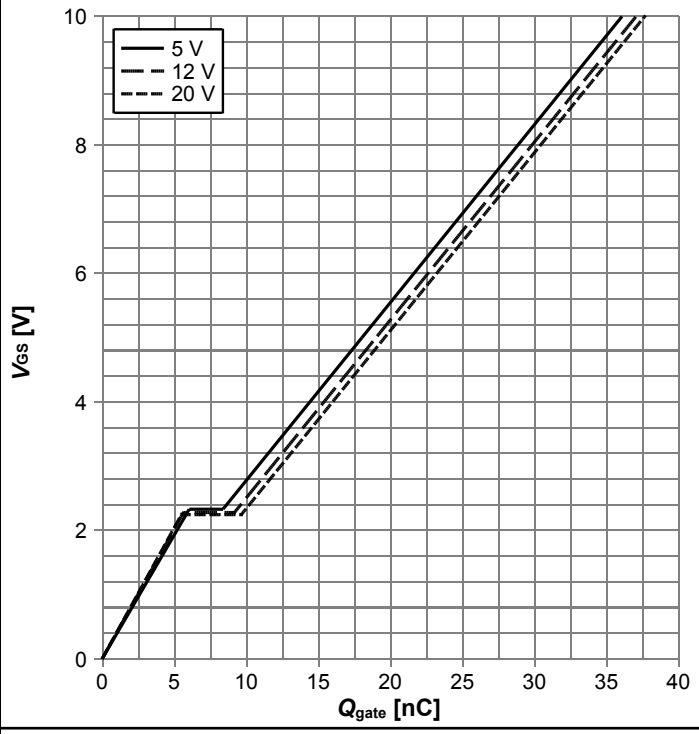
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



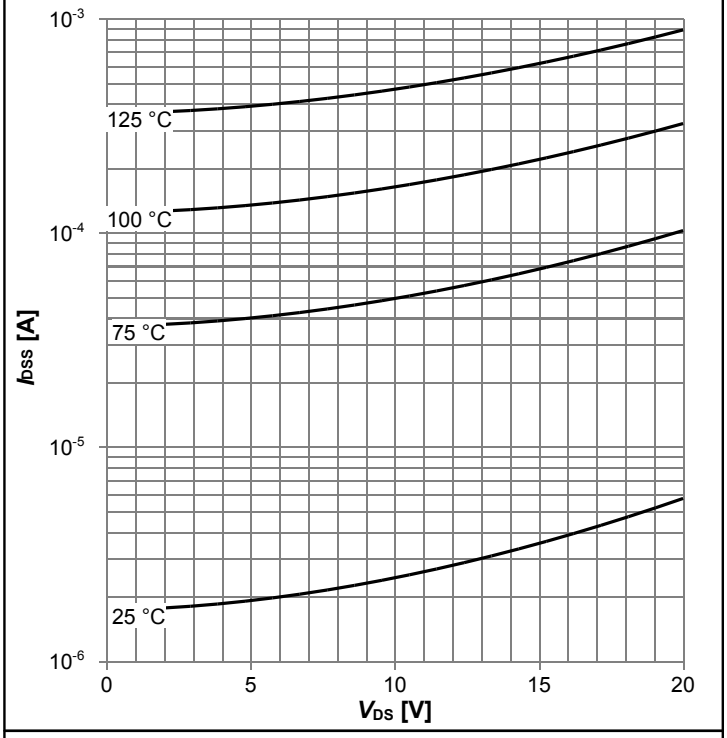
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



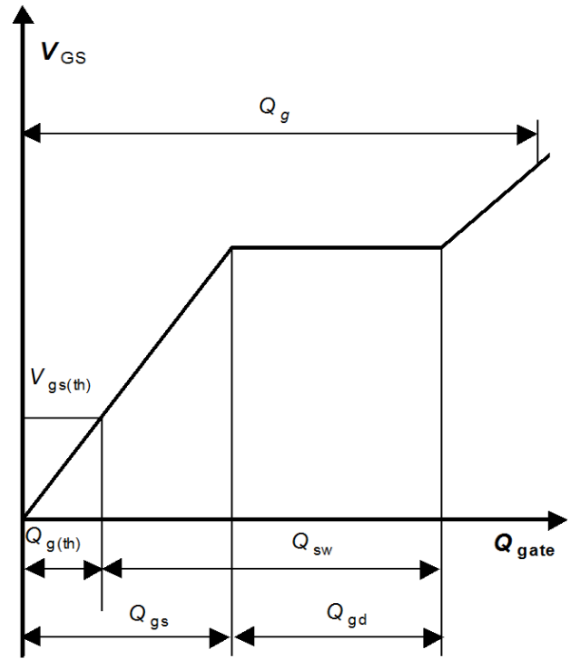
V_{GS}=f(Q_{gate}), I_D=20 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Typ. drain-source leakage current

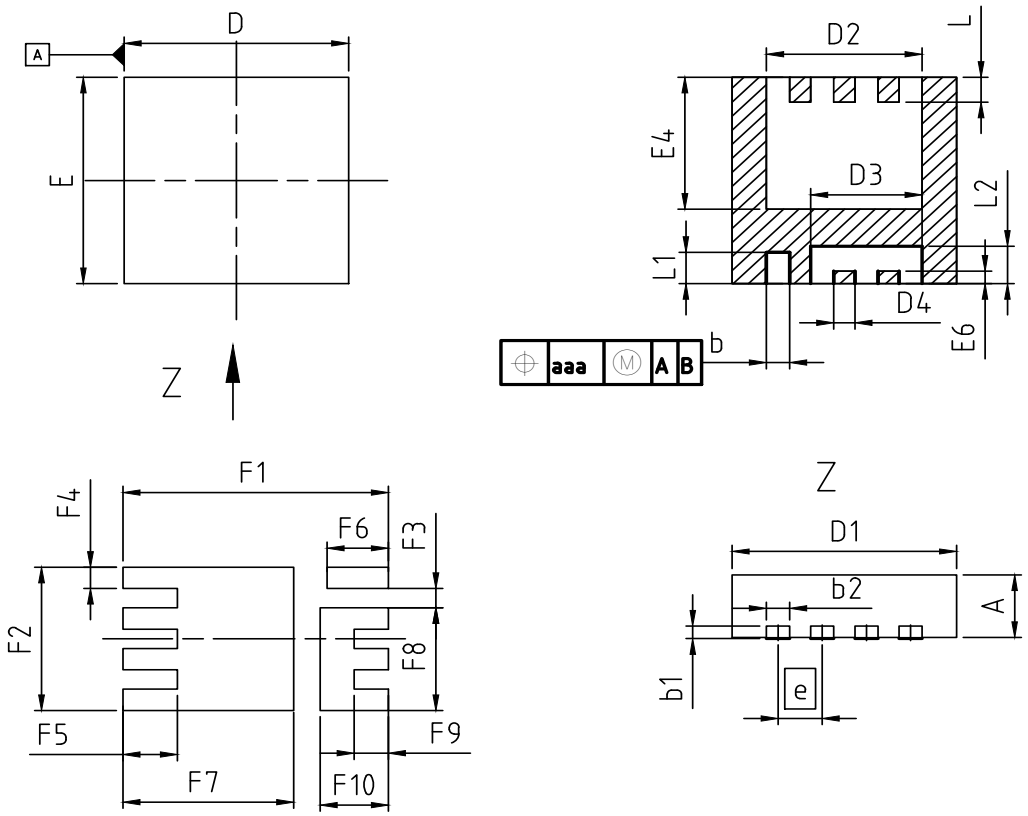


I_{DSS}=f(V_{DS}), V_{GS}=0 V; parameter: T_j

Diagram Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.24	0.44	0.009	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.19	2.39	0.086	0.094
D3	1.54	1.74	0.061	0.069
D4	0.21	0.41	0.008	0.016
E	3.20	3.40	0.126	0.134
E4	2.01	2.21	0.079	0.087
E6	0.10	0.30	0.004	0.012
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.30	0.51	0.012	0.020
L1	0.40	0.70	0.016	0.028
L2	0.50	0.70	0.020	0.028
aaa	0.25		0.010	
F1	3.90		0.154	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.80		0.031	
F6	1.00		0.039	
F7	2.51		0.099	
F8	1.64		0.065	
F9	0.50		0.020	

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Z8B00158553

SCALE
0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
27-12-2010

REVISION
02

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm/inches

Revision History

BSZ011NE2LS5I

Revision: 2020-10-23, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2019-02-04	Release of final version
2.1	2020-10-23	Update current rating

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