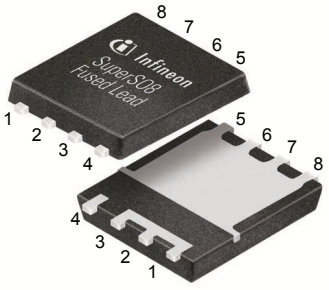
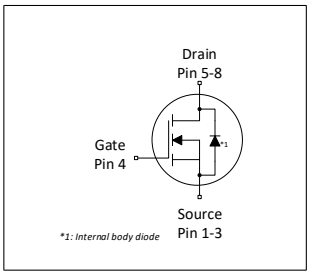
MOSFET

OptiMOS™ 6 Power-Transistor, 100 V

TDSON-8 FL (enlarged source interconnection)





Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Optimized for high frequency switching and synchronous rectification
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	8.05	mΩ
I_D	75	A
Q_{oss}	35	nC
Q_G(0V...10V)	19	nC
Q_{rr} (100A/µs)	31	nC

Type / Ordering Code	Package	Marking	Related Links
ISC080N10NM6	PG-TDSON-8 FL	080N10N6	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - -	- - - -	75 53 48 13	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=8 V, T_C=100 °C V_{GS}=10V, T_A=25°C, R_{thJA}=50°C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	300	A	T_A=25 °C
Avalanche current, single pulse[4]	I_{AS}	-	-	20	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	185	mJ	I_D=11 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	100 3.0	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.77	1.5	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area	R_{thJA}	-	-	50	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.3	2.8	3.3	V	V_{DS}=V_{GS}, I_D=36 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1.0 100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C[1)]
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	7.1 8.7	8.05 10	mΩ	V_{GS}=10 V, I_D=20 A V_{GS}=8 V, I_D=10 A
Gate resistance	R_G	0.6	1.2	1.8	Ω	-
Transconductance	g_{fs}	15	30	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1400	1800	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	310	390	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	9	13	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	6.4	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=10 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	1.5	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=10 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	10.7	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=10 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	4.3	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=10 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge[1)]	Q_{gs}	-	6.4	8.5	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 10 V
Gate charge at threshold[1)]	$Q_{g(th)}$	-	3.9	4.9	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 10 V
Gate to drain charge[1)]	Q_{gd}	-	3.4	5.1	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	5.9	-	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 10 V
Gate charge total[1)]	Q_g	-	19	24	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	17	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	35	44	nC	V_{DS}=50 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See ″Gate charge waveforms″ for parameter definition

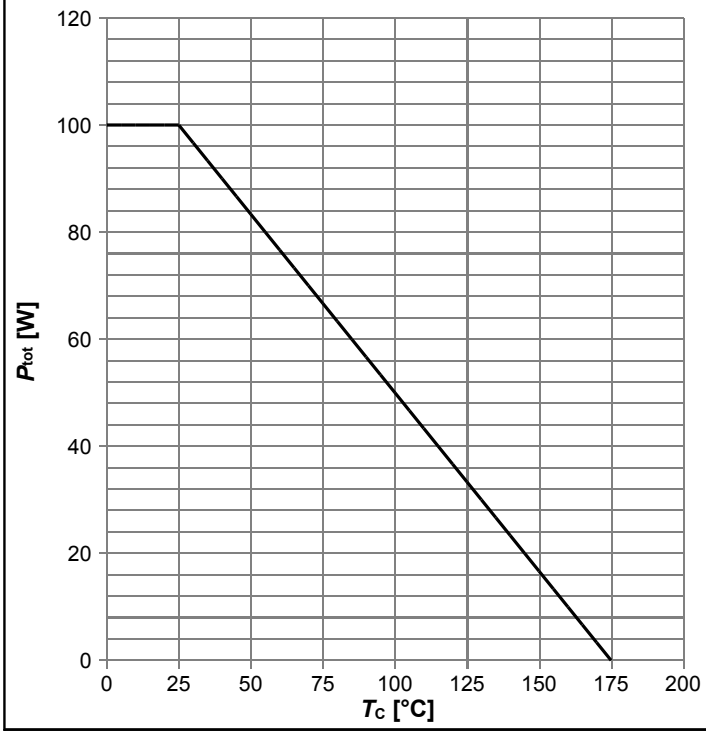
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	75	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	300	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.82	1.0	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	31.5	47	ns	V_R=50 V, I_F=10 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	31	46.5	nC	V_R=50 V, I_F=10 A, di_F/dt=100 A/µs
Reverse recovery time[1)]	t_{rr}	-	18	27	ns	V_R=50 V, I_F=10 A, di_F/dt=1000 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	140	210	nC	V_R=50 V, I_F=10 A, di_F/dt=1000 A/µs

[1)] Defined by design. Not subject to production test.

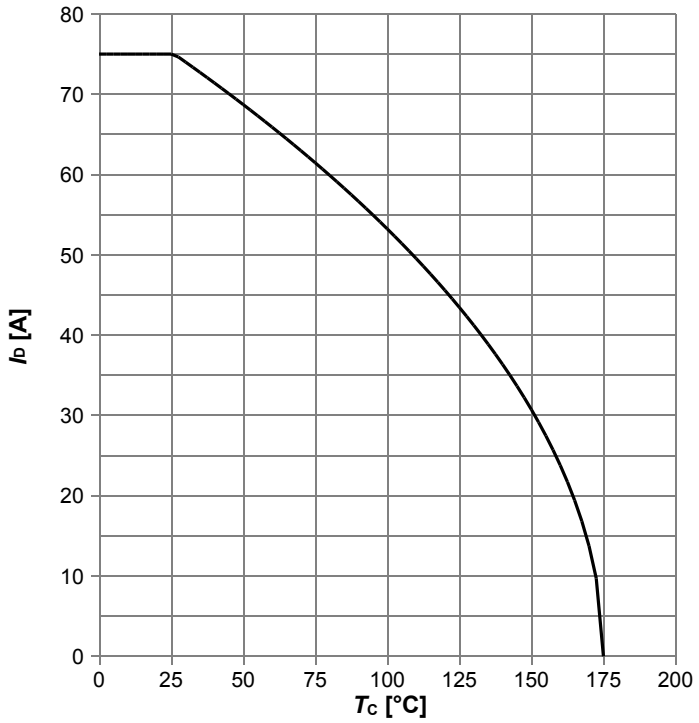
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



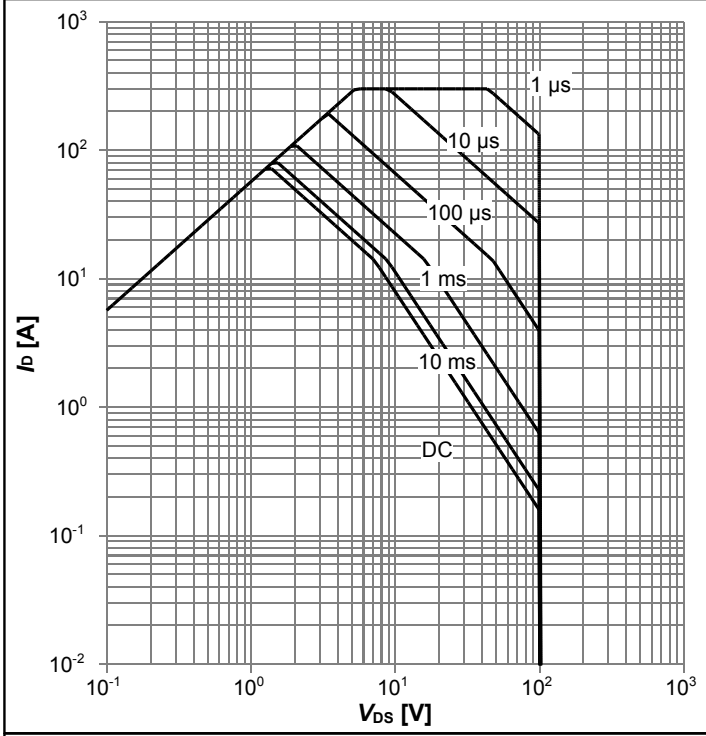
$P_{tot}=f(T_C)$

Diagram 2: Drain current



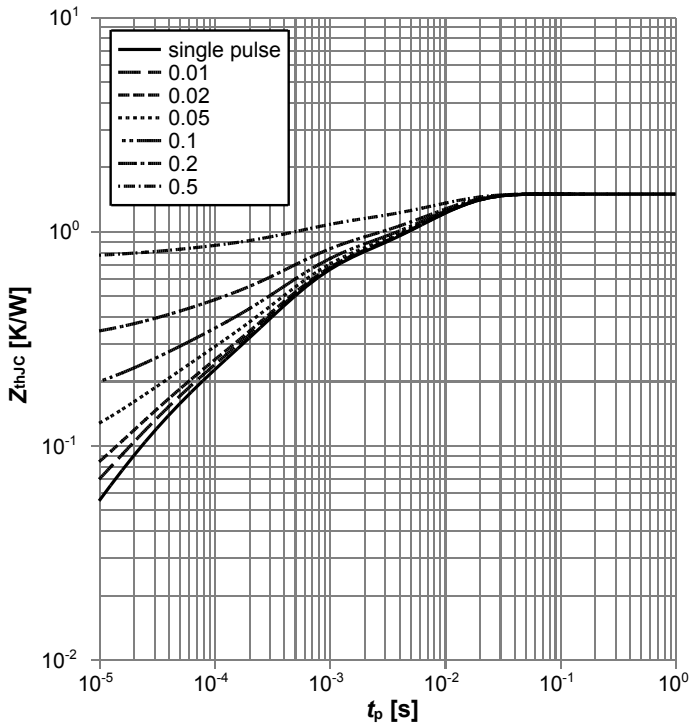
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



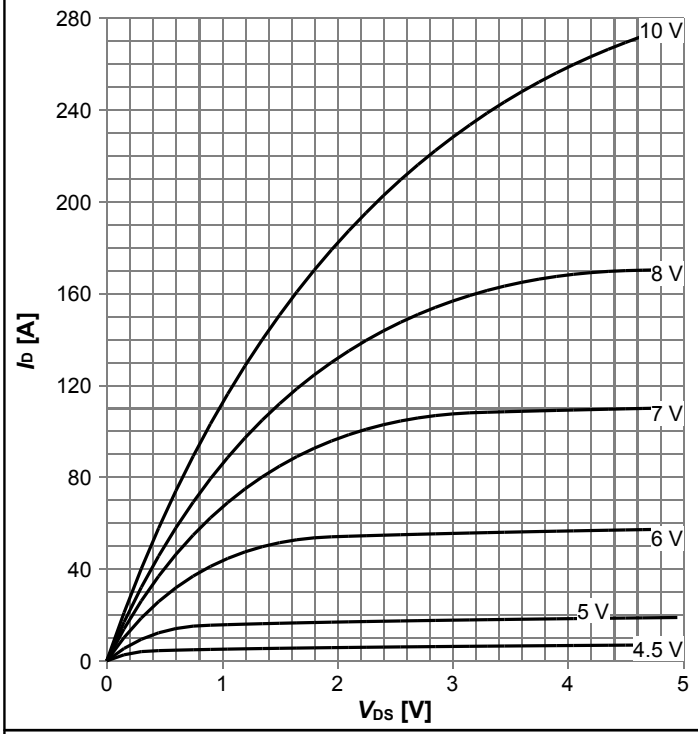
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



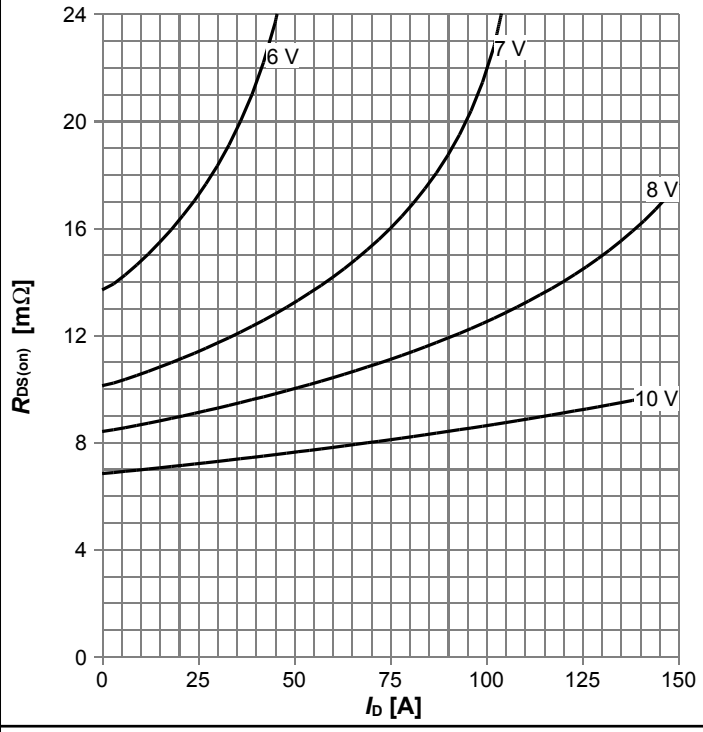
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



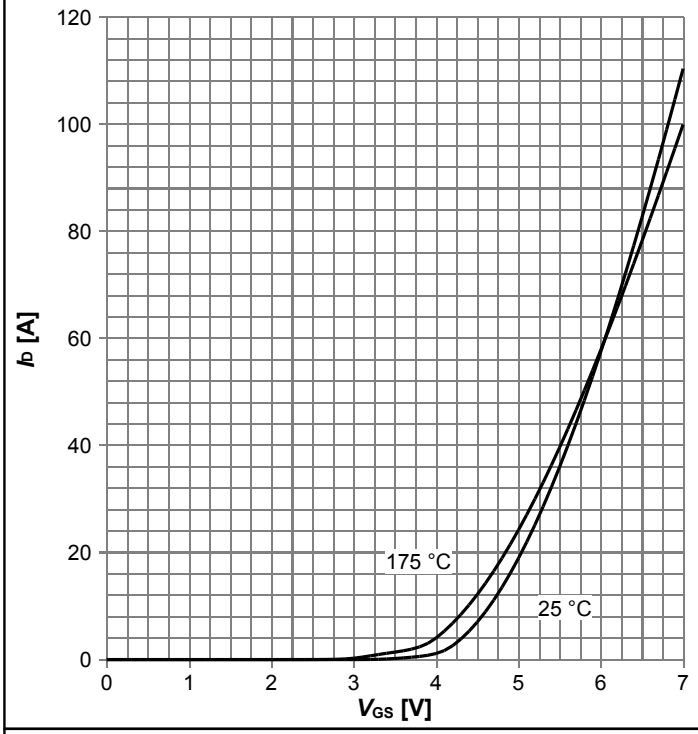
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



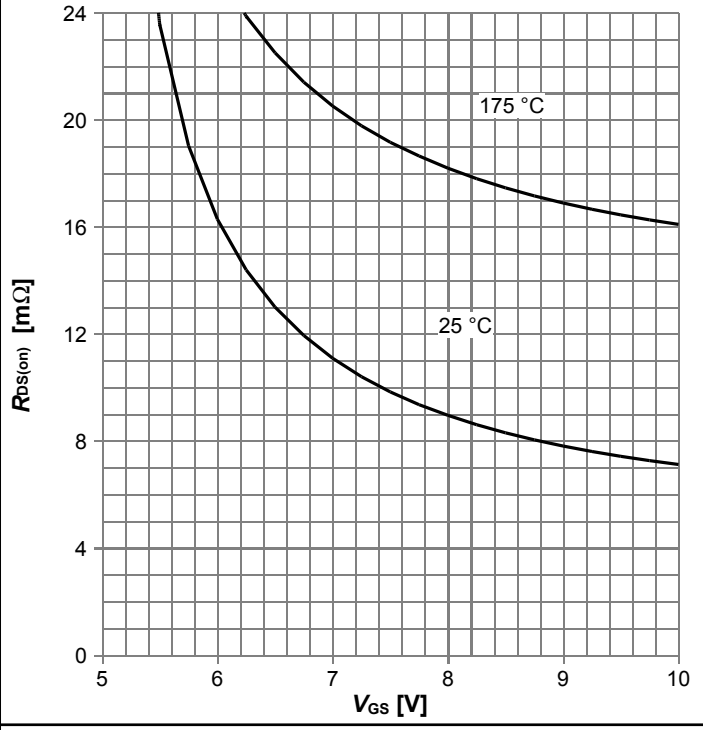
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



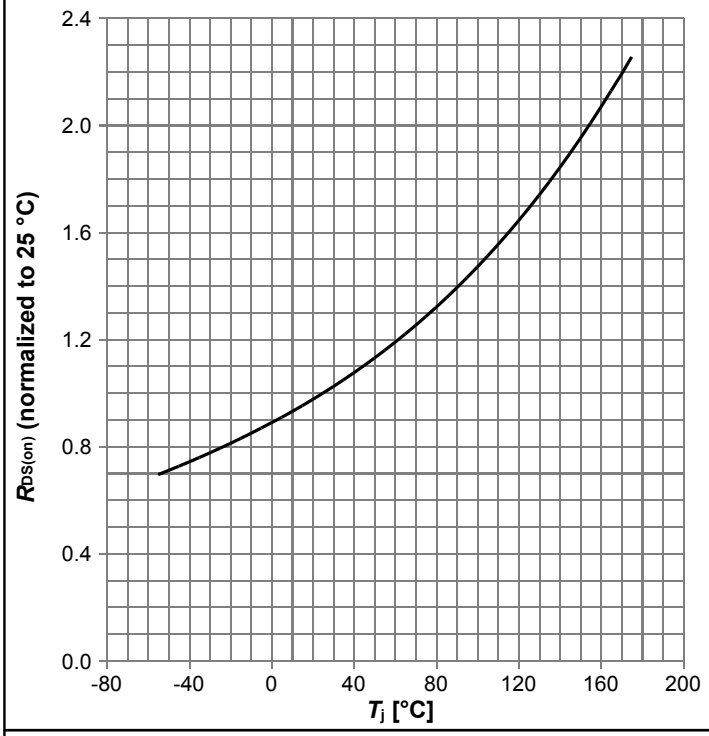
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



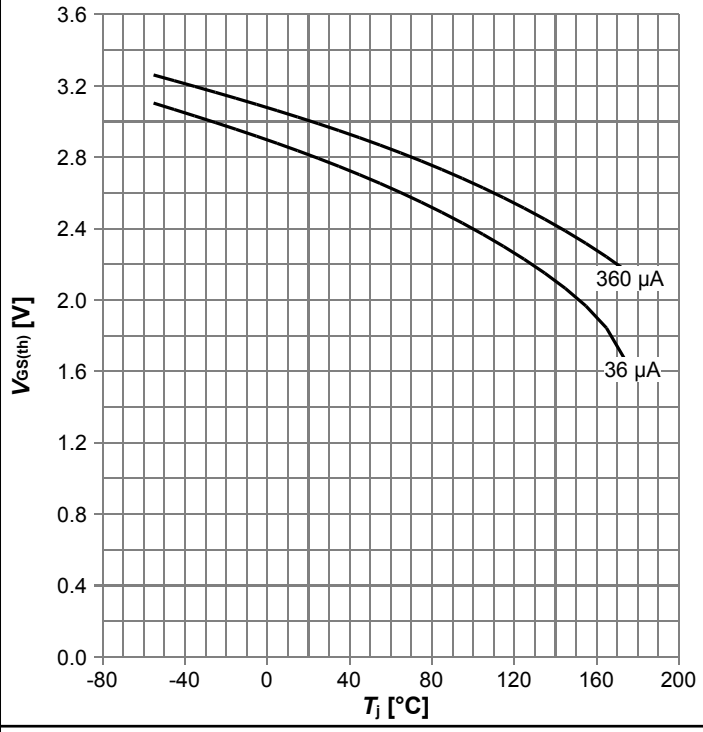
$R_{DS(on)}=f(V_{GS})$, $I_D=20$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



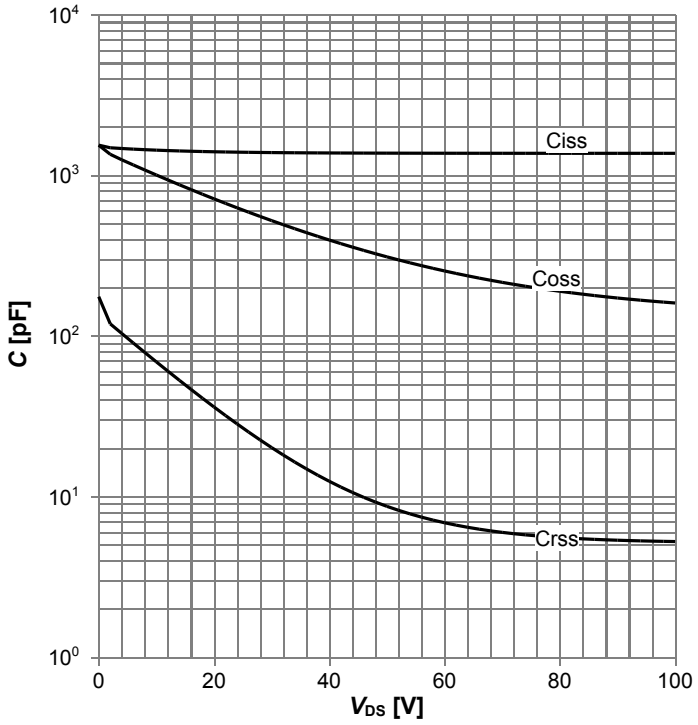
$R_{DS(on)}$=f(T_j), I_D=20 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



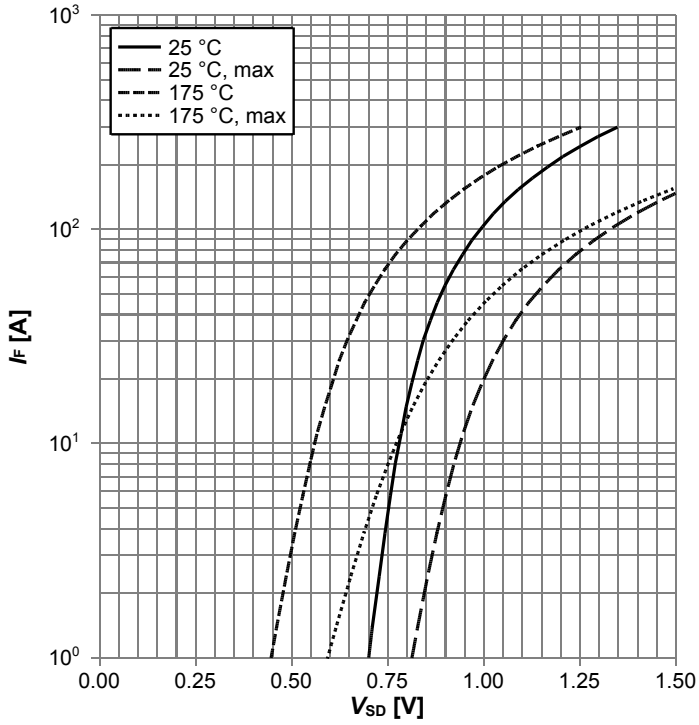
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



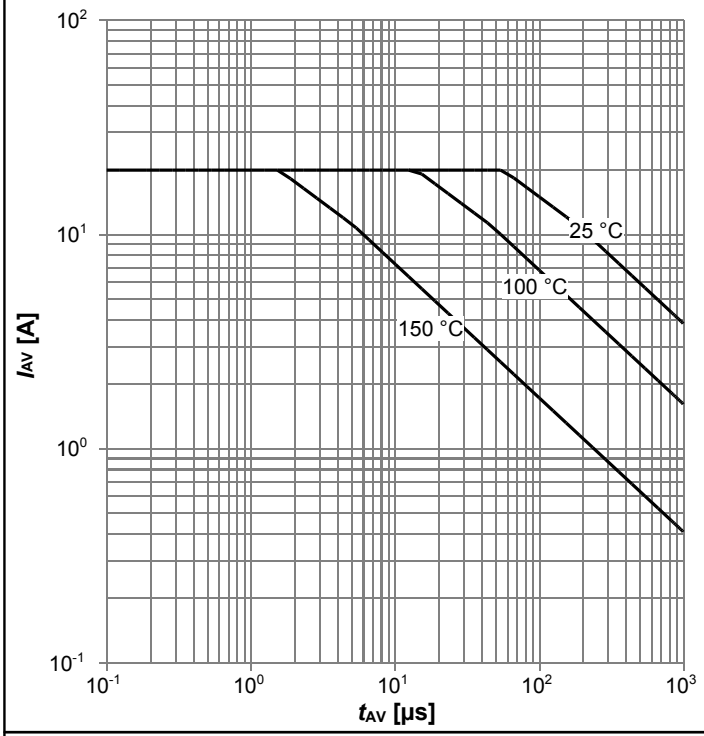
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



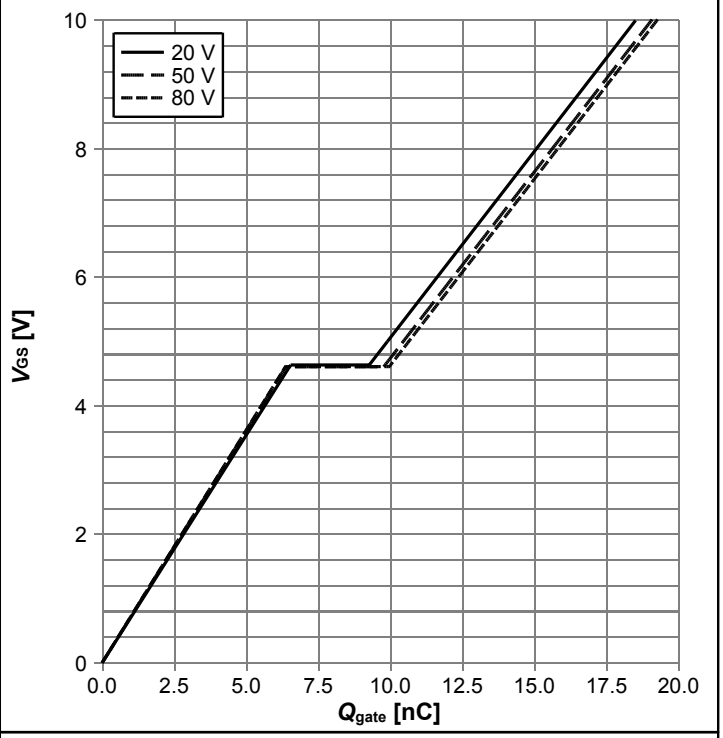
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



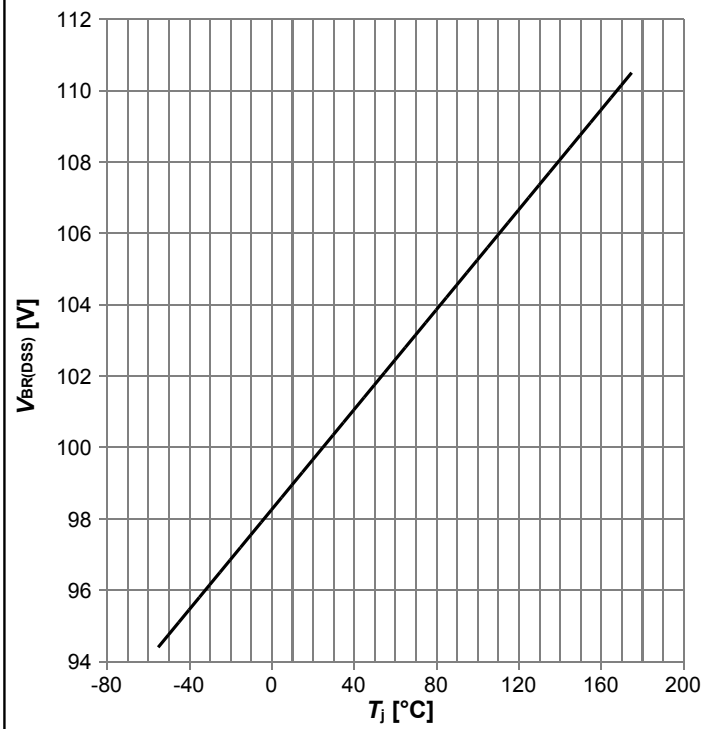
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



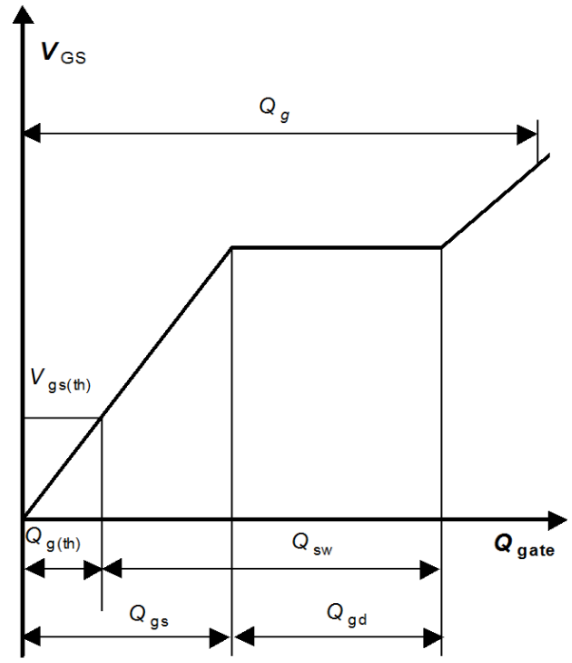
V_{GS}=f(Q_{gate}), I_D=10 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

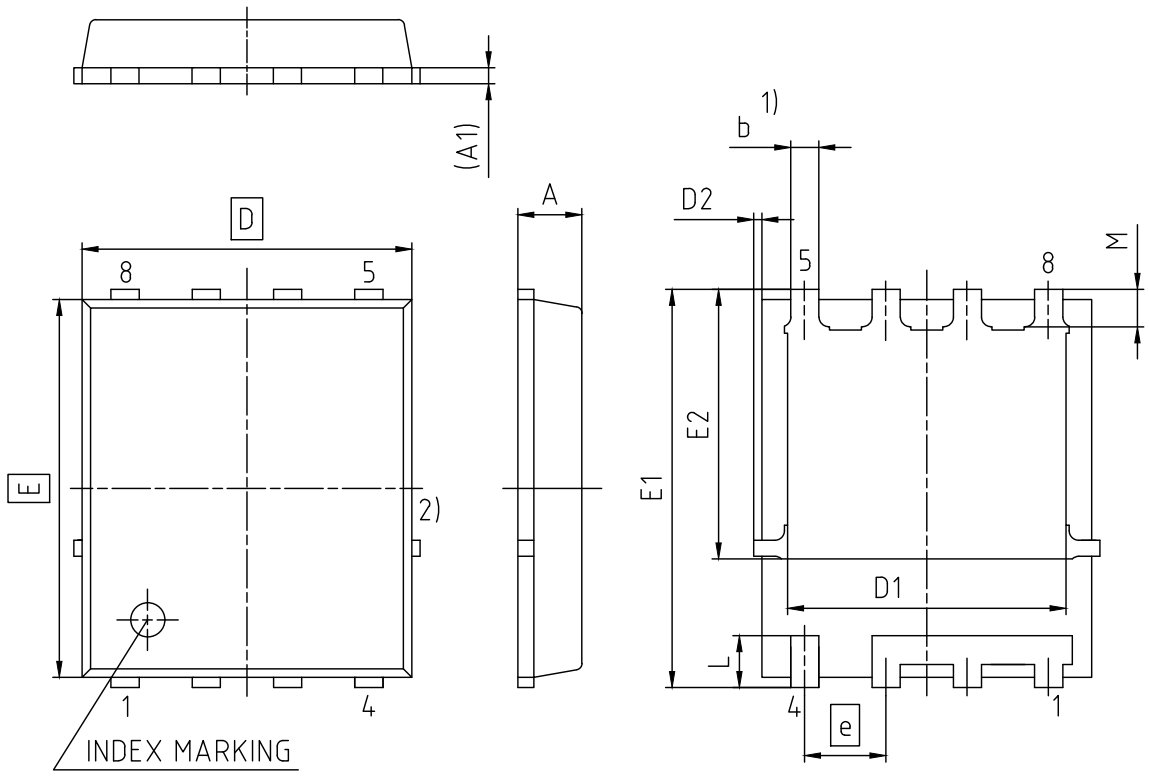


$V_{BR(DSS)}$=f(T_j); I_D=10 mA

Diagram Gate charge waveforms



5 Package Outlines



1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.26	0.54
D	4.80	5.35
D1	3.70	4.40
D2	0.00	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.42
e	1.27	
L	0.69	0.90
M	0.45	0.69

DOCUMENT NO. Z8B000193699
REVISION 04
SCALE 10:1 0 1 2 3mm
EUROPEAN PROJECTION
ISSUE DATE 05.11.2019

Figure 1 Outline PG-TDSON-8 FL, dimensions in mm

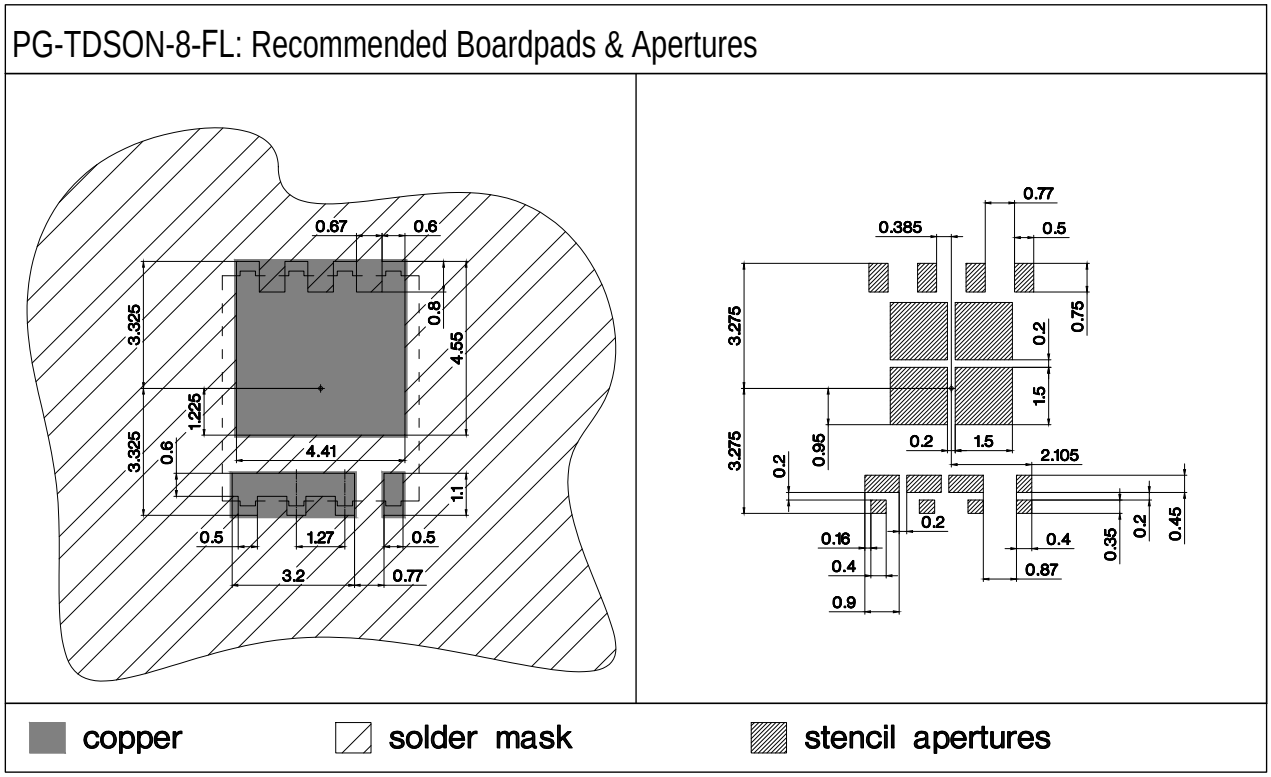


Figure 2 Outline Boardpads (TDSON-8 FL)

Revision History

ISC080N10NM6

Revision: 2023-02-07, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-07-05	Release of final version
2.1	2021-07-20	Update IAS
2.2	2023-02-07	Update SOA Diagram