

## Automotive MOSFET

## OptiMOS™ 5 Power-Transistor



## Features

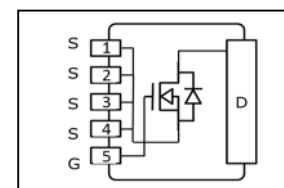
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL3 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

## Potential applications

General automotive applications.

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



## Product Summary

$V_{DS}$	40	V
$R_{DS(on),max}$	1.4	mΩ
$I_D$ (chip limited)	120	A

Type	Package	Marking
IAUA120N04S5N014	PG-HSOF-5-2	5N04N014



## **Table of Contents**

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	4
Electrical characteristics .....	4
Electrical characteristics diagrams .....	6
Package outline & footprint .....	10
Disclaimer .....	11
Revision history .....	12

## Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C = 25\text{ °C}, V_{GS} = 10\text{ V}^{1)}$	120	A
		$T_C = 100\text{ °C}, V_{GS} = 10\text{ V}^{2)}$	120	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C = 25\text{ °C}$	480	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D = 60\text{ A}$	190	mJ
Avalanche current, single pulse	$I_{AS}$	–	120	A
Gate source voltage	$V_{GS}$	–	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C = 25\text{ °C}$	136	W
Operating and storage temperature	$T_j, T_{stg}$	–	-55 ... +175	°C

### Thermal characteristics<sup>2)</sup>

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	–	–	–	1.10	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	6 cm <sup>2</sup> cooling area <sup>3)</sup>	–	–	60	

### Electrical characteristics

at T<sub>j</sub>=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V,$ $I_D = 1 mA$	40	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 60 \mu A$	2.2	2.8	3.4	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 40 V, V_{GS} = 0 V,$ $T_j = 25 \text{ }^\circ C$	–	–	1	$\mu A$
		$V_{DS} = 40 V, V_{GS} = 0 V,$ $T_j = 125 \text{ }^\circ C$ <sup>2)</sup>	–	–	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS} = 20 V, V_{DS} = 0 V$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 7 V, I_D = 60 A$	–	1.50	1.60	m $\Omega$
		$V_{GS} = 10 V, I_D = 60 A$	–	1.20	1.40	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

## Dynamic characteristics<sup>2)</sup>

Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V},$ $f = 1\text{ MHz}$	-	3630	4828	pF
Output capacitance	$C_{oss}$		-	990	1317	
Reverse transfer capacitance	$C_{rss}$		-	46	69	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 120\text{ A}, R_G = 3.5\ \Omega$	-	7	-	ns
Rise time	$t_r$		-	4	-	
Turn-off delay time	$t_{d(off)}$		-	14	-	
Fall time	$t_f$		-	7	-	

## Gate Charge Characteristics<sup>2)</sup>

Gate to source charge	$Q_{gs}$	$V_{DD} = 32\text{ V}, I_D = 120\text{ A},$ $V_{GS} = 0\text{ to }10\text{ V}$	-	16	21	nC
Gate to drain charge	$Q_{gd}$		-	13	20	
Gate charge total	$Q_g$		-	62	82	
Gate plateau voltage	$V_{plateau}$		-	4.6	-	V

## Reverse Diode

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C = 25\text{ °C}$	-	-	120	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	480	
Diode forward voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_F = 60\text{ A},$ $T_j = 25\text{ °C}$	-	0.8	1.1	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R = 20\text{ V}, I_F = 50\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	45	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	41	-	nC

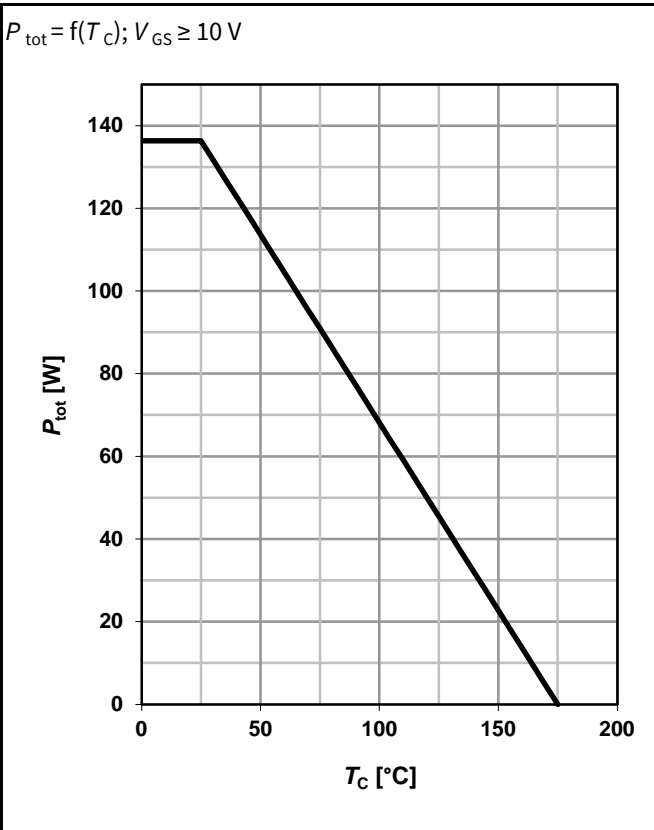
<sup>1)</sup> Current is limited by package; with a  $R_{thjc} = 1.1\text{ K/W}$  the chip is able to carry 230 A at 25°C.

<sup>2)</sup> The parameter is not subject to production test- verified by design/characterization.

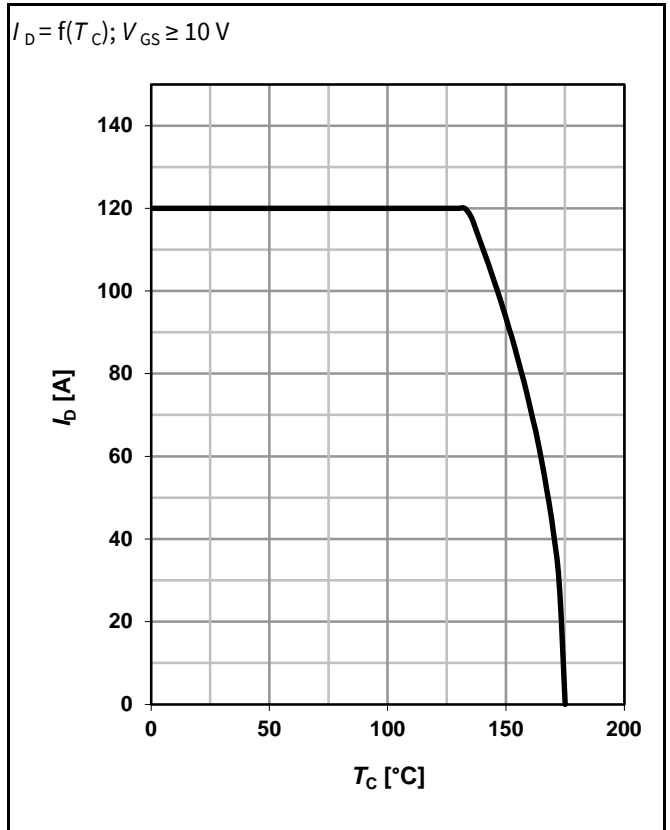
<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

### Electrical characteristics diagrams

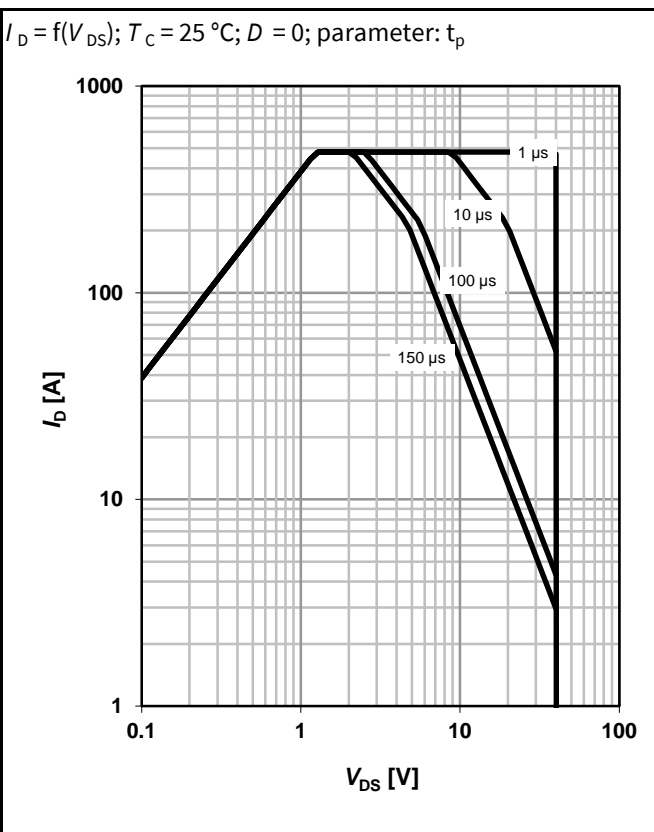
#### 1 Power dissipation



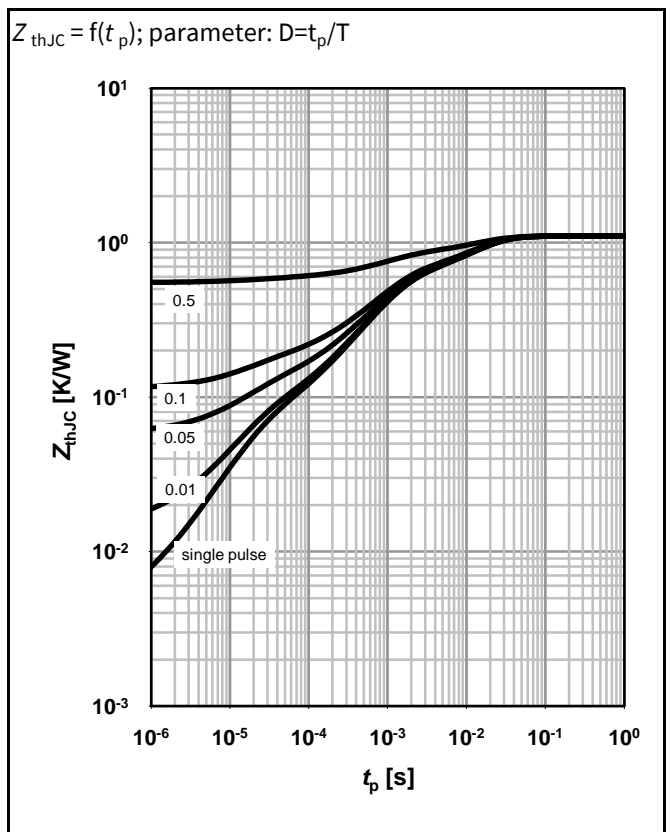
#### 2 Drain current



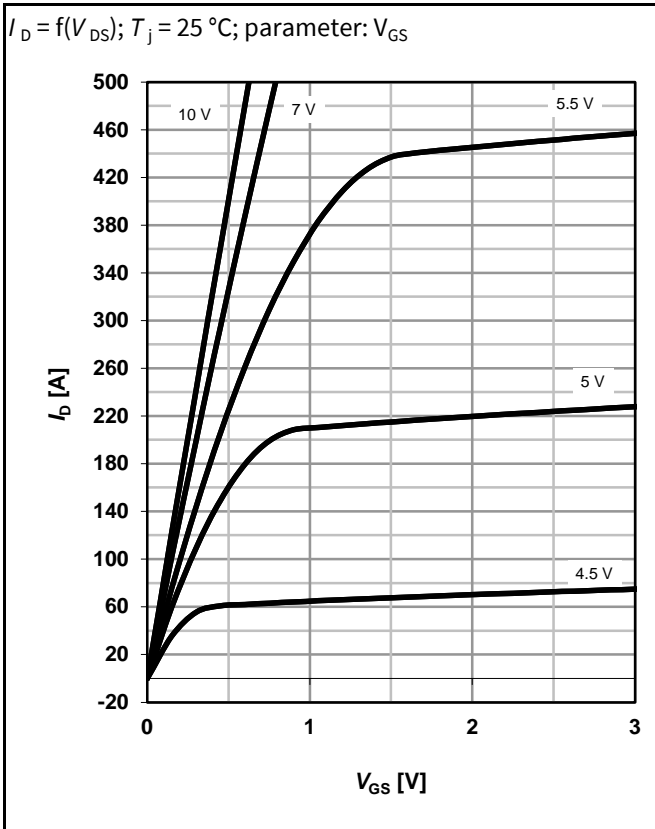
#### 3 Safe operating area



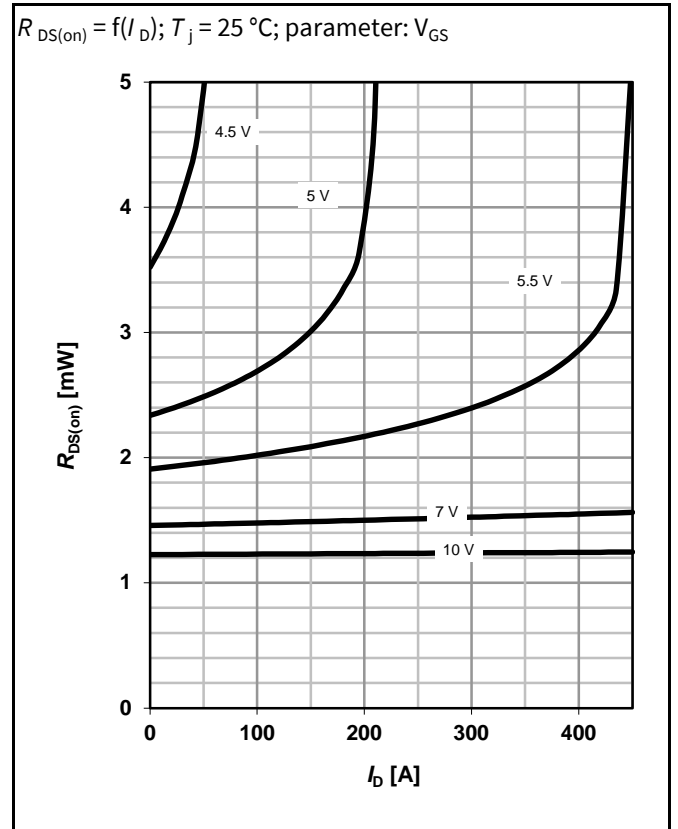
#### 4 Max. transient thermal impedance



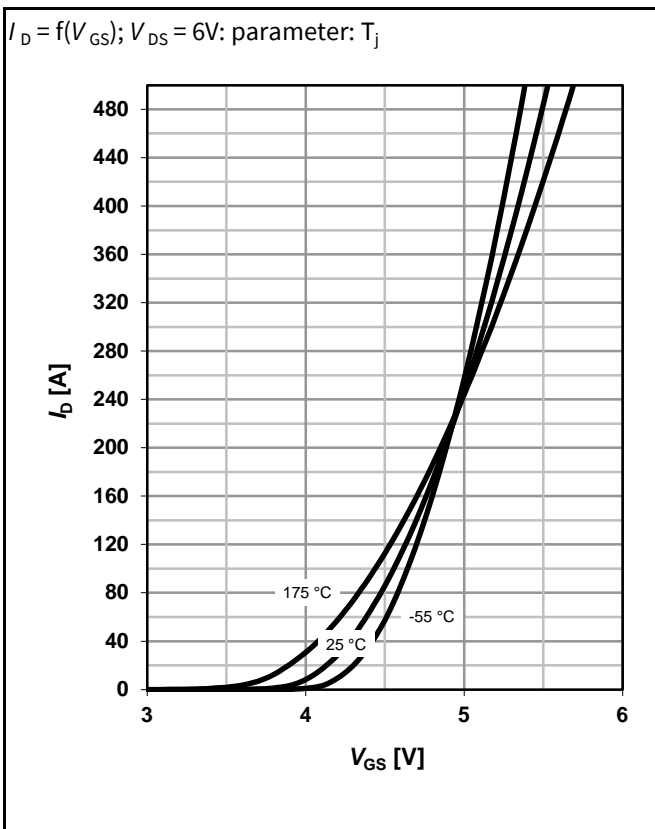
5 Typ. output characteristics



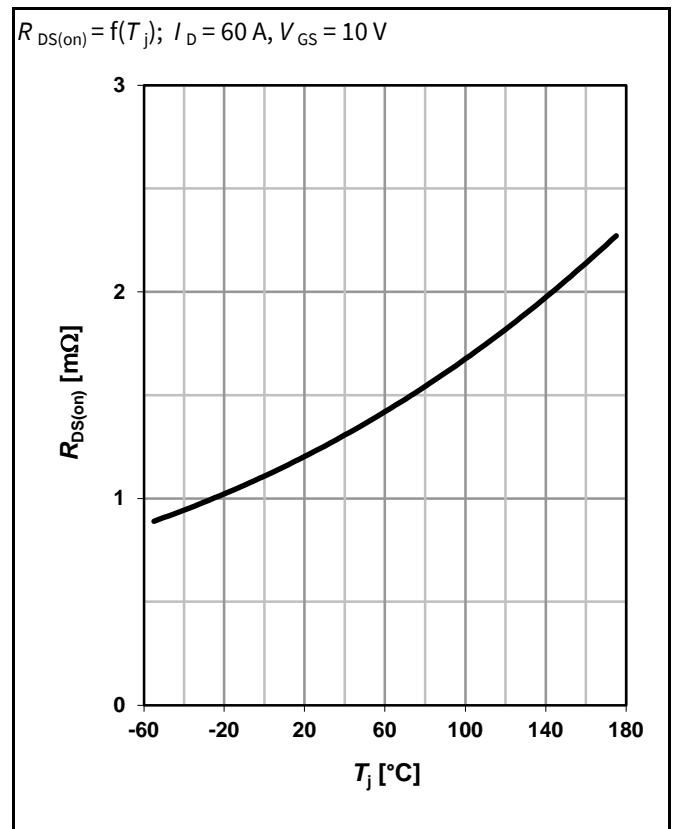
6 Typ. drain-source on-state resistance



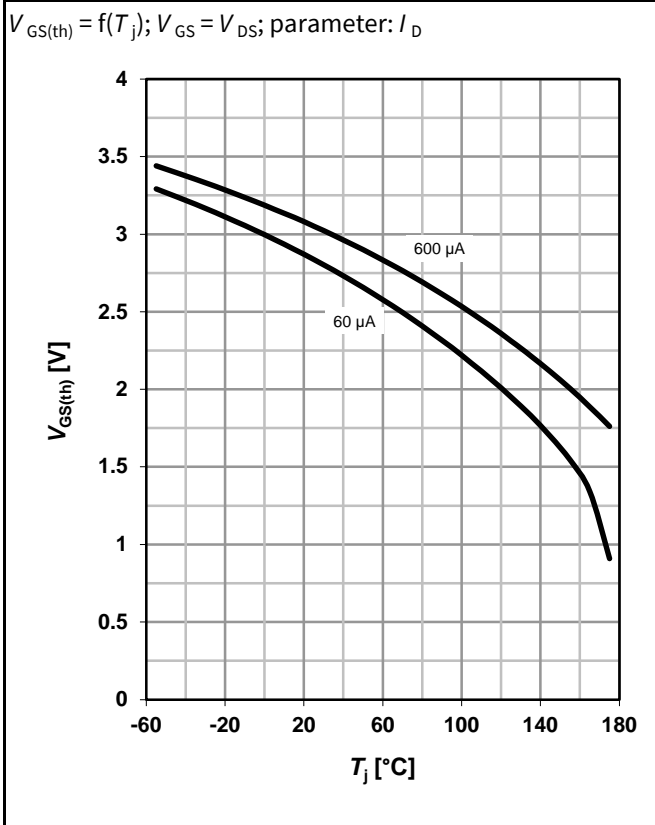
7 Typ. transfer characteristics



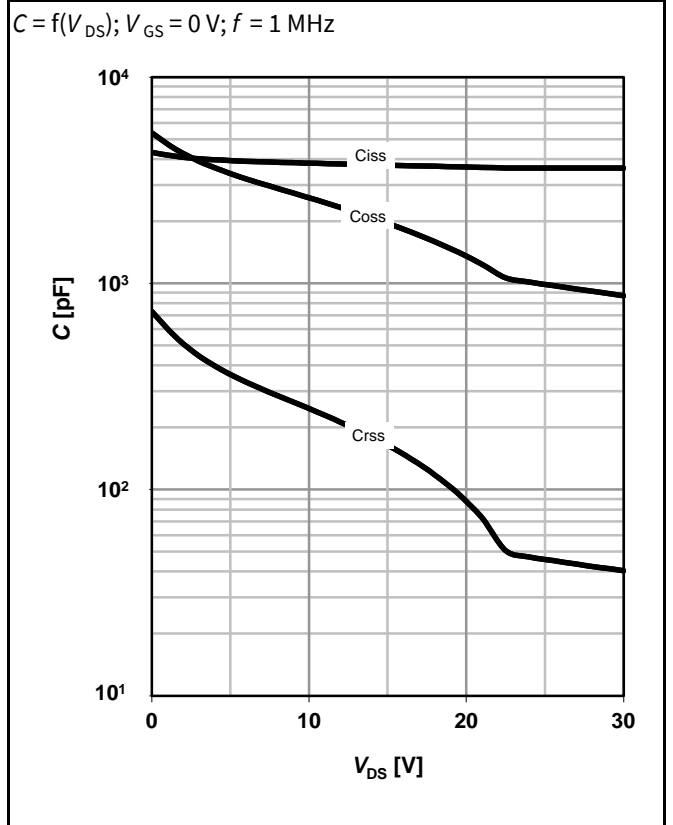
8 Typ. drain-source on-state resistance



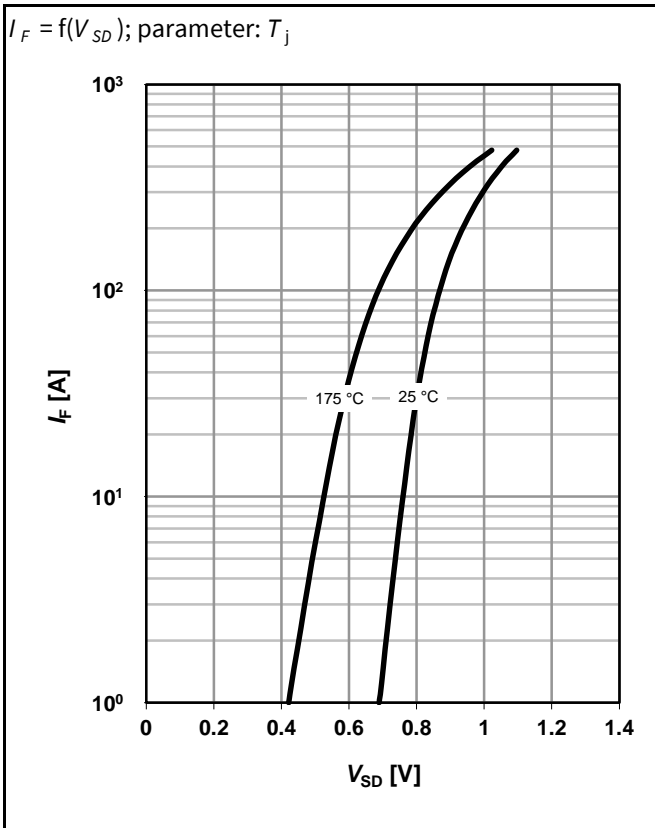
9 Typ. gate threshold voltage



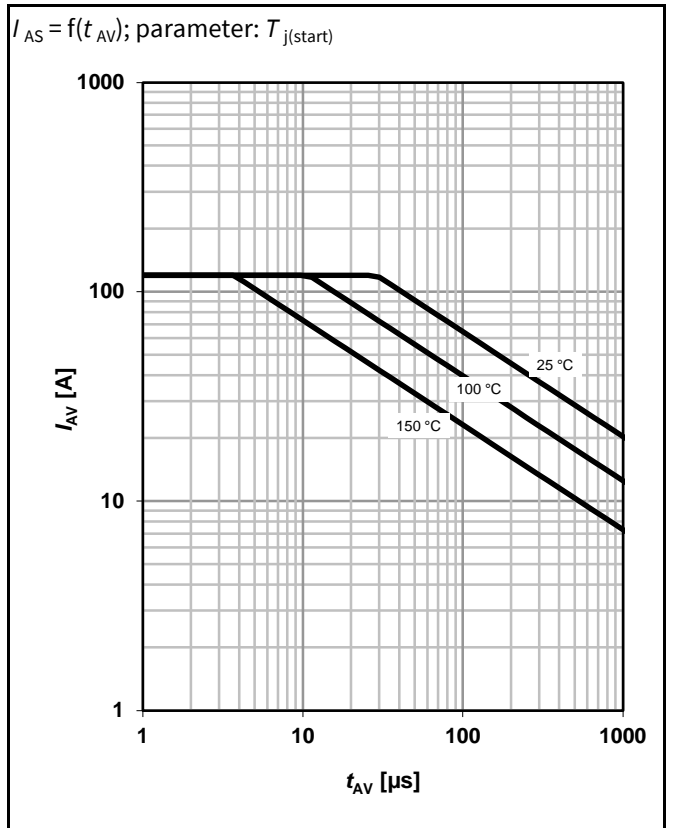
10 Typ. capacitances



11 Typical forward diode characteristics

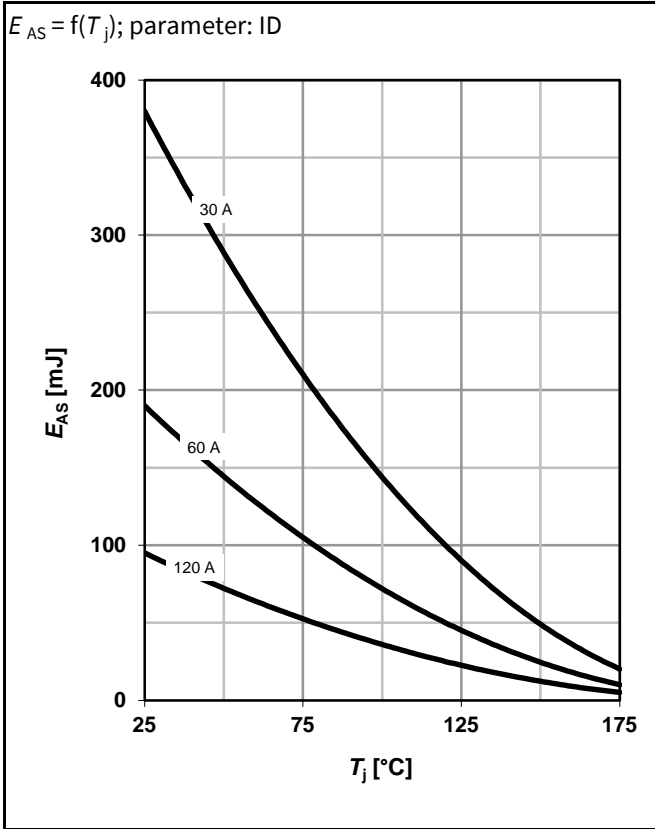


12 Typ. avalanche characteristics

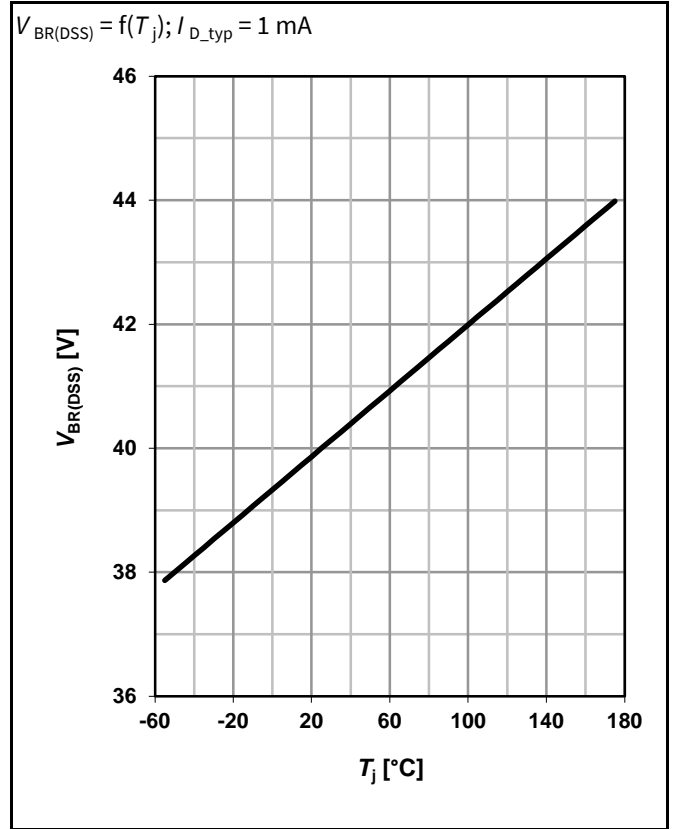




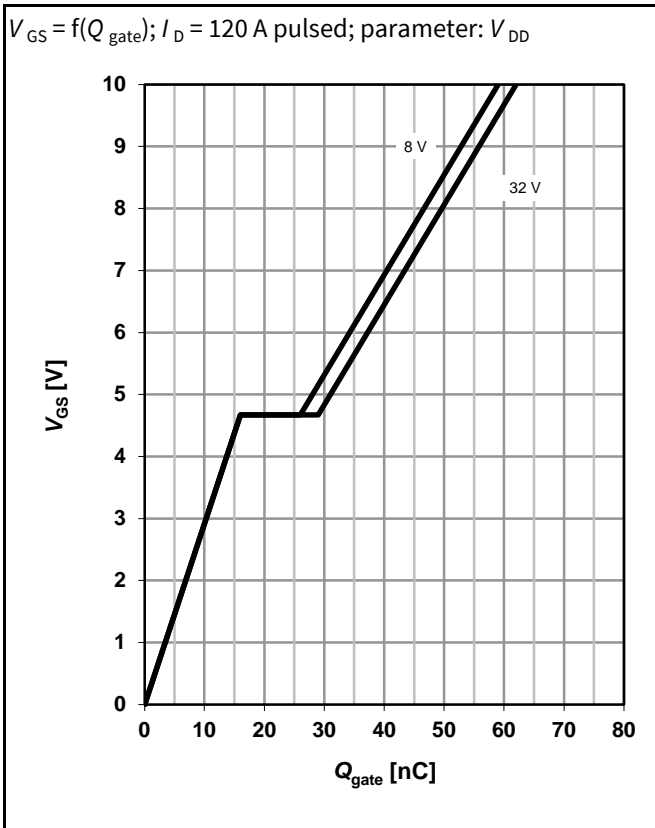
13 Typical avalanche energy



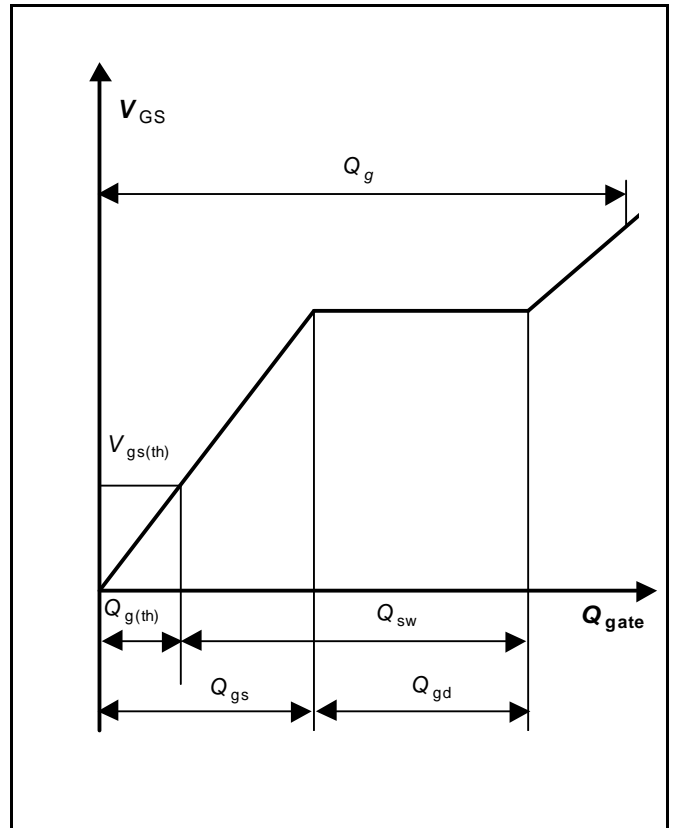
14 Drain-source breakdown voltage



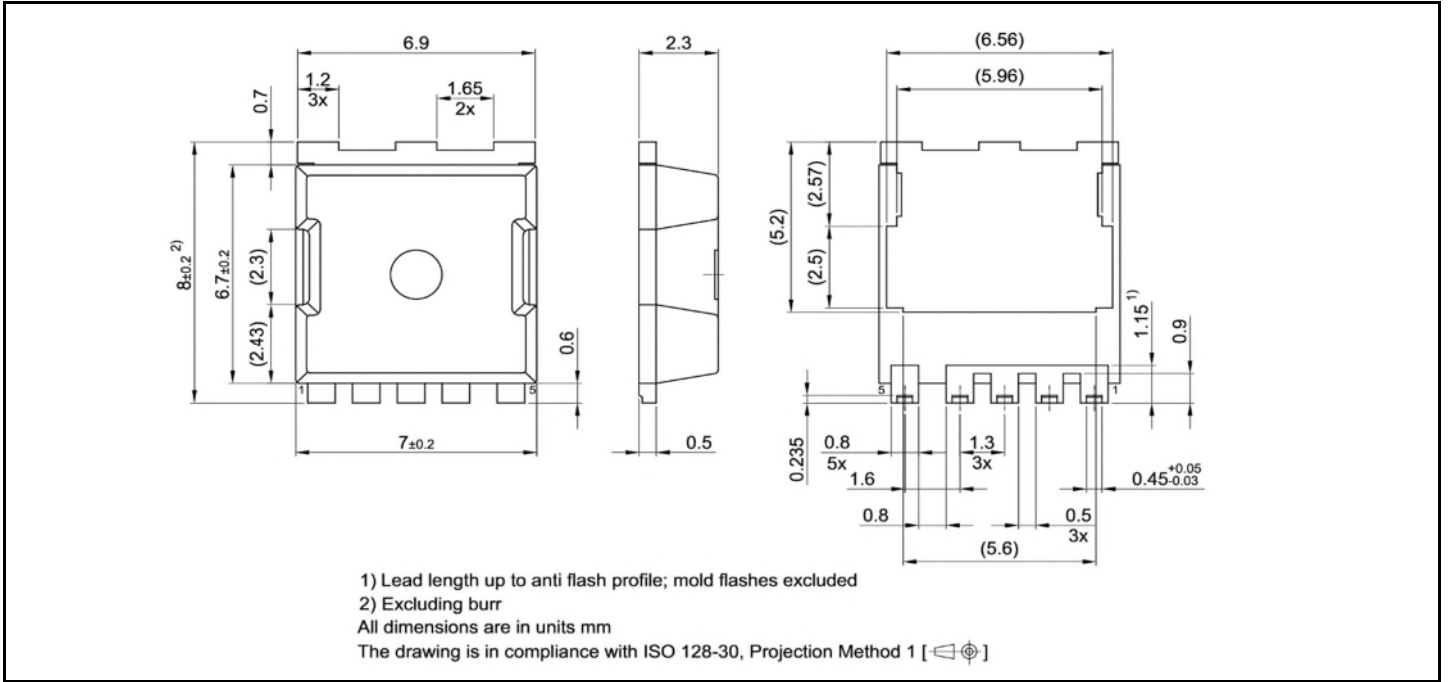
15 Typ. gate charge



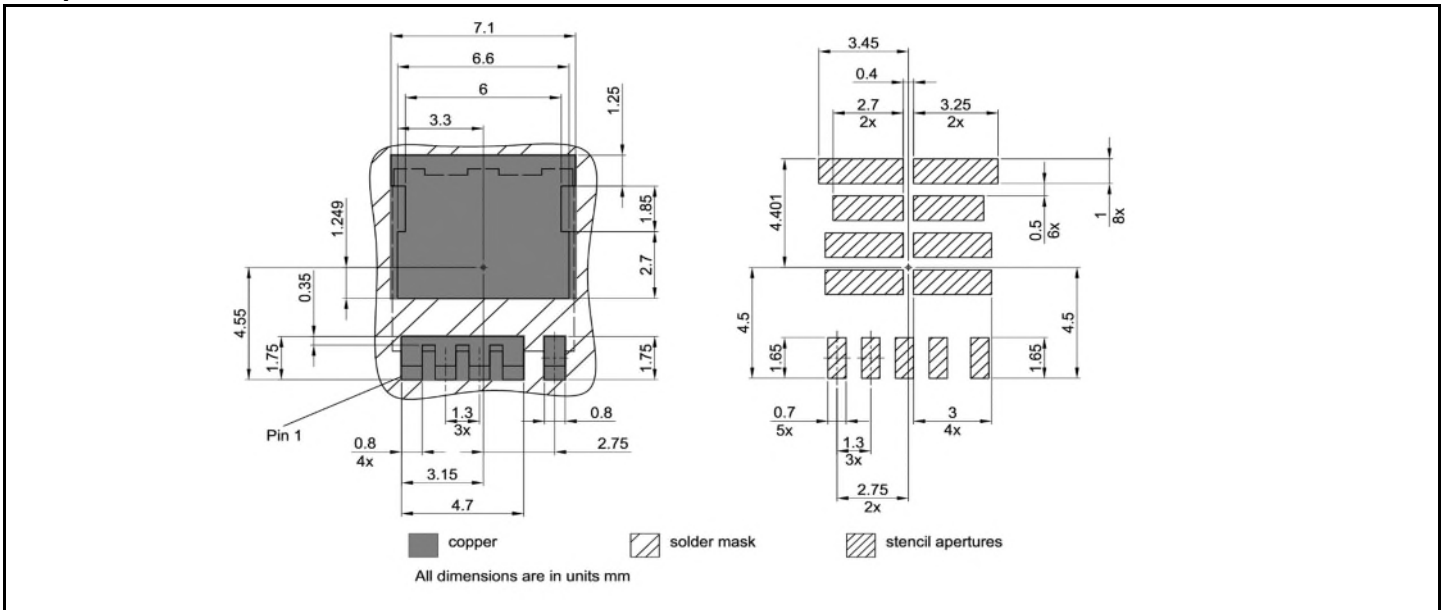
16 Gate charge waveforms



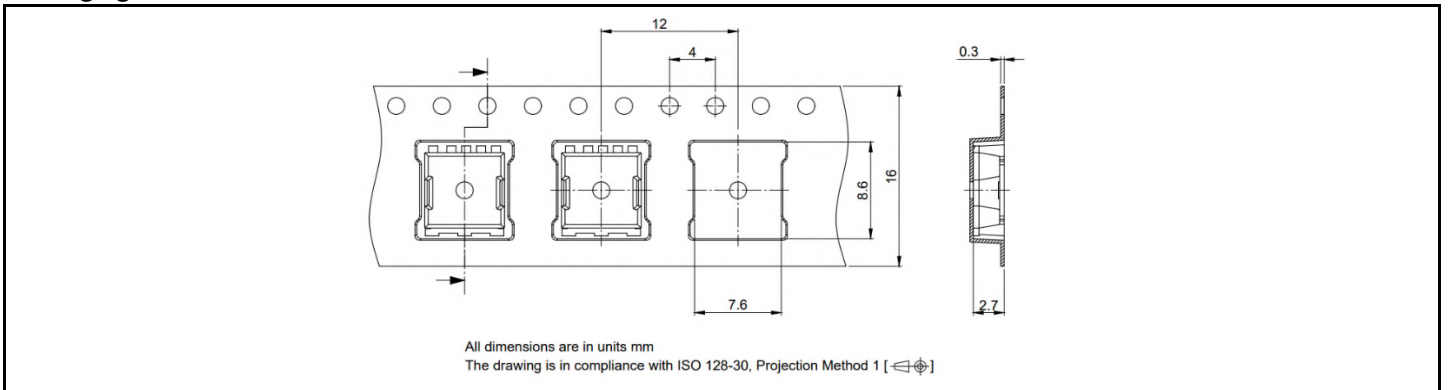
## Package Outline



## Footprint



## Packaging



**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
Revision 1.0	11.04.2019	Final Data Sheet
Revision 1.1	24.01.2022	Editorial changes, package drawing added
Revision 1.2	11.09.2023	SOA diagram and $I_D$ condition in figures 8 and 11 updated

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