HARRIS
SEMICONDUCTOR

IRFD220, IRFD221, IRFD222, IRFD223

0.7A and 0.8A, 150V and 200V, 0.8 and 1.2 Ohm, N-Channel Power MOSFETs

January 1998

Features

- 0.7A and 0.8A, 150V and 200V
- $r_{DS(ON)} = 0.8\Omega$ and 1.2Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

| PART NUMBER	PACKAGE	BRAND
IRFD220	HEXDIP	IRFD220
IRFD221	HEXDIP	IRFD221
IRFD222	HEXDIP	IRFD222
IRFD223	HEXDIP	IRFD223

NOTE: When ordering, use the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09600.

Symbol

Packaging

HEXDIP

File Number **2317.2**
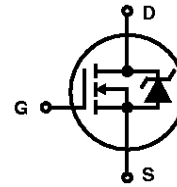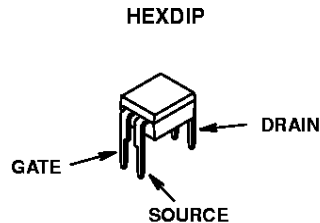
Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

		IRFD220	IRFD221	IRFD222	IRFD223	UNITS
Drain to Source Breakdown Voltage (Note 1)............	V_{DS}	200	150	200	150	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	200	150	200	150	V
Continuous Drain Current............................	I_D	0.8	0.8	0.7	0.7	A
Pulsed Drain Current (Note 3)	I_{DM}	6.4	6.4	5.6	5.6	A
Gate to Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 1)		0.008	0.008	0.008	0.008	W/$^{\circ}$C
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	85	85	85	85	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^{\circ}$C
Maximum Temperature for Soldering						
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	300	300	$^{\circ}$C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	260	260	$^{\circ}$C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
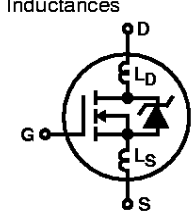
NOTE:

1. $T_J = 25^{\circ}C$ to $T_J = 125^{\circ}C$.

Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

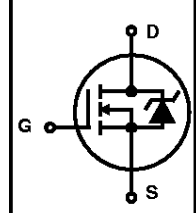| PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$, (Figure 9)				
IRFD220, IRFD222			200	-	-	V
IRFD221, IRFD223			150	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, $V_{GS} = 0V$	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, $V_{GS} = 0V$, $T_C = 125^{\circ}C$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)}$ x $r_{DS(ON)MAX}$, $V_{GS} = 10V$, (Figure 6)				
IRFD220, IRFD221			0.8	-	-	A
IRFD222, IRFD223			0.7	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm20V$	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 0.4A$, $V_{GS} = 10V$, (Figures 7, 8)				
IRFD220, IRFD221			-	0.5	0.8	Ω
IRFD222, IRFD223			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)}$ x $r_{DS(ON)MAX}$, $I_D = 0.4A$ (Figure 11)	0.5	1.1	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5$ x Rated BV_{DSS}, $I_D \approx 0.8A$,	-	20	40	ns
Rise Time	t_r	$R_G = 9.1\Omega$, $R_L = 74\Omega$, $V_{GS} = 10V$, (Figures 16, 17), MOSFET Switching Times are	-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$	Essentially Independent of Operating Tempera-ture	-	50	100	ns
Fall Time	t_f		-	30	60	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 10V$, $I_D \approx 0.8A$, $V_{DS} = 0.8$ x Rated BV_{DSS}, $I_{G(REF)} = 1.5mA$, (Figures 13, 18, 19) Gate Charge is Essentially Independent of Operating Temperature	-	11	15	nC
Gate to Source Charge	Q_{gs}		-	6.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	5.0	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1MHz, (Figure 10)	-	450	-	pF
Output Capacitance	C_{OSS}		-	150	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	40	-	pF

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Internal Drain Inductance	L_D	Measured from the Drain Lead, 2mm (0.08in) from Package to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 2mm (0.08in) from Header to Source Bonding Pad		-	6.0	-	nH
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	120	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	0.8	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	6.4	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 0.8A$, $V_{GS} = 0V$ (Figure 12)		-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, $I_{SD} = 0.8A$, $dI_{SD}/dt = 100A/\mu s$		-	150	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^oC$, $I_{SD} = 0.8A$, $dI_{SD}/dt = 100A/\mu s$		-	0.6	-	μC

NOTES:

2. Pulse test: pulse width $\leq$ 300μs, duty cycle $\leq$ 2%.

3. Repetitive rating: pulse width limited by maximum junction temperature.

4. $V_{DD} = 25V$, starting $T_J = 25^oC$, L = 12.62mH, $R_G = 50\Omega$, peak $I_{AS} = 3.5A$. See Figures 14, 15.

Typical Performance Curves Unless Otherwise Specified
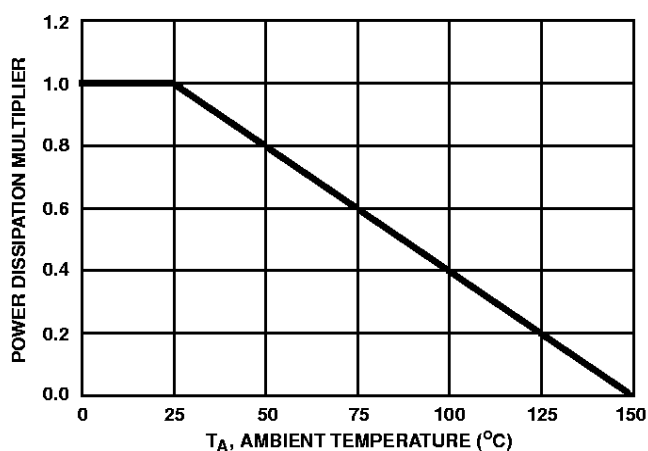
FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE
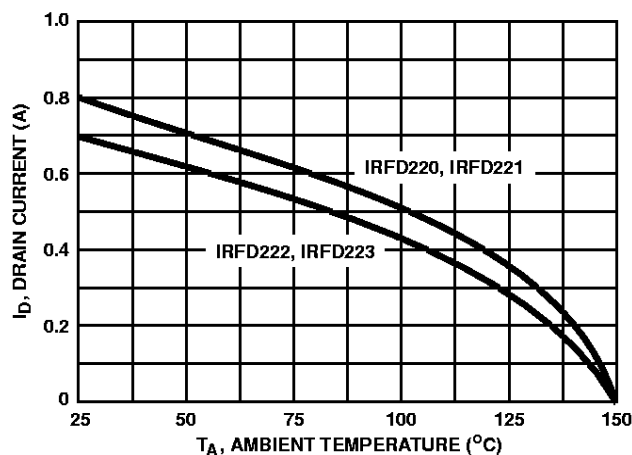
FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)
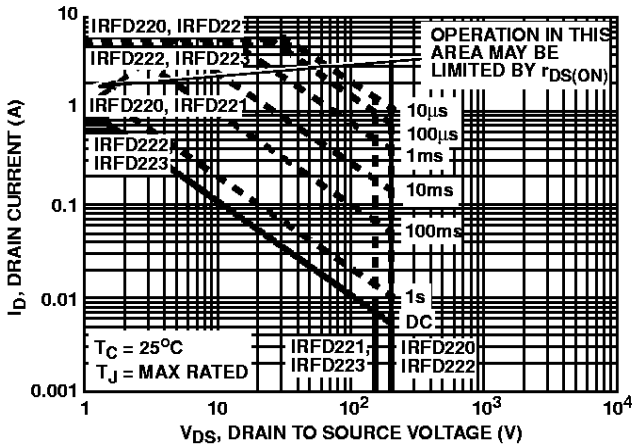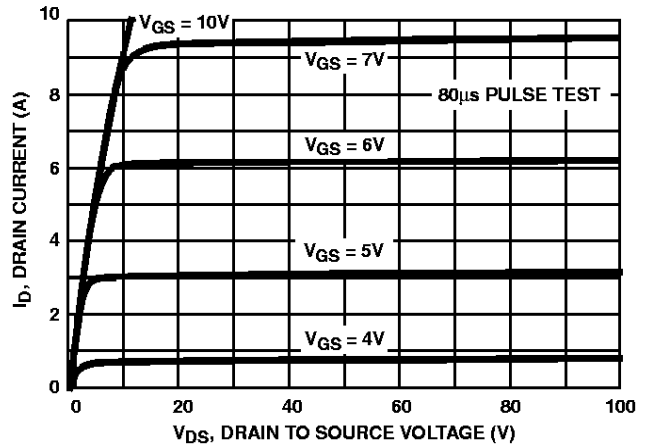
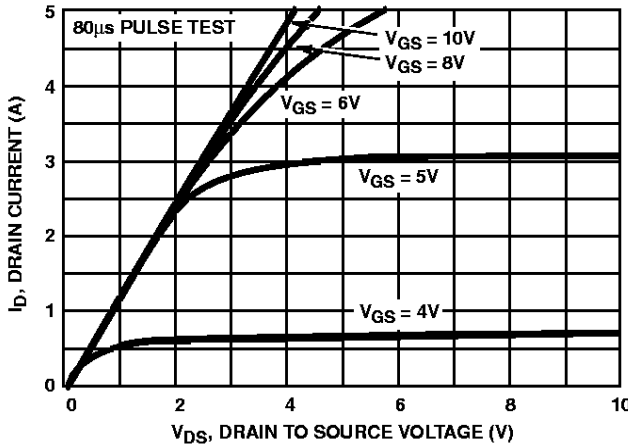FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

FIGURE 4. OUTPUT CHARACTERISTICS

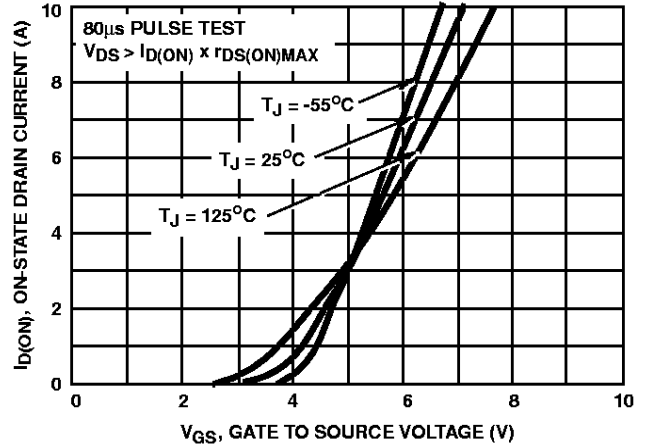FIGURE 5. SATURATION CHARACTERISTICS
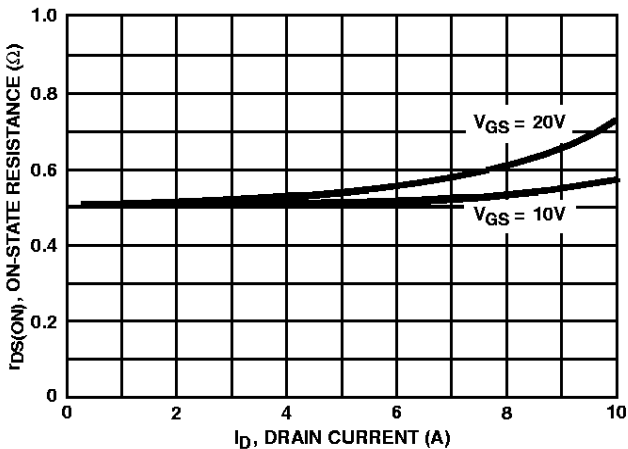
FIGURE 6. TRANSFER CHARACTERISTICS

FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE
VOLTAGE AND DRAIN CURRENT
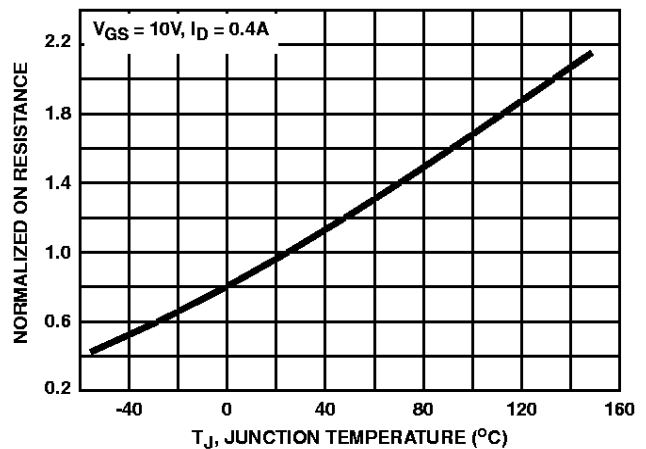
FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE
vs JUNCTION TEMPERATURE

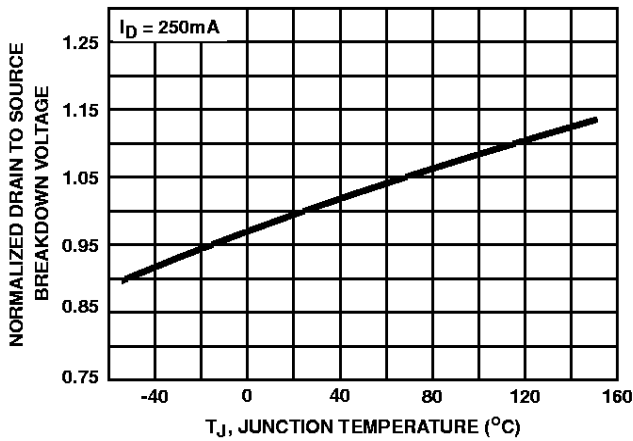*Typical Performance Curves* Unless Otherwise Specified **(Continued)**

FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN
VOLTAGE vs JUNCTION TEMPERATURE
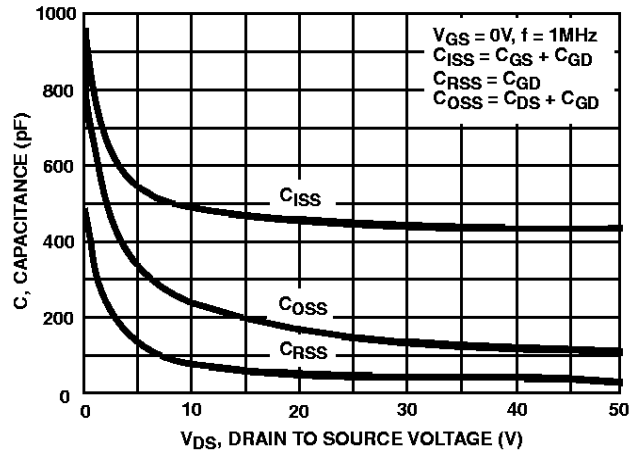
FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE
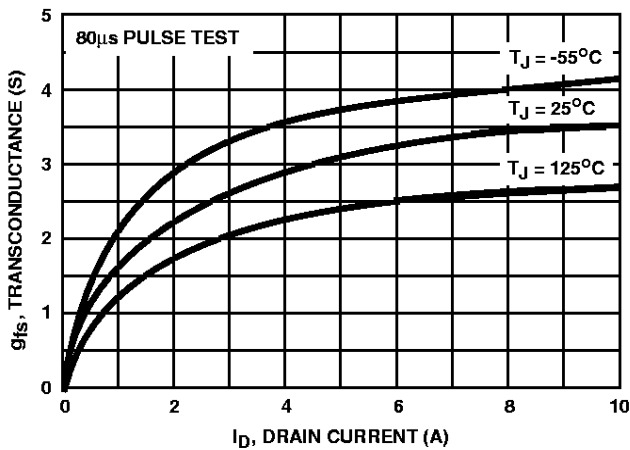
FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT
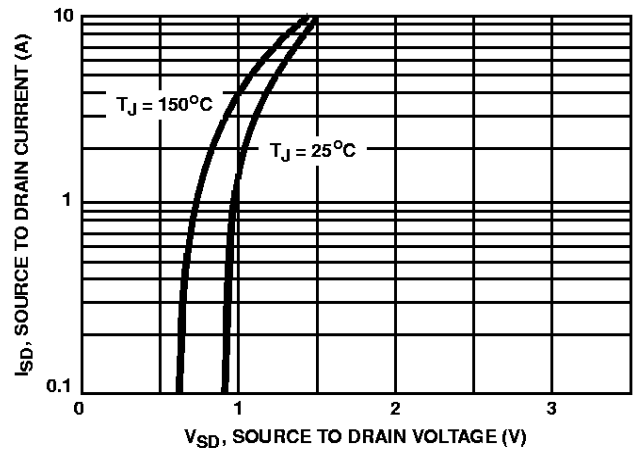
FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE
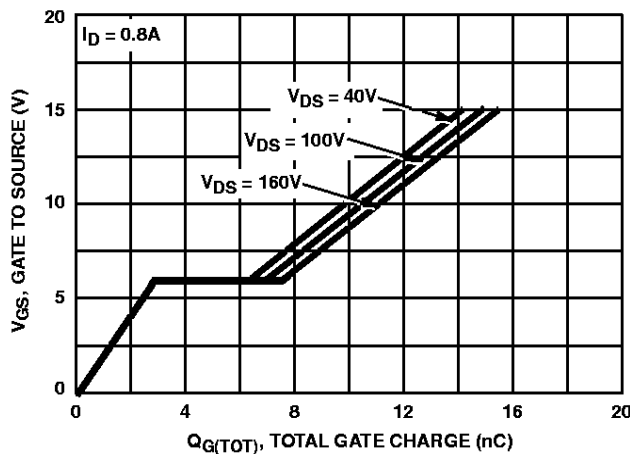
FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE
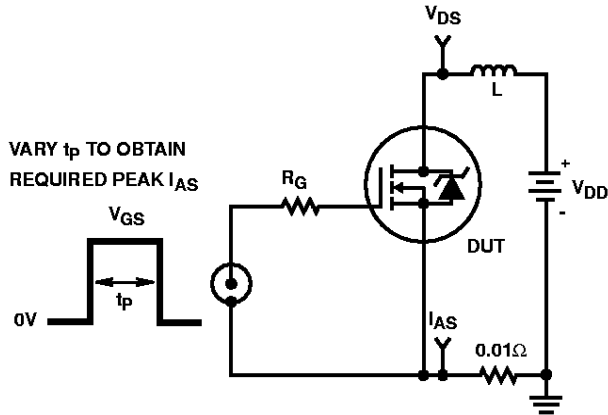
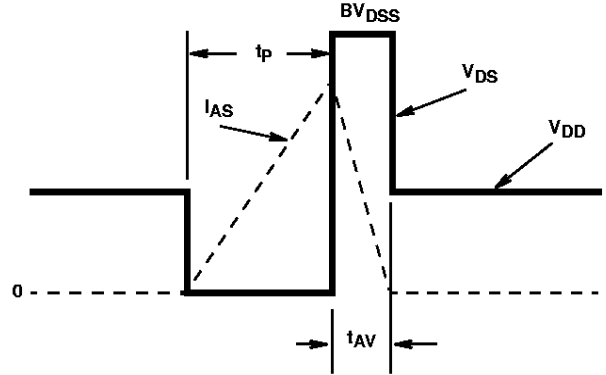## Test Circuits and Waveforms

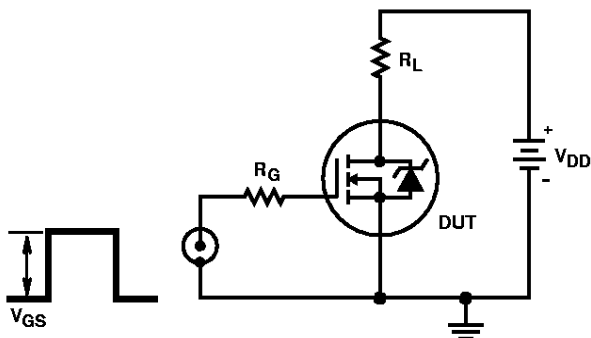FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

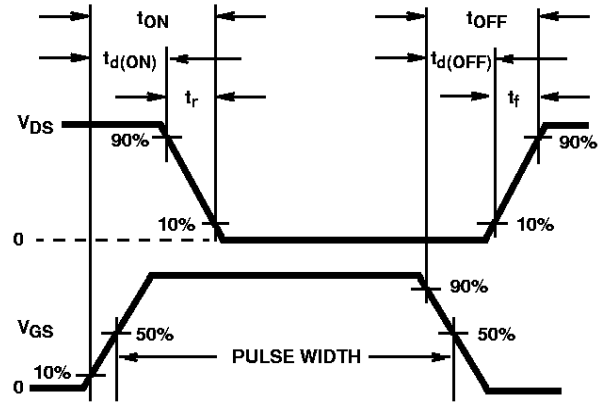FIGURE 16. SWITCHING TIME TEST CIRCUIT
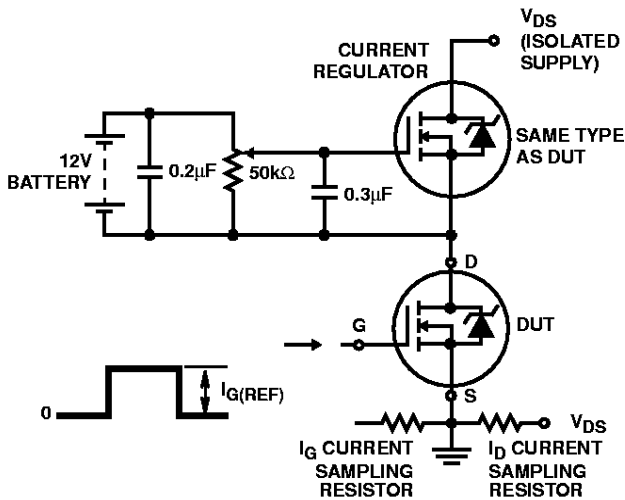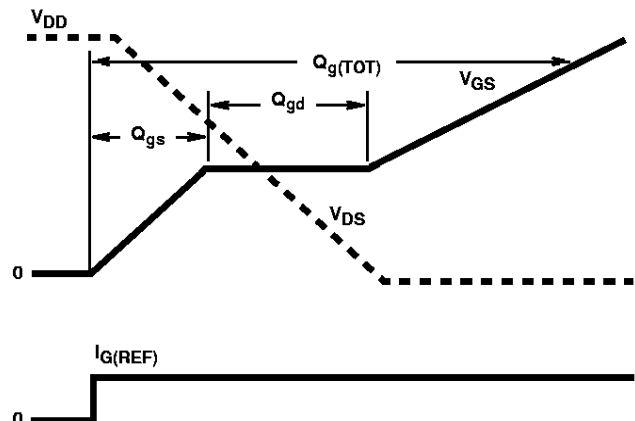
FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

FIGURE 18. GATE CHARGE TEST CIRCUIT

FIGURE 19. GATE CHARGE WAVEFORMS