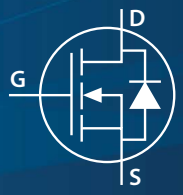
# EPC2218 – Enhancement Mode Power Transistor

$V_{DS}$, 100 V

$R_{DS(on)}$, 3.2 mΩ max

$I_D$, 60 A




EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low $Q_G$ and zero $Q_{RR}$. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

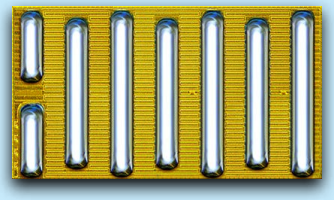
| Maximum Ratings | | | |
|---|---|---|---|
| PARAMETER | | VALUE | UNIT |
| $V_{DS}$ | Drain-to-Source Voltage (Continuous) | 100 | V |
| | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C) | 120 | |
| $I_D$ | Continuous ($T_A$ = 25°C) | 60 | A |
| | Pulsed (25°C, $T_{PULSE}$ = 300 µs) | 231 | |
| $V_{GS}$ | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| $T_J$ | Operating Temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage Temperature | -40 to 150 | |

| Thermal Characteristics | | | |
|---|---|---|---|
| PARAMETER | | TYP | UNIT |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.5 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board | 1.4 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 53 | |

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

| Static Characteristics ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 0.4 mA | 100 | | | V |
| $I_{DSS}$ | Drain-Source Leakage | $V_{GS}$ = 0 V, $V_{DS}$ = 80 V | | 0.08 | 0.35 | mA |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | $V_{GS}$ = 5 V | | 0.02 | 2.3 | |
| | Gate-to-Source Forward Leakage# | $V_{GS}$ = 5 V, $T_J$ = 125°C | | 0.6 | 9 | |
| | Gate-to-Source Reverse Leakage | $V_{GS}$ = -4 V | | 0.06 | 0.4 | |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 7 mA | 0.8 | 1.1 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS}$ = 5 V, $I_D$ = 25 A | | 2.4 | 3.2 | mΩ |
| $V_{SD}$ | Source-Drain Forward Voltage# | $I_S$ = 0.5 A, $V_{GS}$ = 0 V | | 1.5 | | V |

# Defined by design. Not subject to production test.



Die Size: 3.5 x 1.95 mm

**EPC2218 eGaN® FETs are supplied only in passivated die form with solder bars.**

## Applications

- DC-DC Converters
- BLDC Motor Drives
- Sync Rectification for AC/DC and DC-DC
- Point of Load Converters
- USB-C
- Lidar
- Class D Audio
- LED Lighting
- E-Mobility

## Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low $Q_G$
- Small Footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2218

| Dynamic Characteristics# ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 1189 | 1570 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 4.3 | | |
| $C_{OSS}$ | Output Capacitance | | | 562 | 843 | |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | $V_{DS}$ = 0 to 50 V, $V_{GS}$ = 0 V | | 740 | | |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 3) | | | 925 | | |
| $R_G$ | Gate Resistance | | | 0.4 | | Ω |
| $Q_G$ | Total Gate Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 5 V, $I_D$ = 25 A | | 10.5 | 13.6 | nC |
| $Q_{GS}$ | Gate-to-Source Charge | $V_{DS}$ = 50 V, $I_D$ = 25 A | | 3.2 | | |
| $Q_{GD}$ | Gate-to-Drain Charge | | | 1.5 | | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | | 1.9 | | |
| $Q_{OSS}$ | Output Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 46 | 69 | |
| $Q_{RR}$ | Source-Drain Recovery Charge | | | 0 | | |

# Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$.

**Figure 1: Typical Output Characteristics at 25°C**

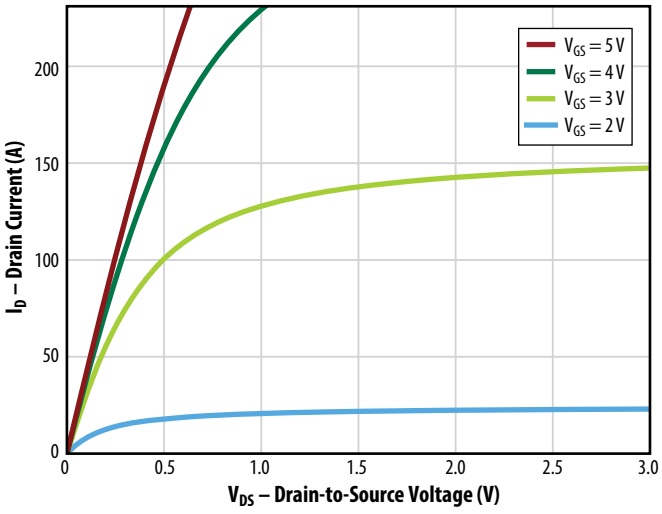



**Figure 2: Typical Transfer Characteristics**

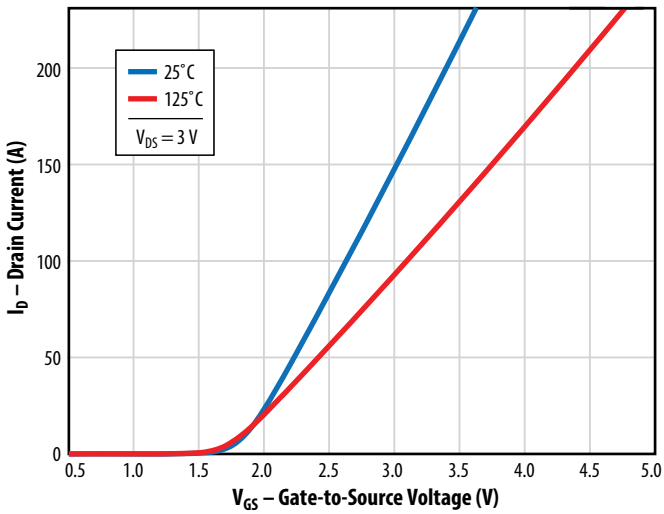



**Figure 3: $R_{DS(on)}$ vs. $V_{GS}$ for Various Drain Currents**

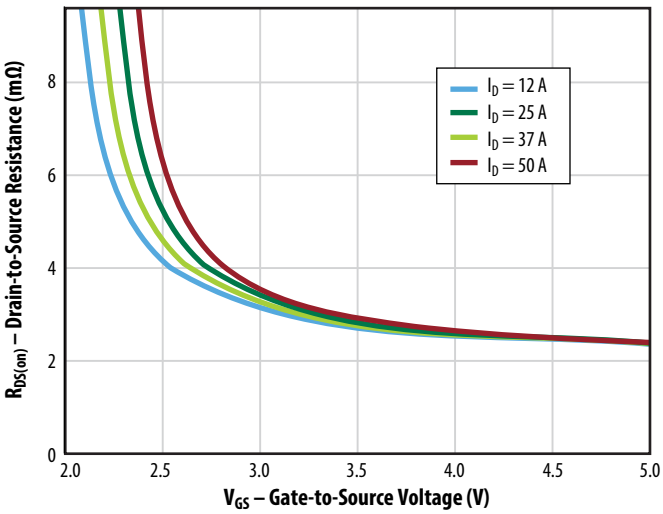



**Figure 4: $R_{DS(on)}$ vs. $V_{GS}$ for Various Temperatures**

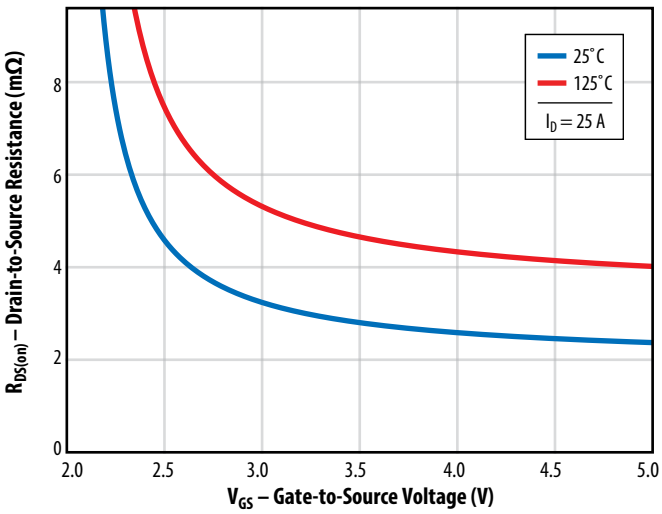


**Figure 5a: Typical Capacitance (Linear Scale)**

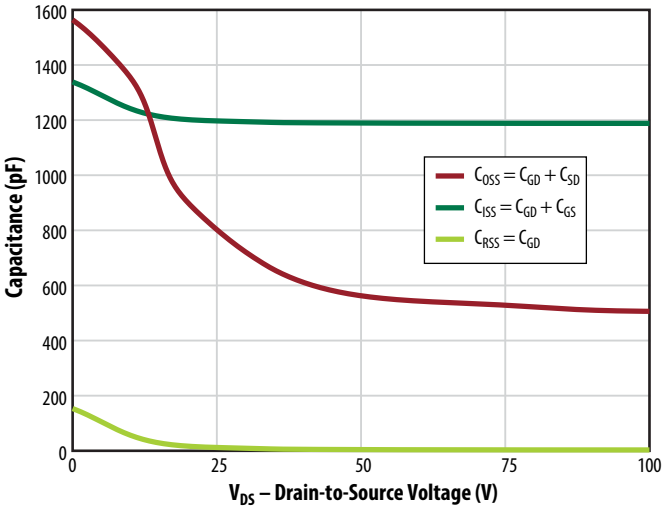



**Figure 5b: Typical Capacitance (Log Scale)**

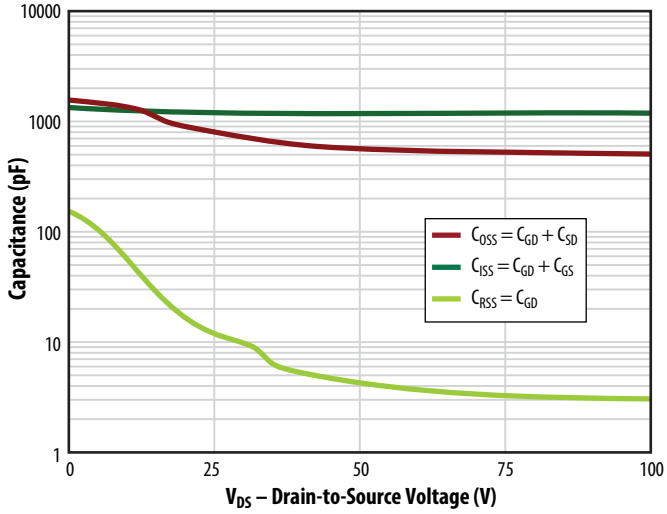



**Figure 6: Typical Output Charge and $C_{OSS}$ Stored Energy**

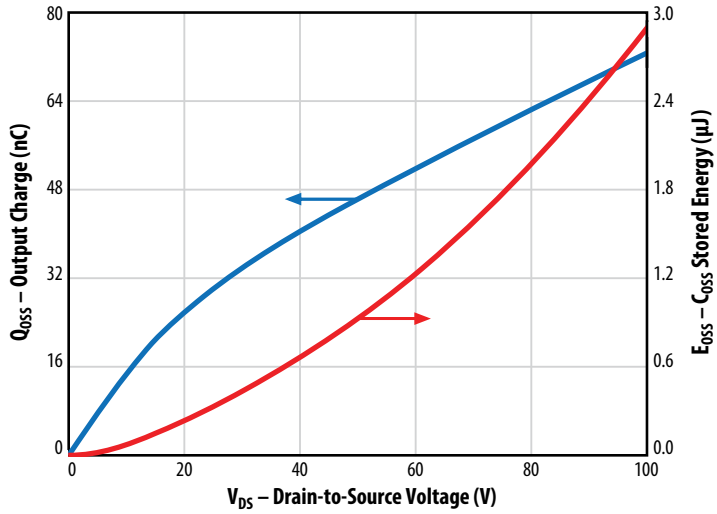



**Figure 7: Typical Gate Charge**

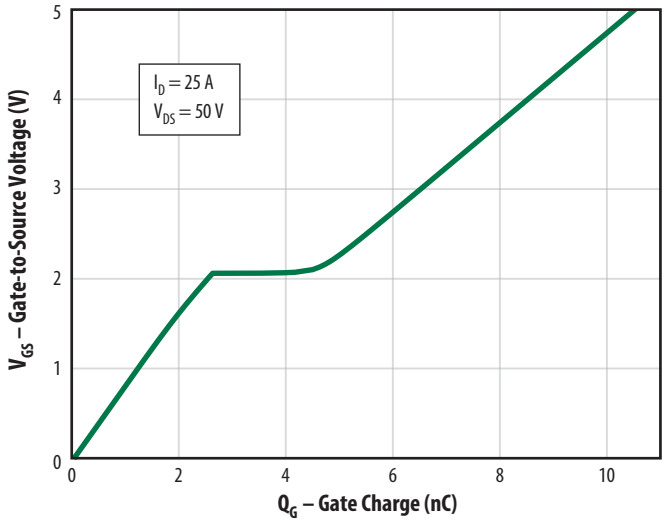
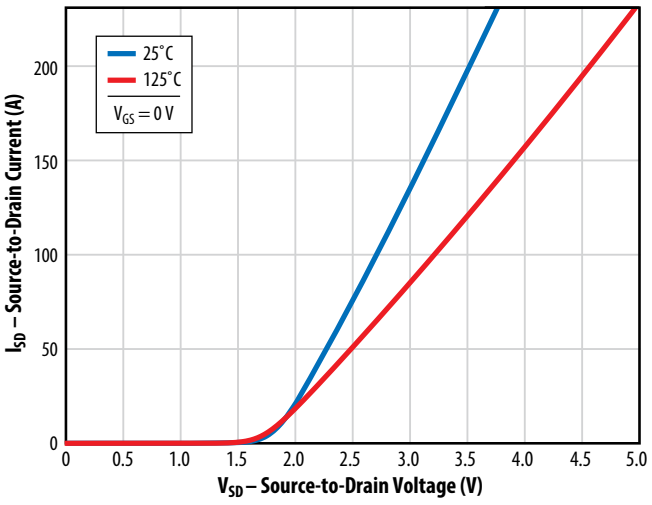



**Figure 8: Reverse Drain-Source Characteristics**




Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

**Figure 9: Normalized On-State Resistance vs. Temperature**

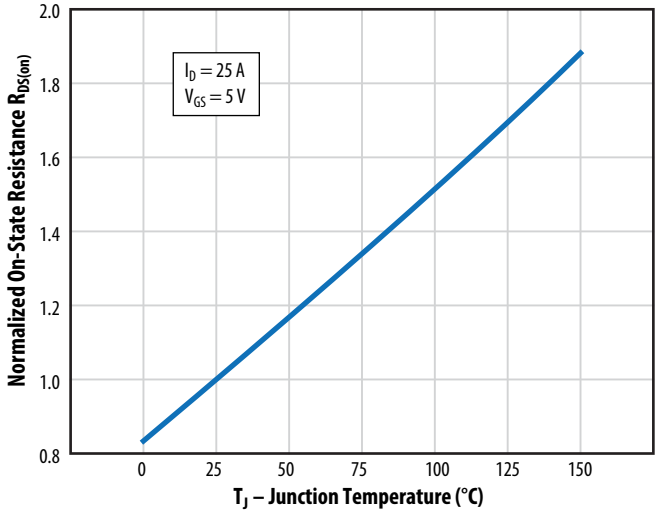


**Figure 10: Normalized Threshold Voltage vs. Temperature**

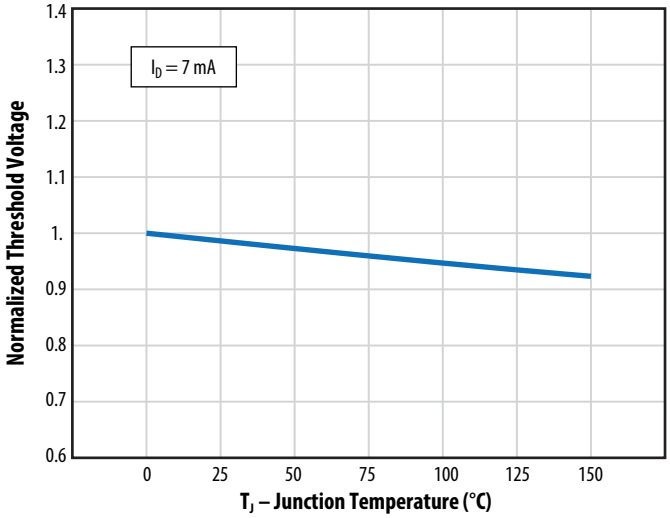
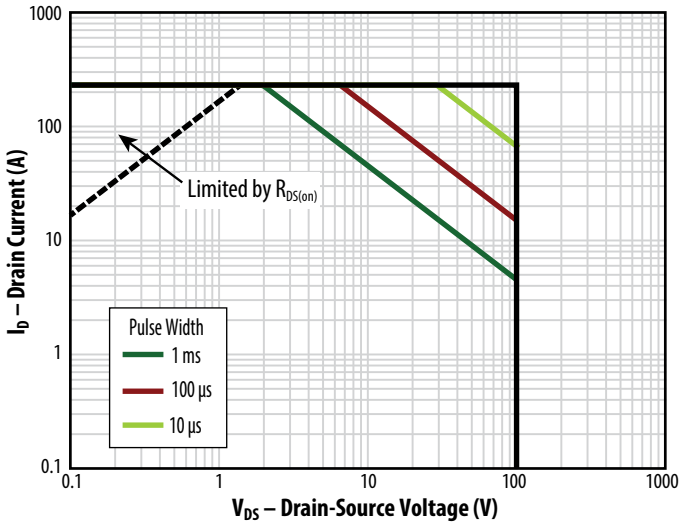


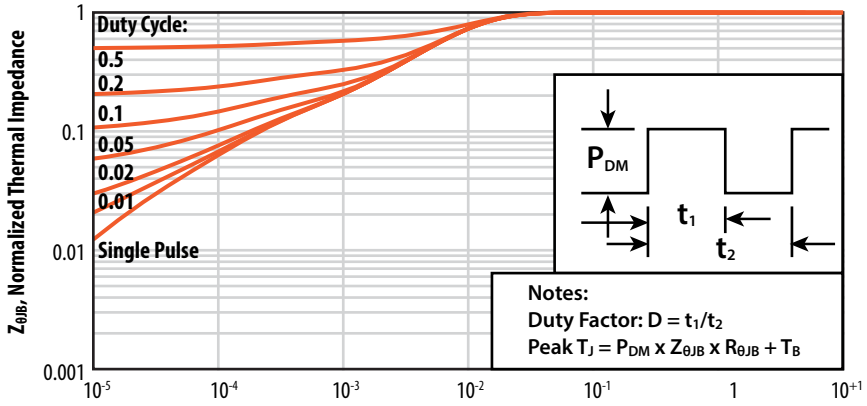

**Figure 11: Safe Operating Area**



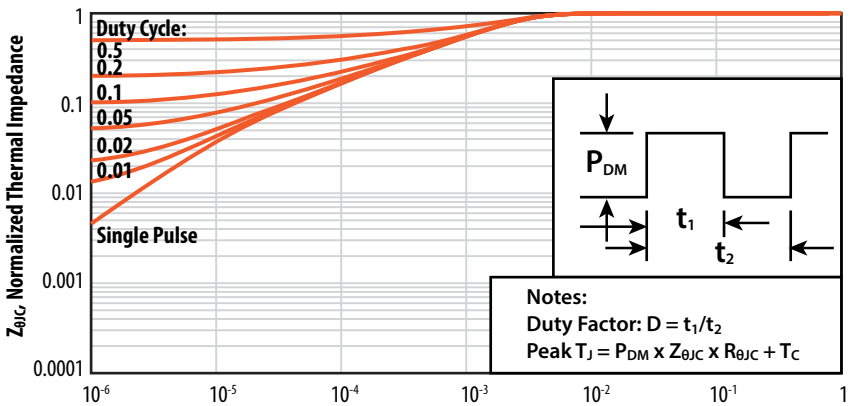

$T_J$ = Max Rated, $T_C$ = +25°C, Single Pulse

**Figure 12: Transient Thermal Response Curves**

Junction-to-Board

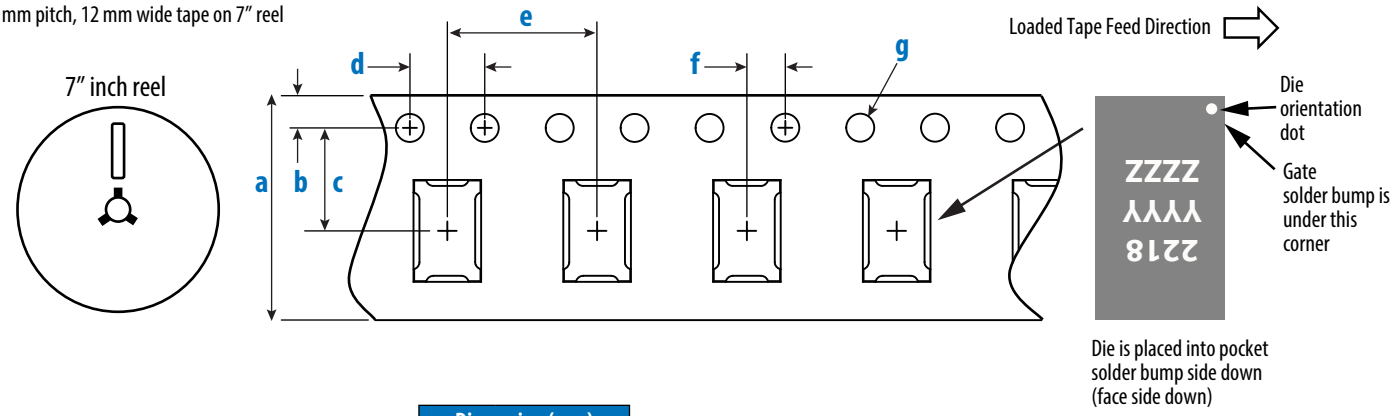



Junction-to-Case



## TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

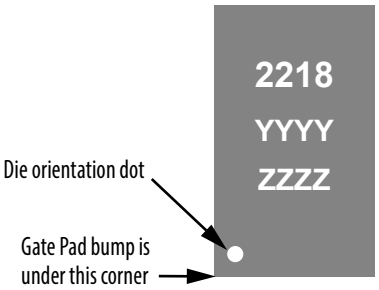



| EPC2218 (Note 1) | Dimension (mm) Target | MIN | MAX |
|---|---|---|---|
| a | 12.00 | 11.90 | 12.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (Note 2) | 5.50 | 5.45 | 5.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 8.00 | 7.90 | 8.10 |
| f (Note 2) | 2.00 | 1.95 | 2.05 |
| g | 1.50 | 1.50 | 1.60 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

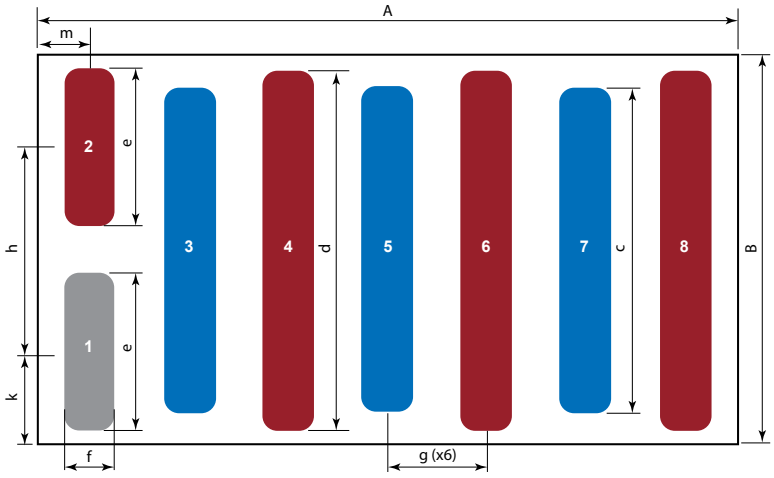
## DIE MARKINGS



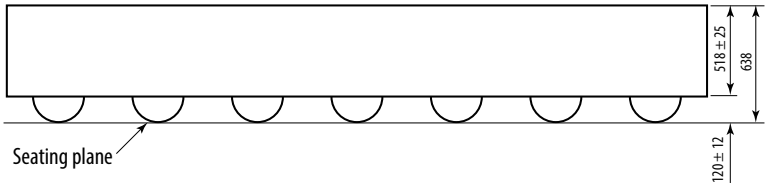

| Part Number | Laser Markings Part # Marking Line 1 | Lot_Date Code Marking Line 2 | Lot_Date Code Marking Line 3 |
|---|---|---|---|
| EPC2218 | 2218 | YYYY | ZZZZ |

## DIE OUTLINE

Solder Bump View




Side View




| DIM | Micrometers MIN | Nominal | MAX |
|---|---|---|---|
| A | 3470 | 3500 | 3530 |
| B | 1920 | 1950 | 1980 |
| c | 1605 | 1625 | 1645 |
| d | 1780 | 1800 | 1820 |
| e | 755 | 775 | 795 |
| f | 230 | 250 | 270 |
| g | | 500 | |
| h | | 1025 | |
| k | | 462.5 | |
| m | | 250 | |

Pad 1 is Gate;

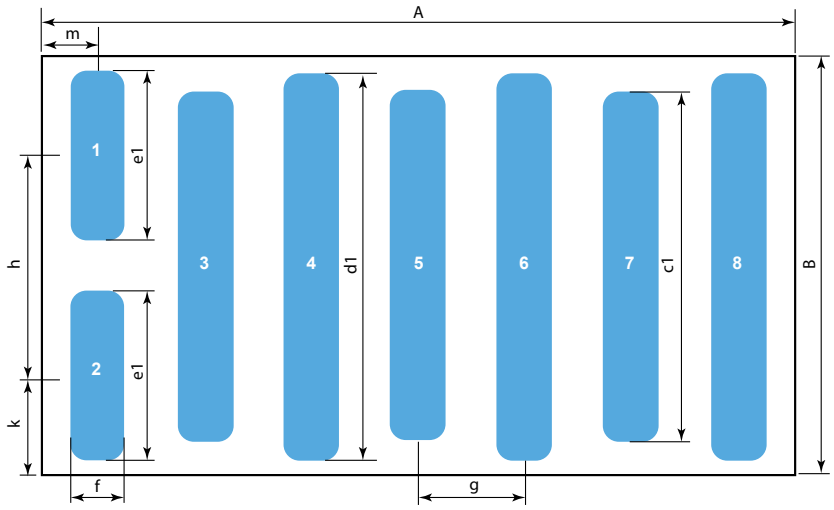
Pads 2 ,4, 6, 8 are Source;

Pads 3, 5, 7 are Drain

Note: Dimensions **d** and **c** are centered

## RECOMMENDED LAND PATTERN

*(units in µm)*



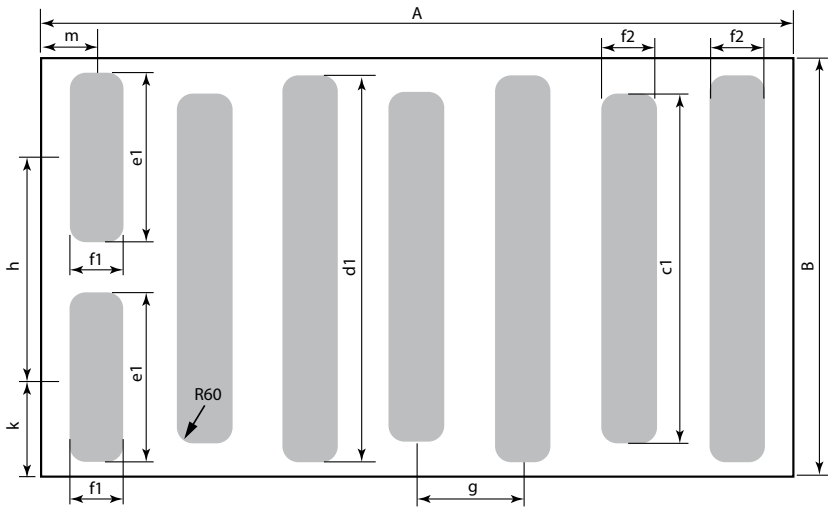

Land pattern is solder mask defined

| DIM | Nominal |
|---|---|
| A | 3500 |
| B | 1950 |
| c1 | 1605 |
| d1 | 1780 |
| e1 | 755 |
| f | 230 |
| g | 500 |
| h | 1025 |
| k | 462.5 |
| m | 250 |

Pad 1 is Gate;
Pads 2 ,4, 6, 8 are Source;
Pads 3, 5, 7 are Drain

## RECOMMENDED STENCIL DRAWING

*(units in µm)*




| DIM | Nominal |
|---|---|
| A | 3500 |
| B | 1950 |
| c1 | 1605 |
| d1 | 1780 |
| e1 | 755 |
| f1 | 230 |
| f2 | 210 |
| g | 500 |
| h | 1025 |
| k | 462.5 |
| m | 250 |

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

The corner has a radius of R60.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx