

Multilayer Ceramic Chip Capacitor

Part Number: 2211JA250221JKTSYX

2211 250Vac (Y2), 305Vac (X1), 50/60Hz / **Description:** 1000Vdc 220pF ±5% C0G/NP0 (1B) to AEC-

Q200

Approval IEC/EN60384-14:2013+A1

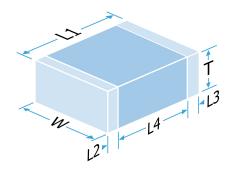
Specifications: UL60384-14, CAN/CSA E60384-14:14

Certification: TÜV R60153659 / ID1111233476

UL/cUL E228790-20201127

Classification: IEC/EN 60384-14:2013+A1 Class Y2 / X1

UL/cUL FOWX2, FOWX8



Component Marking and Certification Bodies:



Material Group I: CTI >= 600

Mechanical Specification

Size Code 2211

Length (L1) in mm (") $5.7 \pm 0.40 \ (0.225 \pm 0.016)$ Width (W) in mm (") $2.79 \pm 0.30 \ (0.11 \pm 0.012)$

Thickness (T) in mm (") 2.0 Max (0.08 Max)

Minimum Termination Band (L2,L3) in mm (") 0.50 (0.020)

Maximum Termination Band (L2,L3) in mm (") 0.80 (0.030)

Minimum Band Gap (L4) in mm (") 4.0 (0.158)

Termination Material Nickel Barrier, Sn Plated Solder (RoHS compliant)

Solderability IEC-60068-2-58

Packaging 7" Reel Horizontal Orientation, 500 per reel

General Electrical Specification

Rated Voltage

Humidity Grade

Maximum DC Working Voltage Nominal Capacitance Value Capacitance Tolerance

Tangent of Loss Angle (Tan δ)

Capacitance and Tan δ Test Conditions

Voltage Proof

(50mA max charging current for DC tests)
Min Insulation Resistance (IR)
Dielectric Classification

Rated Temperature Range

Maximum Capacitance Change over Temperature Range

Climatic Category (IEC)
Ageing Characteristic

Class Y2 (250Vac), Class X1 (305Vac), 50/60Hz, 5kV impulse

Grade III (IEC/EN60384-14:2013 Annex 1)

1000Vdc certified / (2500Vdc outside scope of any specification)

220pF ±5%

≤0.0015

1.0Vrms @ 1MHz

100% test: 4000Vdc 1s min / 5s max

AQL test: 4000Vdc / 3000Vac 60s min / 5kV 1.2x50µs impulse

100.00GOhm @ 100Vdc C0G/NP0 (1B) to AEC-Q200

-55°C / +125°C

No DC Voltage 0±30ppm/°C

Rated DC Voltage -

55/125/56

Zero

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Date: Thursday, September 02, 2021

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Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Compliant

REACH Compliant

211 compliant

California Proposition 65

No exposure risk

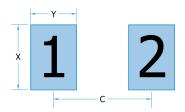
Board Layout

Knowles' conventional 2-terminal chip capacitors generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

IPC-7351 pad design

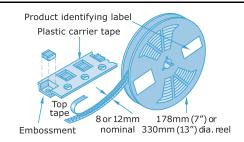
	2211	
С	5.40mm	0.213"
Υ	1.35mm	0.053"
Х	3.10mm	0.122"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



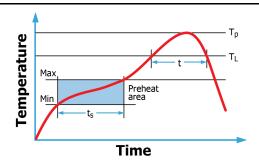
Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

DLI



Application notes with mounting and handling guidance are available on request.

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