Am93S48

Twelve-Input Parity Checker/Generator

Distinctive Characteristics

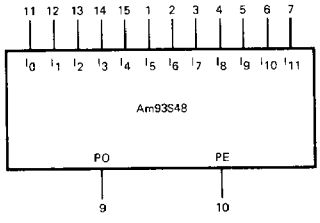
- Generates or checks parity over 12 bits
- Advanced Schottky technology
- Same delay to EVEN and ODD parity outputs
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am93S48 is a high-speed, 12-input parity checker or parity generator. The device is built using advanced Schottky technology and also incorporates PNP input transistors to reduce the input loading to only 0.4 STTL Unit Loads.

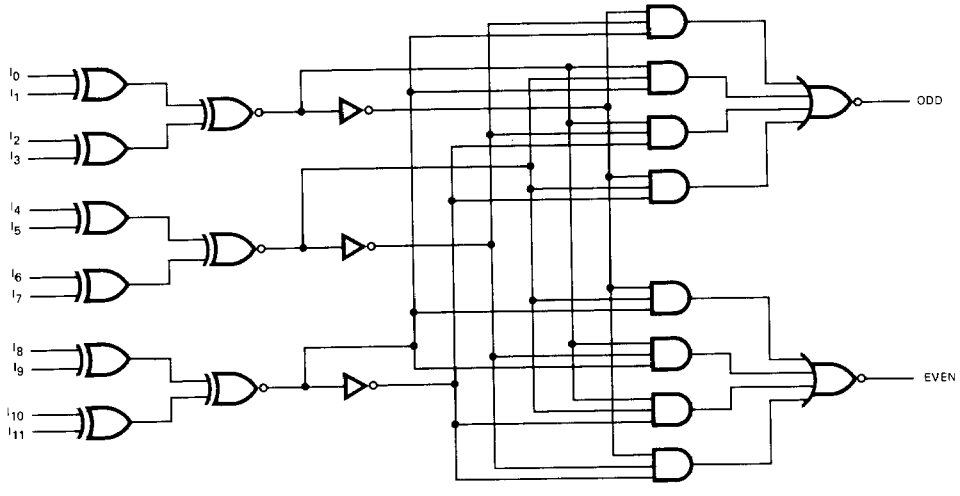
Both an ODD parity output and an EVEN parity output are obtained with the same propagation delay. This is accomplished by using an output structure that looks at the input as three 4-bit parity trees.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

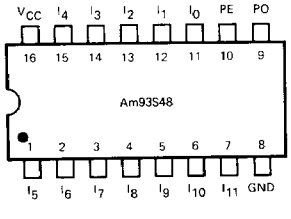
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	93S48PC
Hermetic DIP	0°C to +70°C	93S48DC
Dice	0°C to +70°C	93S48XC
Hermetic DIP	−55°C to +125°C	93S48DM
Hermetic Flat Pak	−55°C to +125°C	93S48FM
Dice	−55°C to +125°C	93S48XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150
Temperature (Ambient) Under Bias	−55°C to +125
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} m
DC Input Voltage	−0.5V to +5.
DC Output Current, Into Outputs	30r
DC Input Current	−30mA to +5.0r

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93S48XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am93S48XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	XC	2.7			Volts
			XM	2.5			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−0.8	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			57	80	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Both outputs open; all inputs at 4.5V.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	I_0 through I_{11} to Even Output	V_{CC} = 5.0V, C_L = 15 pF, R_L = 280Ω		19	28	ns
t_{PHL}				19	28	ns
t_{PLH}	I_0 through I_{11} to Odd Output			19	28	ns
t_{PHL}				19	28	ns

TRUTH TABLE

NUMBER OF I INPUTS		OUTPUT	
LOW	HIGH	ODD	EVEN
0	12	L	H
1	11	H	L
2	10	L	H
3	9	H	L
4	8	L	H
5	7	H	L
6	6	L	H
7	5	H	L
8	4	L	H
9	3	H	L
10	2	L	H
11	1	H	L
12	0	L	H

H = HIGH
L = LOW
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
I_5	1	0.4	–	–
I_6	2	0.4	–	–
I_7	3	0.4	–	–
I_8	4	0.4	–	–
I_9	5	0.4	–	–
I_{10}	6	0.4	–	–
I_{11}	7	0.4	–	–
GND	8	–	–	–
PO	9	–	20	10
PE	10	–	20	10
I_0	11	0.4	–	–
I_1	12	0.4	–	–
I_2	13	0.4	–	–
I_3	14	0.4	–	–
I_4	15	0.4	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS

I_0 through I_{11} The twelve inputs to the parity tree.

ODD The ODD parity output of the device. When an ODD number of I inputs are at a HIGH level, the ODD output will be HIGH.

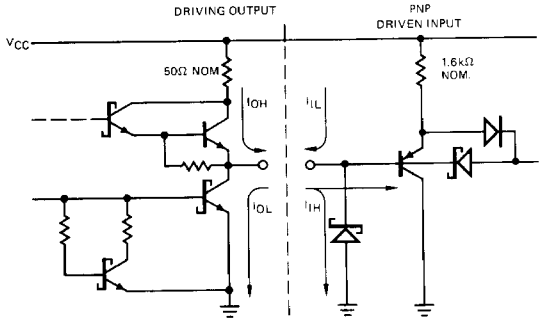
EVEN The EVEN parity output of the device. When an EVEN number of I inputs are at a HIGH level, the EVEN output will be HIGH.

LOGIC EQUATIONS

Odd Output = $I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$

Even Output = $\overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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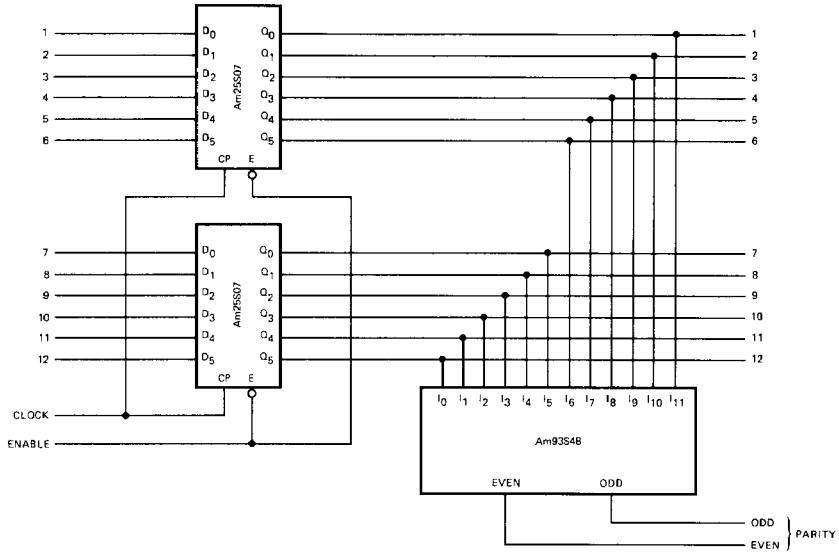
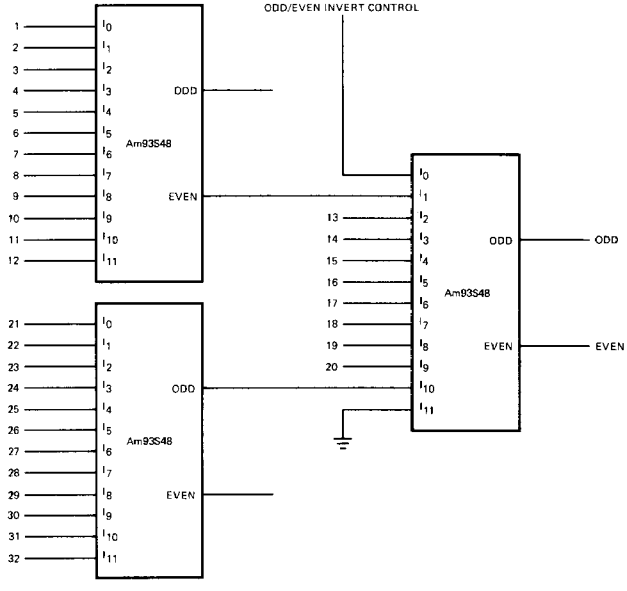
APPLICATIONS

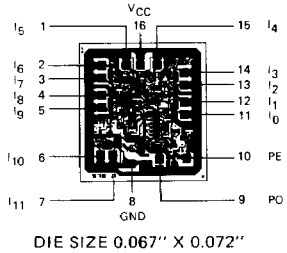
12-BIT PARALLEL ODD/EVEN PARITY CHECKER/GENERATOR



32-BIT PARITY CHECKER/GENERATOR



Metallization and Pad Layout



DIE SIZE 0.067" X 0.072"