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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR NP36N055HLE, NP36N055ILE, NP36N055SLE

SWITCHING N-CHANNEL POWER MOSFET

DESCRIPTION		★ ORD	ERING INFORMA	TION
These products are N-Channel MOS Field Effect			PART NUMBER	PACKAGE
Transistor designed for high current swit	tching applic	ations.	NP36N055HLE	TO-251 (JEITA) / MP-3
FEATURES			NP36N055ILE Note	TO-252 (JEITA) / MP-3Z
Channel temperature 175 degree rate	d		NP36N055SLE	TO-252 (JEDEC) / MP-3ZK
 Super low on-state resistance RDS(on)1 = 13 mΩ MAX. (VGS = 10 V, In RDS(on)2 = 16 mΩ MAX. (VGS = 5 V, In F Low Ciss : Ciss = 2900 pF TYP. 	,	Note	Not for new design.	
Built-in gate protection diode			0	
				(TO-251)
ABSOLUTE MAXIMUM RATINGS	(T _A = 25°0			
Drain to Source Voltage	VDSS	55 📀	V	
Gate to Source Voltage	Vgss	±20	V	
Drain Current (DC)	D(DC)	±36	A	
Drain Current (Pulse) Note1	D(pulse)	±144	А	
Total Power Dissipation ($T_A = 25^{\circ}C$)	Pr	1.2	W	(TO-252)
Total Power Dissipation (Tc = 25°C)	PT	120	W	
Single Avalanche Current Note2	las	36 / 33	А	
Single Avalanche Energy Note2	Eas	12 / 108	mJ	
Channel Temperature	Tch	175	°C	
Storage Temperature	Tstg	–55 to + 175	°C	
Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%				
2. Starting T_{ch} = 25°C, R_G = 25 Ω	, Vgs = 20 –	→ 0 V (See Figu	re 4.)	

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	1.25	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

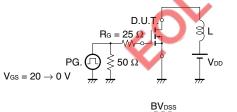
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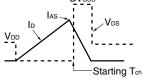
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 55 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	$V_{\text{GS(th)}}$	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2	2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 18 A	11	23		S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 18 A		10	13	mΩ
	RDS(on)2	V _{GS} = 5 V, I _D = 18 A		12	16	mΩ
	RDS(on)3	V _{GS} = 4.5 V, I _D = 18 A		13	18	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V		2900	4400	pF
Output Capacitance	Coss	V _{GS} = 0 V		370	560	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		180	330	pF
Turn-on Delay Time	td(on)	V _{DD} = 28 V, I _D = 18 A		22	48	ns
Rise Time	tr	V _{GS} = 10 V		14	36	ns
Turn-off Delay Time	td(off)	R _G = 1 Ω	5	69	140	ns
Fall Time	tr			12	29	ns
Total Gate Charge	Q _{G1}	V _{DD} = 44 V, V _{GS} = 10 V, I _D = 18 A		53	80	nC
	Q _{G2}	V _{DD} = 44 V		30	45	nC
Gate to Source Charge	QGS	V _{GS} = 5 V		9		nC
Gate to Drain Charge	Qgd	ID = 18 A		15		nC
Body Diode Forward Voltage Note	VF(S-D)	I⊧ = 36 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	trr	I⊧ = 36 A, V _{GS} = 0 V		42		ns
Reverse Recovery Charge	Qrr 👝	di/dt = 100 A/ <i>µ</i> s		60		nC

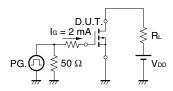
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TEST CIRCUIT 1 AVALANCHE CAPABILITY

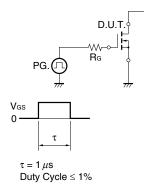


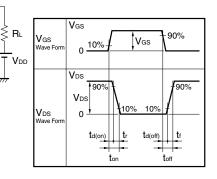


TEST CIRCUIT 3 GATE CHARGE



TEST CIRCUIT 2 SWITCHING TIME





TYPICAL CHARACTERISTICS (TA = 25°C)

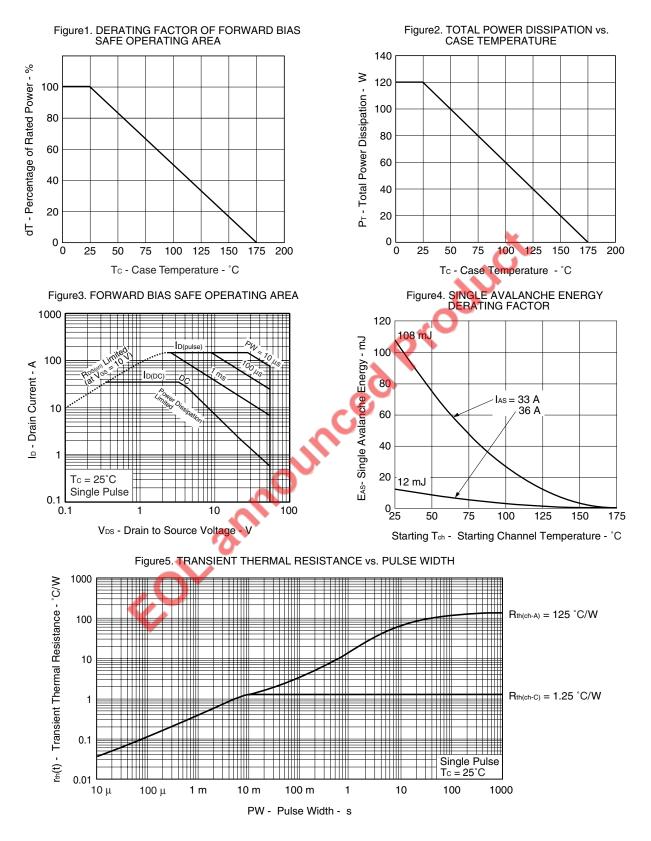
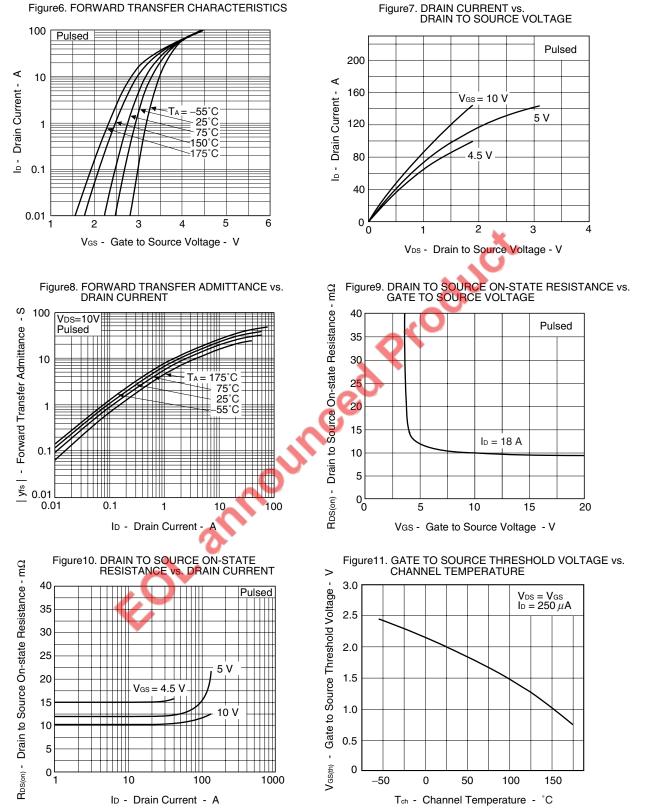
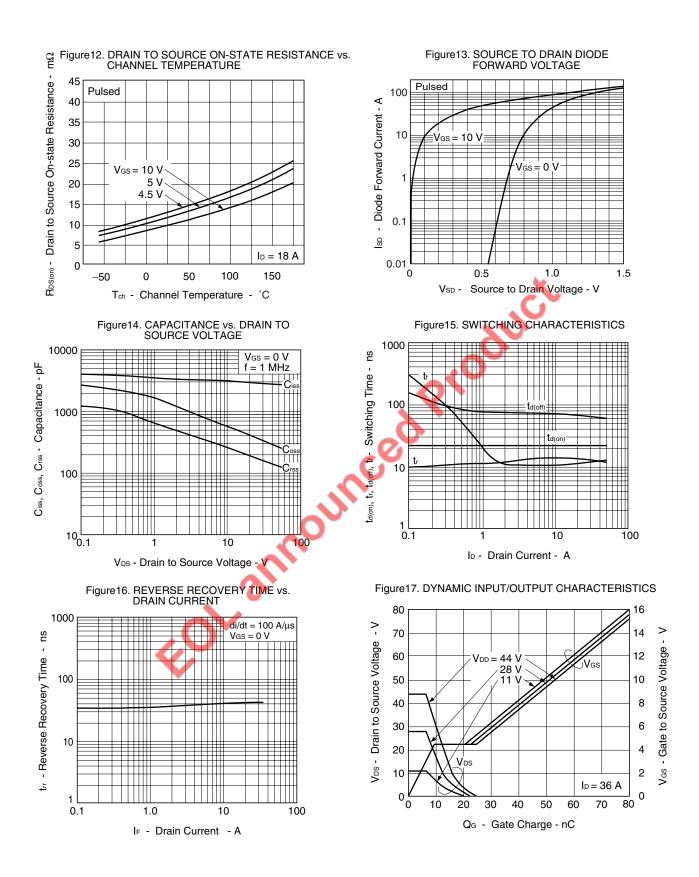


Figure6. FORWARD TRANSFER CHARACTERISTICS

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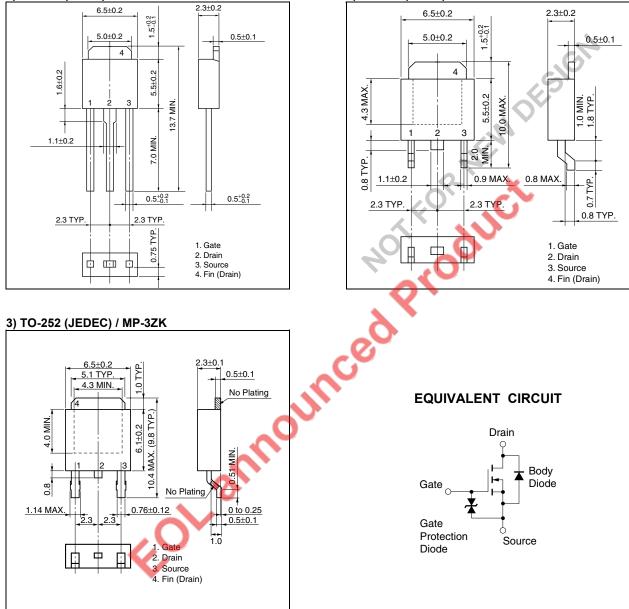
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2) TO-252 (JEITA) / MP-3Z

★ PACKAGE DRAWINGS (Unit: mm)





Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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