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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTORS

2SK2499, 2SK2499-Z

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2499 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

• Low On-Resistance

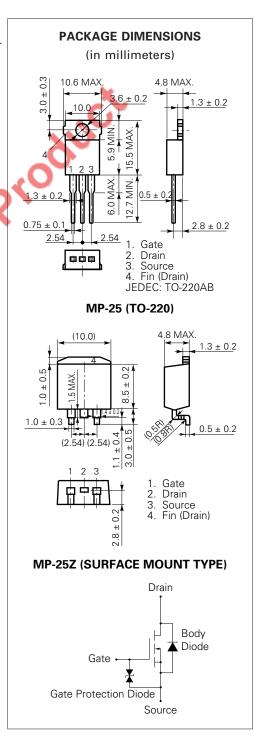
 $R_{DS(on)1} = 9 \text{ m}\Omega \text{ (VGS} = 10 \text{ V, ID} = 25 \text{ A)}$ $R_{DS(on)2} = 14 \text{ m}\Omega \text{ (VGS} = 4 \text{ V, ID} = 25 \text{ A)}$

- Low Ciss Ciss = 3 400 pF TYP.
- · High Avalanche Capability.
- · Built-in G-S Protection Diode

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	VDSS	60	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	ID(DC)	±50	Α
Drain Current (pulse)*	ID(puls	±200	Α
Total Power Dissipation (Tc = 25 °C)	P _{T1}	75	W
Total Power Dissipation (TA = 25 °C)	PT2	1.5	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current**	las	50	Α
Single Avalanche Energy**	Eas	250	mJ

- * PW \leq 10 μ s, Duty Cycle \leq 1 %
- ** Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0



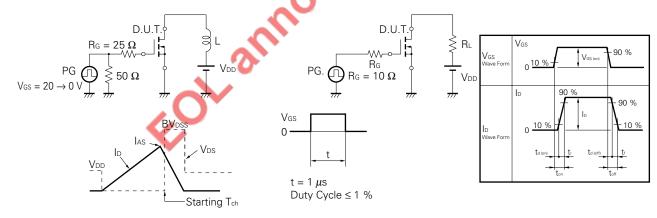


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

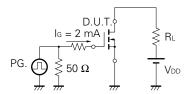
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-State Resistance	RDS(on)1		7.3	9.0	mΩ	Vgs = 10 V, ID = 25 A
	R _{DS(on)2}		11	14	mΩ	VGS = 4 V, ID = 25 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0	1.5	2.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	l yfs l	20	58		S	V _{DS} = 10 V, I _D = 25 A
Drain Leakage Current	loss			10	μΑ	V _{DS} = 60 V, V _{GS} = 0
Gate to Source Leakage Current	Igss			±10	μΑ	$V_{GS} = \pm 20 \text{ V, } V_{DS} = 0$
Input Capacitance	Ciss		3 400		pF	V _{DS} = 10 V
Output Capacitance	Coss		1 600		pF	V _{GS} = 0
Reverse Transfer Capacitance	Crss		770		pF	f = 1 MHz
Turn-On Delay Time	td(on)		55		ns	ID = 25 A
Rise Time	tr		360		ns	V _{GS(on)} = 10 V
Turn-Off Delay Time	td(off)		480		ns	$V_{DD} = 30 \text{ V}$
Fall Time	tf		360		ns	$R_G = 10 \Omega$
Total Gate Charge	Q _G		152		nC	lo = 50 A
Gate to Source Charge	Qgs		11		nC	V _{DD} = 48 V
Gate to Drain Charge	Q _{GD}		60		nC	V _{GS} = 10 V
Body Diode Forward Voltage	V _F (S-D)		0.92	Y	V	IF = 50 A, VGS = 0
Reverse Recovery Time	trr		105	2	ns	IF = 50 A, VGS = 0
Reverse Recovery Charge	Qrr		265		nC	di/dt = 100 A/μs

Test Circuit 1 Avalanche Capability

Test Circuit 2 Switching Time



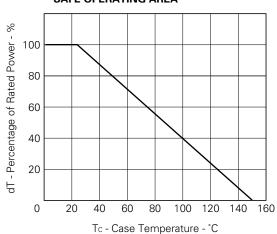
Test Circuit 3 Gate Charge



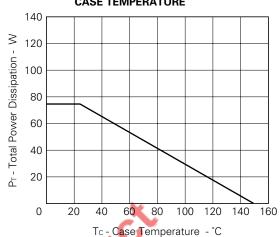
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS (TA = 25 °C)

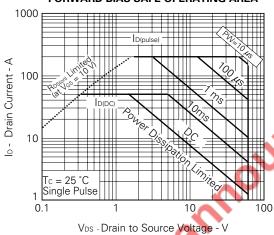




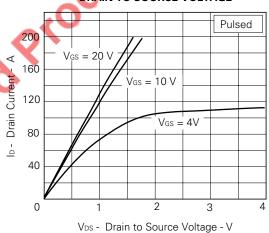
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



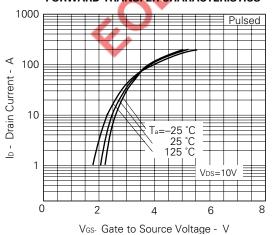
FORWARD BIAS SAFE OPERATING AREA



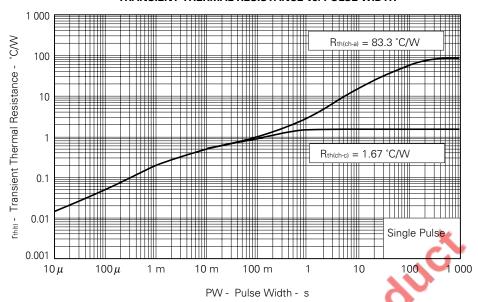
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



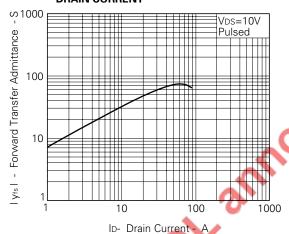
FORWARD TRANSFER CHARACTERISTICS



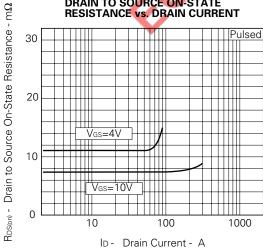
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



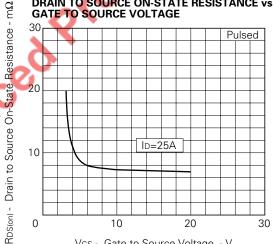
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

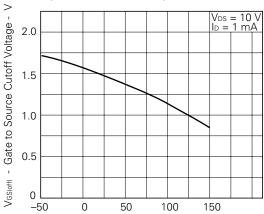


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

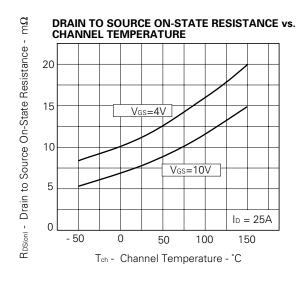


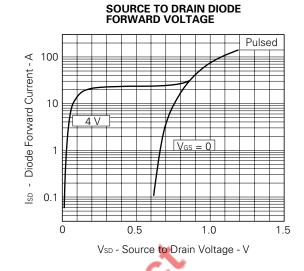
Vgs - Gate to Source Voltage - V

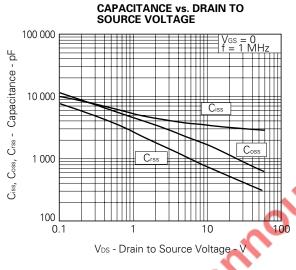
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

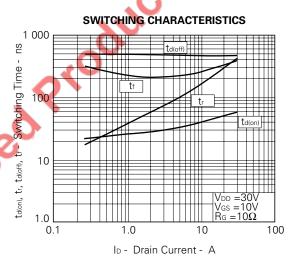


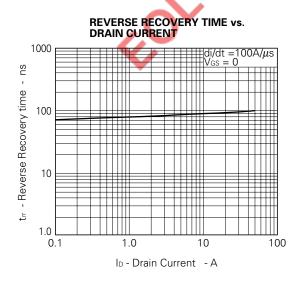
Tch - Channel Temperature - °C

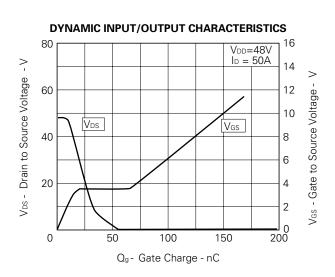












100

10

1.0

 $V_{DD} = 30 \text{ V}$ $V_{GS} = 20 \text{ V} \rightarrow 0$

 $0.1 \frac{R_G = 25 \Omega}{\Omega}$

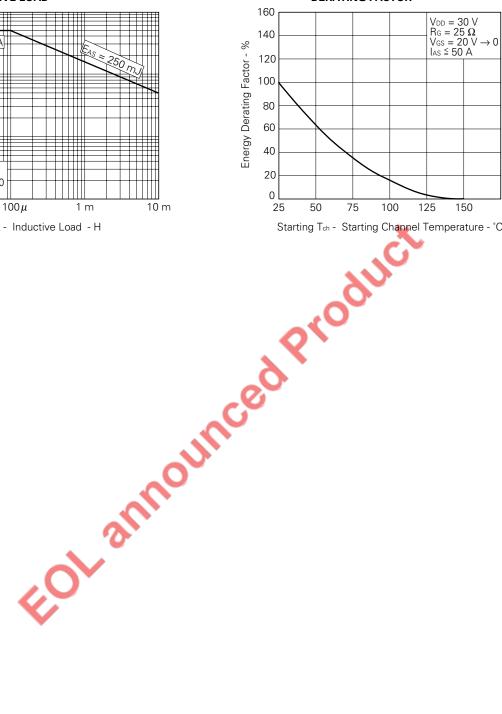
10 μ

las - Single Avalanche Current - A

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD Ias = 50 A

L - Inductive Load - H

SINGLE AVALANCHE ENERGY DERATING FACTOR



Starting Tch - Starting Channel Temperature - °C

REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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